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Structural Design of an Electrically Erasable EEPROM Memory Cell

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Abstract

EEPROM is an electrically erasable and programmable memory. The technology is mature and stable with low cost, so it is the mainstream in the application of electronic products in daily life. People use it in every way. In the fields of personal identity card, bank card, medical insurance card, traffic card and other smart cards, which are closely related to personal property, and in the field of communication system and other consumer electronic products such as PDA and digital camera, EEPROM is used. In instruments and other embedded systems, such as smart flowmeters, it is usually necessary to store information such as setting parameters, field data, etc., which requires that the system is not lost when it is powered down so that the data you originally set could be restored next time. Therefore, a certain capacity of EEPROM. Through the storage or release of electrons on the floating gate tube of the memory cell, the memory appears to be on or off when the floating gate tube is read, so its logic value will be judged as "0" Or "1". The definition of logic "0" or "1" varies depending on the logical design of the product. This work designs a memory cell consisting of two transistors. The NMOS tube is used as a selection tube and controlled by the word line. It can withstand a part of the high voltage and reduce the probability of breakdown of the ultra-thin oxide layer of the floating gate transistor. As a storage tube, the EEPROM device model designed in this paper can work well through the tunnel oxide layer to store data, achieving better storage functions, higher work efficiency, and lower power consumption.

Keywords

EEPROM Memory, Storage Array, Digital Logic Control Circuit

1. Introduction

Since the beginning of the 21st century, there have been more and more types of

portable consumer electronics products, and new varieties of semiconductor memories have been emerging. Among them, non-volatile semiconductor memory has become the main stream with its more advanced and more suitable characteristics for the development of the times. EEPROM memory (Electrically Erasable Programmable Read-Only Memory) is one of them. EEPROM uses a single power supply and is very convenient to use. It is widely used in the embedded IC card market and communication systems [1] [2].

Most of the EEPROM memory cells belong to floating gate devices, and their structures are also many. The earliest use was a metal-nitride-silica-silicon unit (MNOS) structure system. It uses the interface trap of the double-gate dielectric SiO_2/Si_3N_4 to store charge. A double-layer dielectric is used between the gate of the structure system and the silicon substrate. First, a thin SiO_2 layer is grown on the silicon substrate, about 3 nm thick, and then a layer of tens of nanometers thick Si_3N_4 is regrown. This makes the process difficult to control, at the same time, the stored charge is easy to leak through the ultra-thin silicon oxide, and its programming and erasing require different polarities to operate, which is not very convenient to use [3].

Currently, there are commonly used floating gate tunneling oxide (MOS) structure, referred to as FLOTOX; floating gate electronic tunnel (MOS) transistor structure, referred to as FETMOS; Gate), referred to as TPFG structure. This structure uses three layers of polysilicon, and the tunnel oxide layer is thick and difficult to be penetrated. Therefore, its data retention durability is particularly strong, but its polysilicon and oxide layer structure is complex [4]. Accurately manufacture the best product form, resulting in its wide application. Later, it also developed radiation-resistant ferroelectric memory (FeRAM), and high-speed, high-density, large-capacity flash memory (Flash Memory).

Compared with volatile memory, non-volatile memory has the characteristics of no loss of data during power failure. It mainly includes programmable read-only memory (PROM), ultraviolet programmable erasable read-only memory (EPROM), and electrically erasable programmable memory. Read-only memory such as read memory (EEPROM) and flash memory (Flash). In addition, in recent years, academic researchers have made innovative breakthroughs in the research of new non-volatile memory technologies, and made great scientific progress in the research of ferroelectric memories (Fe RAM), resistive memory (RRAM), etc. [5] [6]. Flash memory Flash is an improvement of EEPROM. It combines EEPROM with EPROM technology. It usually uses channel hot electron injection to achieve "write" and F-N tunneling effect to "erase". Flash erases the block area according to Block, so it has faster erase speed and can realize larger capacity data storage. However, because the block erase and the memory cell have no selection tube, it is easy to cause over-erase, the bit-wise erase is not accurate and reliable, the peripheral circuits are more complicated, and the chip cost is higher [7].

This work presents an electrically erasable EEPROM memory cell structure. By exploring various modules, master various key technologies in EEPROM de-

sign, such as memory arrays, digital logic control circuits, and peripheral circuits such as high-voltage generation circuits, Sensitive amplifier, etc. Through the above content, we can have a basic understanding of the core of the EEPROM, that is, the storage unit. This article also makes a detailed analysis of the overall structure of the EEPROM to understand its overall structure and understand the working process of the EEPROM, which is expected to bring great economic value.

2. Methods

2.1. EEPROM Cell Types

The EEPROM memory cell described in this article uses a floating gate tunnel oxide (FLOTOX) transistor. FLOTOX has a simple structure, high reliability, and good durability. The so-called durability means that it can maintain the rated opening window erasing times. At the same time, the process is simple and the transistor area is small, which is the mainstream of current applications [8]. The so-called floating gate refers to the addition of a layer of polysilicon gate between the conventional MOS gate and the substrate. Its structure is shown in Figure 1. There are two layers of polysilicon. The upper gate is the control gate. This control gate plays the role of word address selection during reading and writing. The external voltage, the floating gate below, is surrounded by a SiO_2 layer. There is a small window of ultra-thin oxide layer between the floating gate and the drain region, that is, the tunnel oxide layer. When the floating gate device operates, there is a transfer of electrons from the drain to the floating gate or the floating gate to the drain between the tunnel oxide layers This is the charging and discharging process of the floating gate [9], in which electrons are charged from the drain to the floating gate and charged from the floating gate to the drain.

FLOTOX works based on the F-N effect. When the two materials Si and SiO_2 are in close contact, since the conduction band of SiO_2 has a higher energy level

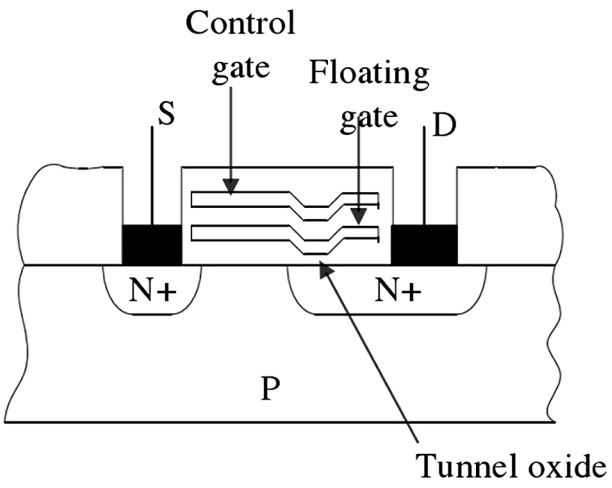

Figure 1. Floating-gate transistor structure.

than the conduction band of Si, there is an energy barrier at the interface between the two. When a sufficiently high electric field is applied to Si, the electrons in the conduction band of Si will have the possibility of quantum mechanical tunneling, and the energy barrier between the two will appear in the conduction band of SiO_2 [10]. The current generated by this type of electron tunneling increases exponentially with increasing electric field. When the electric field strength reaches about 107 V/cm, more electrons undergo tunneling, and the tunneling current becomes easier to observe. This is the Fowler-Nordheim tunneling effect, referred to as the F-N effect [11]. The floating gate EEPROM is designed based on this principle. Under a strong electric field (electric field greater than 107 V/cm), there is a process of electron transfer in the tunnel oxide layer, which is the working process of the erase or write operation, respectively [12]. The specific process is as follows: When the control gate is added with a level of about 20 V and the drain region is at 0 V level, a strong positive electric field exists between the floating gate and the drain due to the capacitive voltage division, which attracts electrons to the floating gate and makes the FLOTOX tube Become a high open tube. This state is defined as a "1" state. The process of charging the floating gate is called scrubbing; when the control gate is at a low level and the drain region is added with 20 V, the electrons on the floating gate are pulled to the drain region under a strong field. When there are no electrons on the floating gate, the FLOTOX tube is normally turned on. This state is defined as the "0" state. The process of pulling electrons from the floating gate to the drain is defined as writing or programming [13].

The voltage applied to the control gate creates a divided voltage inside the floating gate device. The greater the voltage between the tunnel oxide layers, the better the erasure performance. This voltage is obtained through the capacitive partial voltages existing between the two gates, between the floating gate and the drain region. Therefore, the smaller the oxide hole in the floating gate and drain region, the smaller the area, and the smaller the capacitance. The higher the voltage reached [14]. The capacitor voltage division of the FLOTOX device is shown in **Figure 2**.

Figure 2 clearly describes the approximate distribution of capacitors in the entire FLOTOX tube, which can be seen at a glance. C_C represents the capacitance between the control gate and the floating gate; C_{FD} is the capacitance between the floating gate ultra-thin tunnel oxide and the drain region. For a well-designed floating gate tube, the C_{FD} should be as small as possible, that is, the tunnel oxide layer should be as small as possible. Not only is the electric field strength affected by this, the data retention characteristics are also related to it. The smaller the area, the longer the data retention time. Therefore, the area of the tunnel hole that should be manufactured should be small enough, and at the same time, it should be guaranteed to be in a strong field greater than 107 V/cm. It will not be destroyed by breakdown [15]. For reliability, the rated turn-on voltage in the charging state must be greater than 5 V V_{CG}. The rated turn-on voltage in the discharged state is 0 V.

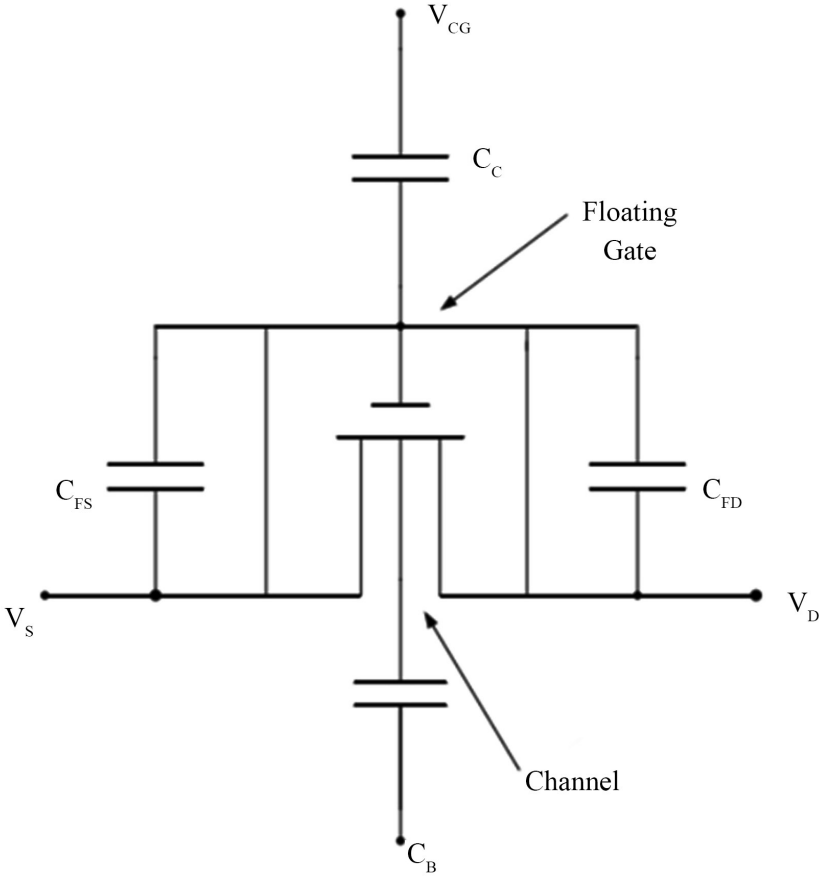

Figure 2. Capacitance voltage divider diagram of floating gate tube.

2.2. EEPROM Cell Structure

The floating-gate EEPROM memory cell uses two-tube cells, and its circuit diagram is shown in Figure 3. One is the NMOS selection tube, which is used as the cell address selection. The gate is connected to the word line (WL) and its drain bit line (BL). When performing a read operation, add a level of about 2.5 V to the control grid of the FLOTOX tube. Due to the previous erase and write operations, the turn-on voltage of the storage tube on the selected byte is different, some are cut off, and some are turned on. From this, it can be discriminated whether the unit stores "1" or "0".

In our design, the memory cell consists of two transistors. As shown in Figure 3, the NMOS tube is used as a selection tube and is controlled by the word line. It can withstand a part of the high voltage and reduce the probability of breakdown of the ultra-thin oxide layer of the floating gate tube. The floating gate transistor serves as a memory tube and stores data through a tunnel oxide layer.

2.3. Working Principle of EEPROM Memory Cell

EEPROM memory cells have three different working states: erase, write, and read. The details are described below in conjunction with Figure 4.

Erase state: A pulse voltage of about 20 V is applied to the control gate VCG

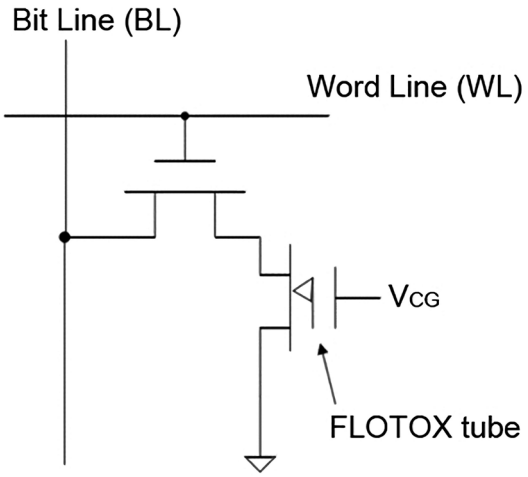

Figure 3. EEPROM memory cell.

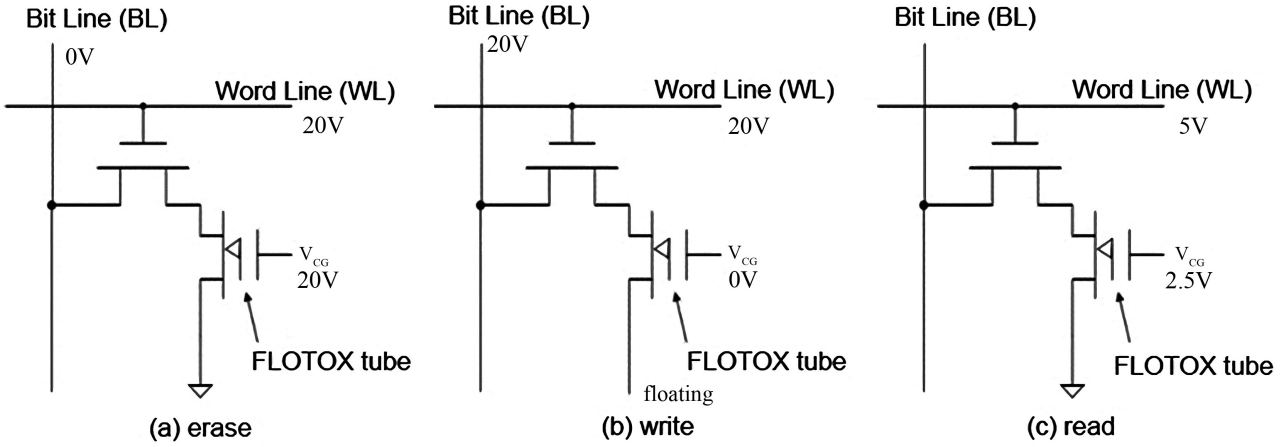

Figure 4. Work status of EEPROM memory cell.

and the word line WL of the FLOTOX tube, and the bit line is connected to 0 level. At this time, the control gate-floating gate capacitance and the floating gate-drain capacitance can divide the voltage so that the voltage in the floating gate-drain region is sufficiently large, so a strong electric field is generated in the tunnel region, attracting electrons to the floating gate, and making the floating gate When charging, the floating grid tube becomes a high-opening tube. This state is defined as a "1" state, and the process of charging the floating gate is called scrubbing.

Write state: The floating gate of the FLOTOX tube of the write unit is discharged. When 0 is written, the control gate VCG is at the 0 level, and high voltage is applied to the word line WL and the bit line BL. The electrons on the floating gate are pulled to the drain region under another strong field opposite to the erased state. There are no electrons on the floating gate. FLOTOX is normally turned on. This state is defined as the "0" state for the low turn on tube. Writing a "1" is the opposite and the control gate is high. The process of pulling electrons from the floating gate to the drain is defined as writing or programming.

Read status: Before the read operation, the bit line needs to be precharged to about 3.5 V. The control gate VCG is applied with a voltage of 2.5 V, and the word line WL is applied with a high level of 5 V. At this time, the tube is selected to be turned on. If there is no electron ("0" state) on the floating gate of the FLOTOX tube and the threshold voltage is less than 2.5 V, then FLOTOX The tube is turned on, and 0 is read on the bit line BL. If there are electrons on the floating gate of the FLOTOX tube ("1" state) and the threshold voltage is higher than 2.5 V, the FLOTOX tube is turned off and a "1" is read on the bit line BL.

The reprogramming time of the EEPROM is relatively long, and the number of reprogramming times is relatively low, so it usually works in the read state for ROM use. The working voltage of the memory cell is shown in Table 1.

Table 1 lists the drain voltage of the memory cell, the gate voltage of the selector tube, the gate voltage of the memory tube, and the source voltage under the three operating states of erase, write, and read. Through the function of the internal logic circuit, these different working voltages can be connected in different working states. The high-voltage generating circuit boosts the input voltage to provide the high voltage required for the memory unit to perform the erase/write operation; the sensitive amplifier distinguishes the memory units that have undergone different erase/write operations and reads the stored data; the row/column decoding is used separately In order to select the storage unit to be operated; the voltage of the circuit port is different in different operation modes, so the voltage switching module is used to switch the port voltage in different operation modes. The main function of the digital circuit is to control the timing, to issue operation instructions during read/erase/write, and the address selection of the operation object by the decoding circuit.

There are three operating modes of the memory, so there are erase signals, write signals, and read signal. In addition, an erase enable signal PE is also required. When the erase enable signal PE is high, the erase signal Eras and write signal can work. When the erase enable signal PE is low, the read signal is enabled high; the row address signal and column address signal are used for address selection; the sense amplifier needs charging requires a pre-charge signal.

3. Conclusion and Discussion

By introducing these contents, we can give readers a basic understanding of the core of EEPROM, *i.e.* storage unit. Through the function of internal logic circuit, different operating voltages could be connected to the circuit in different states. We can see from the article that EEPROM erasure does not need to resort to

Table 1. Operating voltage of storage unit.

Mode	V_D (V)	V_{SG} (V)	V_{CG} (V)	V_S (V)
Erase	0	20	20	0
Write	20	20	0	floating
Read	3.5	5	2.5	0

other devices. The content is modified with electronic signal, taking Byte as the minimum modification unit. It is unnecessary to clear all the data for writing so that the EEPROM is completely free from the shackles of EPROM Eraser and programmers, which makes it more widely used.

Conflicts of Interest

The author declares no conflicts of interest regarding the publication of this paper.

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