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The Design of Ternary Field-Effect Transistors, DRAM Memory and NAND Flash Memory

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Abstract

Based on the binary MOSFET and FinFET field-effect transistors, we have respectively designed ternary 0, +1, −1 digital signals using the improved MOSFET and FinFET field-effect transistors. On this basis, we have given the design principle and structure of ternary DRAM memory, that is, the reading +1, −1 and 0, and writing +1, −1 and 0 respectively, and also have given NAND flash memory, which include erasing operation, programming operation and reading operation. In addition, the arithmetic and logical operation rules of ternary are given. All the above works will lay a very important foundation for the development of ternary computer. All the above work will lay a very important foundation for the development of ternary computer.

Keywords

Ternary, MOSFET Field-Effect Transistor, FinFET Field-Effect Transistor, Arithmetic Operations, Logical Operation, DRAM Memory, NAND Flash Memory

1. Introduction

At present, electronic computers all adopt binary system, and the research on binary system is still going on. However, binary belongs to the lowest form in terms of numerical expression ability, and it represents two States, 1 and 0, with high and low levels. Although ternary system was put forward long ago, it has not received much attention due to the development of binary machine, which is now the most widely used computing system [1]-[3]. However, in the ever-changing computer system, binary can't occupy a permanent position, especially with the tide of miniaturization of devices, the disadvantages of binary logic of this binary

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have begun to appear: low storage density, difficult to further reduce wiring area and low signal transmission efficiency. People began to extend from this counting method based on 2 to a radix of 3 or even more, and gradually perfected its logic and mathematical operation rules, and put forward multivalued logic, among which ternary logic has been studied more and made some progress. The three bit states of ternary system can store more data and information in the same storage space, which improves the storage efficiency, which is of great significance for dealing with large-scale data and complex computing tasks. Ternary computers can complete calculations in fewer steps when dealing with certain tasks. For example, in logic operation and data processing, ternary system can directly represent more information by its three logic states −1, 0 and 1, and it needs more bits to represent the same information than binary system, thus reducing the operation steps and improving the operation speed. Moreover, in ternary logic, the transition between adjacent States is simpler than that in binary logic, and the corresponding energy consumption is lower [4]-[6]. AI is an important technological industry in the international development, but the main obstacle in its development process is that the binary system seriously affects its computing power. The transistors made with a ternary system will enable a breakthrough in the AI computing power bottleneck internationally, and may also significantly improve the energy efficiency of processor platforms under the same performance. With the decrease in cost and transistor scale, Moore's Law continues to hold. Therefore, the research on ternary systems and ternary computers is very necessary.

In the era of rapid development of modern information technology, MOSFET and Dynamic Random Access Memory (DRAM) have become key semiconductor technologies and hold a pivotal position in various electronic devices. This is because they serve as core components that support the efficient operation of modern electronic systems. From the computers and mobile phones we use daily to large servers and supercomputers, DRAM plays an indispensable role [7]-[9]. In the field of personal digital devices, DRAM is a major component of the main memory. While designing ternary field effect transistor, it is also necessary to design ternary DRAM.

In this paper, we have respectively designed ternary 0, +1, −1 digital signals using the improved MOSFET and FinFET field-effect transistors. Based on the binary MOSFET and FinFET field-effect transistors, we have added one gate, one drain and one drain-source. When a gate voltage V_{GS1} is applied to gate G1, a downward reverse output current I_{DS1} is generated between the source S and the low-voltage drain D1, representing the digital signal −1. At this time, the gate voltage V_{GS2} is not applied to gate G2. When a gate voltage V_{GS2} is applied to gate G2, an upward forward output current I_{DS2} is generated between the high-voltage drain D2 and D1, representing the digital signal +1. When the gate voltage is not applied to gates G1 and G2, the output current is not generated at the output terminal, representing the digital signal 0. On this basis, we have given the design principle and structure of ternary DRAM memory, that is, the reading +1, −1 and

0, and writing +1, −1 and 0 respectively, and also given NAND flash memory, which include erasing operation, programming operation and reading operation. In addition, the arithmetic and logical operation rules of ternary are given. All the above works will lay a very important foundation for the development of ternary computer.

2. The Basic Structure and Principle of Binary MOSFET

The MOSFET Field-Effect Transistor, is currently one of the most widely used types of field-effect transistors. It can serve as both an electronic switch and a signal amplifier. By applying voltage at the gate, it can regulate the current flow between the source and the drain [10]-[15]. With advantages such as low power consumption, fast switching speed, and ease of miniaturization and high-density integration, MOSFET holds a significant position in the field of integrated circuits. In industrial automation equipment, MOSFET is used to control the start, stop, and speed regulation of motors to achieve precise motion control. In the consumer electronics sector, MOSFET is one of the important application areas. The structure of a binary MOSFET is shown in **Figure 1**. Taking the N-channel enhancement type MOSFET as an example to illustrate its structure and working principle.

When there is no voltage, it is used to verify its working principle. When the gate voltage $V_{GS}=0$, there are two opposite PN junctions between the source and the drain. Regardless of the polarity of the drain-source voltage V_{DS}, there is always one PN junction reverse-biased. Therefore, there is no conducting channel, and at this time, it is equivalent to the 0 state in binary, and the current cannot pass effectively.

When the gate voltage V_{GS} is applied, that is, a forward voltage ($V_{GS}>0$) is applied between the gate and the source, since the insulating effect of the insulating layer, the gate current is zero. However, the gate metal layer accumulates positive charges, and these positive charges repel the holes near the SiO_2 side of the P-type substrate, leaving behind a region of negative ions that cannot move, forming a depletion layer. As V_{GS} increases, on the one hand, the depletion layer widens; on the other hand, the free electrons of the substrate are attracted to the depletion layer and the insulating layer, forming a thin N-type layer, called the inversion layer. This inversion layer constitutes the conducting channel between the drain and the source. When V_{GS} increases to a certain extent, the gate voltage at which the channel just forms is called the threshold voltage V_T. At this time, the Drain-to-source current I_D can be allowed to generate, and it flows from the drain to the source, equivalent to the 1 state in binary. When V_{GS} is greater than the threshold voltage V_T, as the V_{GS} voltage increases, the inversion layer becomes thicker, the resistance of the conducting channel decreases, and the Drain-to-source current I_D flowing through also increases. This is the transfer characteristic of MOSTFET, and its transfer characteristic curve is shown in **Figure 2**. From the above discussion, it can be seen that the basic working principle of MOSFET is to

control the conductivity of the channel by changing the gate voltage V_{GS}, thereby controlling the Drain-to-source current I_D.

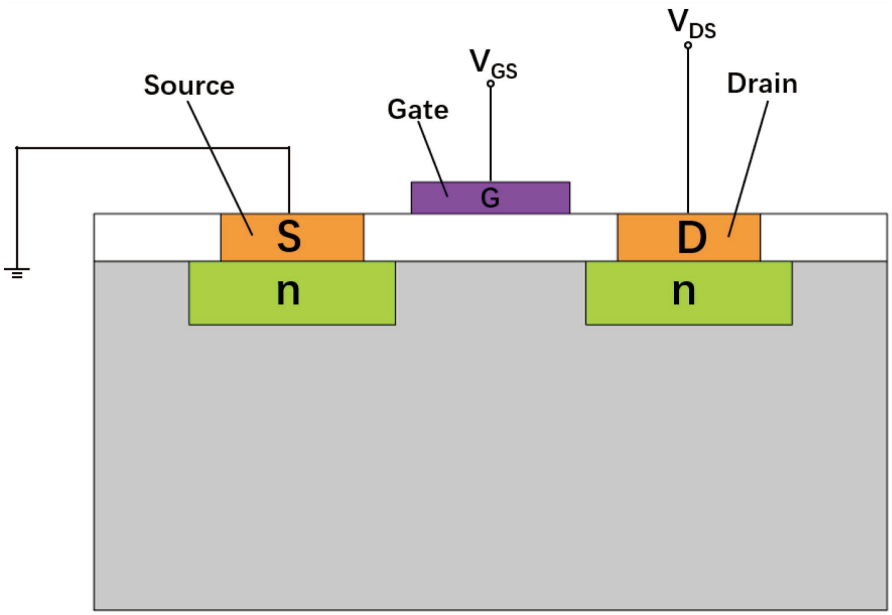

Figure 1. Binary MOSFET structure diagram.

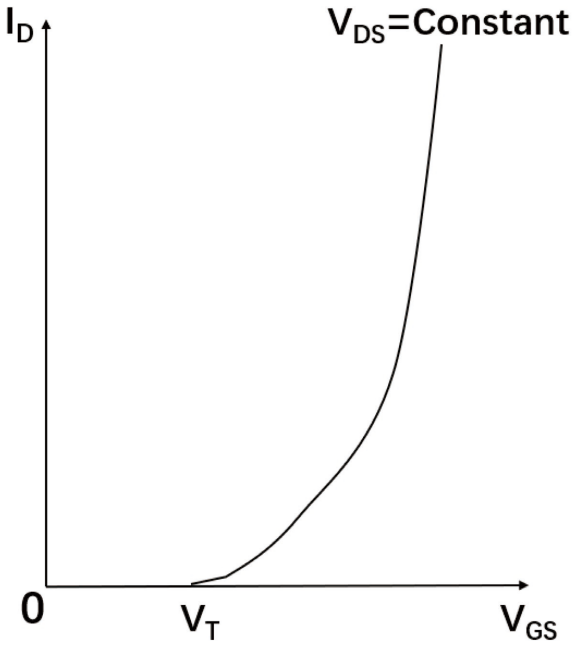

Figure 2. Transfer characteristic curve.

When the gate voltage V_{GS} is higher than the threshold voltage V_T, the inversion layer generates mobile charge carriers (electrons). The threshold voltage V_T is determined by the formula

$$V_T = \phi_{ms} - \frac{Q_0}{C_0} - \frac{Q_B}{C_0} + \psi_S, \tag{1}$$

where ϕ_{ms} is the work function of the MOSFET system, Q_0 is the positive charge per unit area, C_0 is the capacitance of the insulating layer, Q_B is the ionized acceptor charge in the depletion layer, and ψ_S is the surface potential.

The induced carrier charge Q_I supported by the applied bias V_{GS} and the threshold voltage V_T is

$$Q_I = -C_0\left(V_{GS} - V_T\right), \tag{2}$$

After adding the Source-drain voltage V_{DS}, if the potential V(y) is established in the horizontal outward direction from the drain in the vertical cross-section of the MOSFET, then the induced channel charge should be corrected to

$$Q_I = -C_0\left(V_{GS} - V_T - V\left(y\right)\right). \tag{3}$$

Since the carrier distribution within the channel is uniform and there is no concentration gradient, the channel current only contains the drift term of the electric field effect, and the drift current is the electron current.

$$I_D = -Z\mu_n Q_I \,\mathrm{d}V/\mathrm{d}y, \tag{4}$$

where Z represents the cross-sectional area through which the current flows, $\mu_n = q\tau_n / m_p^*$, τ_n is the hole relaxation times, and m_p^* is the effective mass of holes. Substituting formula (3) into (4) yields

$$I_D \mathrm{d}y = Z\mu_n C_0\left(V_{GS} - V_T - V\right)\mathrm{d}V, \tag{5}$$

integrating equation (5) from $y = 0$ to $y = L$ and from $V = 0$ to $V = V_{DS}$, we obtain

$$I_D = C_0\mu_n \frac{Z}{L}\left[\left(V_{GS} - V_T\right)V_{DS} - \frac{V_{DS}^2}{2}\right]. \tag{6}$$

Equation (6) is the leakage current equation, also known as the Sah equation. This is the fundamental equation that describes the DC characteristics of the non-saturation region of MOSFETs.

3. Ternary MOSFET Design

Based on the traditional design principle of binary MOSFET, we have improved its structure to design a ternary MOSFET structure, as shown in **Figure 3**.

Taking the n-channel semiconductor as an example, we choose p-type semiconductor as the substrate. Its structure is similar to that of a binary MOSFET, except that an additional gate, a drain and a drain-source voltage are added. Thus, there are two gates and two drains. There are three n-type semiconductors. The n-type semiconductor at the left end is connected to the metal as the source S, the n-type semiconductor in the middle and the n-type semiconductor at the right end respectively serve as the low-voltage drain D1 and the high-voltage drain D2. The low-voltage drain D1 is taken as the signal output terminal of the entire ternary MOSFET.

The designed structure can generate three digital signals of 0, +1 and −1. Specifically, if the signal output terminal D1 outputs an upward forward current, it is

defined as a +1 signal, if the signal output terminal D1 outputs a downward reverse current, it is defined as a −1 signal, and if the signal output terminal D1 does not output a current, it is defined as a 0 signal.

Two positive voltages are respectively applied to the two gates G1 and G2, namely V_{GS1} and V_{GS2} in Figure 3. Two positive voltages are respectively applied to the two drains D1 and D2, namely V_{DS1} and V_{DS2} in Figure 3, which are called drain-source voltages. Among them, V_{DS1} is the lower drain-source voltage and V_{DS2} is the higher drain-source voltage, with the source S grounded.

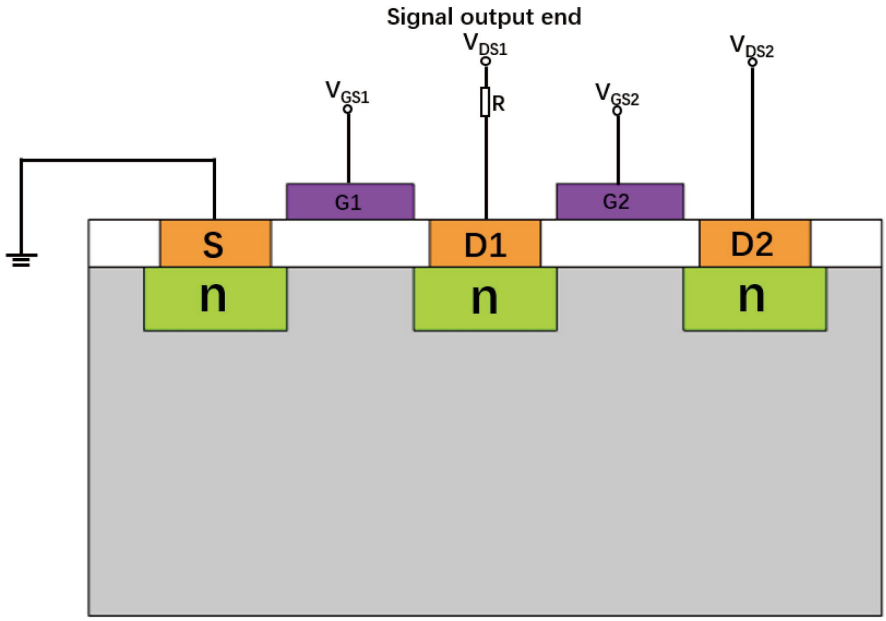

Figure 3. Basic structure diagram of ternary MOSFET.

When the gate voltage V_{GS1} is applied to the gate G1, a downward reverse current I_{DS1} is generated between the source S and the low-voltage drain D1, representing that the digital signal is −1, and the gate voltage V_{GS2} is not applied to the gate G2 at this time. When the gate voltage V_{GS2} is applied to the gate G2, an upward forward current I_{DS2} is generated between the drains D2 and D1, representing the digital signal +1, and the gate voltage V_{GS1} is not applied to the gate G1 at this time. When no gate voltage is applied to the gates G1 and G2, no current is generated at the output terminal V_{DS1}, which represents the digital signal 0. It can be seen that the designed MOSFET structure of Figure 3 can generate ternary 0, +1, −1 digital signals. The voltage digital signals of 0, +1 and −1 are obtained across the resistor R.

4. Basic Structure and Performance of Binary FinFET

The FinFET is Fin Field-Effect Transistor, as shown in Figure 4, it is a new type of complementary metal oxide semiconductor transistor, and its name comes from the similarity between the shape of the transistor and that of a fish fin. This

innovative design is derived from the traditional standard field effect transistor (FET) and plays a key role in the semiconductor field [16]-[19].

Starting from the single Fin N-channel FinFET, this paper elaborates on the basic working principle of FinFET devices. FinFET devices are four-terminal devices, having four ports: gate, source, drain, and substrate. Among them, the source and drain are two N-type semiconductor regions formed on the P-type substrate through heavy doping. To reduce the scattering effect of carriers due to impurities, the channel region of FinFET devices is usually lightly doped or undoped. The gate is isolated from the channel and the substrate through the gate oxide and channel oxide respectively. The three-dimensional structure diagram of the single Fin N-channel undoped FinFET device is shown in **Figure 4**.

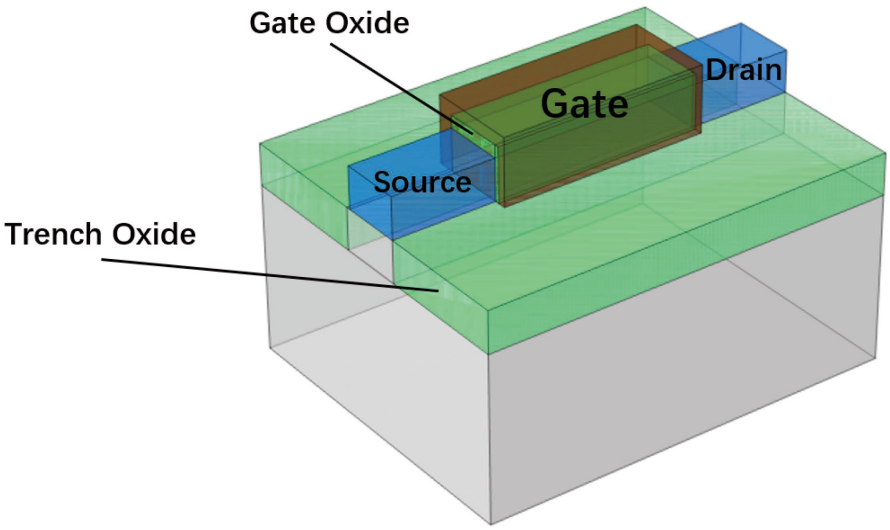

Figure 4. Schematic diagram of binary FinFET.

FinFET device is a voltage-controlled device. Under the control of the gate voltage, the current flows from one end of the fin to the other. If the gate width is defined as W, there are:

$$W = N_F \cdot N_{Fin} \cdot \left(W_{Fin} + 2H_{Fin}\right) \tag{7}$$

Where W_{Fin} is the width of the fin, H_{Fin} is the height of the fin, N_F is the exponent, and N_{Fin} is the number of single-finger fins. This fin structure increases the area of the gate around the channel and strengthens the control of the gate on the channel, thus effectively alleviating the short channel effect in the planar device, greatly improving the circuit control and reducing the leakage current. At the same time, FinFET does not need highly doped channel, which can effectively reduce the scattering effect of impurity ions and improve the channel carrier mobility. High mobility materials, such as strained germanium, are used as channel materials to improve carrier migration speed and transistor performance. But also integrate different functional materials to realize multi-functional chip design. In addition to the traditional double-gate and triple-gate structures, some manufacturers have studied more gate FinFET structures to enhance the control

ability of channel current. At the same time, FinFET is combined with other new device structures, such as carbon nanotube transistors, and high-performance semiconductor devices are developed by combining the advantages of different structures.

5. Trinary FinFET Design

Based on the design principle of binary FinFET, we have designed a ternary FinFET. Taking n-channel semiconductors as an example, that is, using p-type semiconductors as the substrate, and using three n-type semiconductors and two metal gates. The left n-type semiconductor is the source and is grounded, while the middle n-type semiconductor and the right n-type semiconductor are respectively the low-voltage drain and the high-voltage drain. At the same time, the middle low-voltage drain is used as the signal output terminal, as shown in Figure 5. When the gate voltage and the drain-source voltage are respectively applied to Gate 1, the low-voltage drain and the source, the drain-source current I_{DS1} can be generated. At this time, the output current signal is a reverse current (current flows out of the low-voltage drain), which is used as the digital signal −1. If the gate voltage of Gate 1 is turned off, the middle low-voltage drain is used as the source. When the gate voltage is applied to Gate 2, and the drain-source voltage is applied to the low-voltage drain and the right high-voltage drain, the drain-source current I_{DS2} can be generated. At this time, the output current signal is a forward current (current flows into the low-voltage drain), which is used as the digital signal +1. When no voltage is applied to Gate 1 and Gate 2, there is no current passing through the low-voltage drain, which is the signal output terminal, and it is used as the digital signal 0. It can be seen that the FinFET structure designed in Figure 5 can generate ternary 0, +1, −1 digital signals.

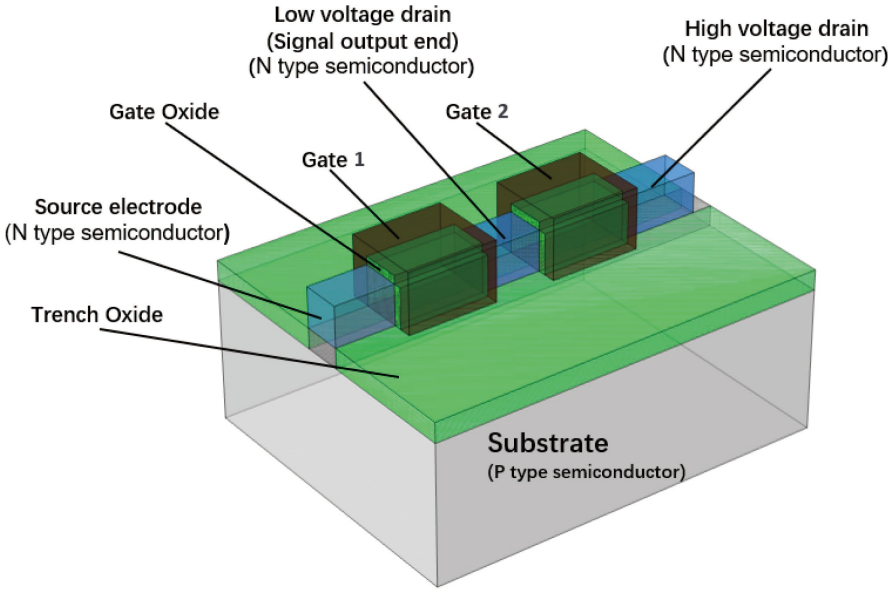

Figure 5. Schematic Diagram of Binary FinFET.

6. Ternary Arithmetic Operation

The ternary arithmetic operation are as follows:

1) The ternary addition operation rule:

$$0+0=0;\ \ 0+1=1;\ \ 0+(-1)=-1;\ \ 1+(-1)=0;\ \ 1+1=1-1;$$

$$-1+(-1)=-11;\ \ 1+1+1=10;\ \ -1+(-1)+(-1)=-10.$$

With the ternary addition operation rule, the ternary addition of $110(-1)$ and $100(-1)$ is $110(-1)+100(-1)=1(-1)1(-1)1$, which is equivalent to the decimal addition: $35+26=61$.

2) The ternary subtraction operation rule:

$$0-0=0;\ \ 0-1=-1;\ \ 0-(-1)=1;\ \ -1+1=0;\ \ 1-(-1)=1-1;$$

$$-1-1=-11;\ \ 1-(-1)-(-1)=10;\ \ -1-1-1=-10.$$

With the ternary subtraction operation rule, the ternary subtraction of $1(-1)01$ and $(-1)011$ is $1(-1)01-(-1)011=1(-1)(-1)0$, which is equivalent to the decimal subtraction: $19-(-23)=42$.

3) The ternary multiplication operation rule:

$$1\cdot 1=1;\ \ 1\cdot(-1)=-1;\ \ -1\cdot(-1)=1;\ \ 1\cdot 0=-1\cdot 0=0;\ \ 0\cdot 0=0.$$

4) The ternary division operation rule:

Judge the absolute values of the dividend and the divisor. If the absolute value of the dividend is greater than that of the divisor, then the quotient is 1 or −1. Specifically, when the dividend and the divisor have the same sign, the quotient is 1, and when the dividend and the divisor have different signs, the quotient is −1. If the absolute value of the dividend is less than that of the divisor, the quotient is 0, and a 0 is added at the lowest bit. Then subtract the product of the divisor and the obtained quotient from the dividend, take the remainder as the new dividend, and repeat the previous steps.

7. The Ternary Logical Operation Rule

1) The Logical AND operation rule:

1AND1 = 1; 0AND0 = 0AND1 = 1AND0 = 0;

1AND(−1) = (−1)AND1 = −1AND0 = 0AND(−1) = −1AND(−1) = −1.

2) The Logical OR operation rule:

−1OR(−1) = −1; 0OR0 = 0OR(−1) = (−1)OR0 = 0;

0OR1 = 1OR0 = 1OR1 = 1OR(−1) = −1OR1 = 1.

3) The Logical NOT operation rule:

NOT0 = 0; NOT1 = −1; NOT(−1) = 1.

The logic operation diagrams are shown in **Figure 6**, **Figure 7** and **Figure 8**.

4) Logical operation rule

The commutative rule: $x_1+x_2=x_2+x_1$, $x_1\cdot x_2=x_2\cdot x_1$.

The associative rule: $(x_1+x_2)+x_3=x_1+(x_2+x_3)$, $(x_1\cdot x_2)\cdot x_3=x_1\cdot(x_2\cdot x_3)$.

The absorption rule: $x_1+x_1\cdot x_2=x_1$, $x_1\cdot(x_1+x_2)=x_1$.

AND	-1	0	1
-1	-1	-1	-1
0	-1	0	0
1	-1	0	1

Figure 6. Logical AND operation.

OR	-1	0	1
-1	-1	0	1
0	0	0	1
1	1	1	1

Figure 7. Logical OR operation.

NOT	-1	0	1
	1	0	-1

Figure 8. Logical NOT operation.

The distributive rule: $x_1 \cdot (x_2 + x_3) = x_1 \cdot x_2 + x_1 \cdot x_3$.

The duality rule: Replace "+1" with "·" and "·" with "+1" in the above expression, the equations still holds.

Where x_1, x_2, x_3 represented in the balanced ternary system(0, +1, −1).

8. Design of Ternary DRAM Memory Cell

The design of ternary DRAM is shown in Figure 9. We have defined that the ungrounded end of the capacitor is positively charged to represent the digital signal "+1", the ungrounded end of the capacitor is negatively charged to represent the digital signal "−1", and the ungrounded end of the capacitor is uncharged to represent the digital signal "0". The forward current is defined as electrons moving from the bit line to the capacitor, and the reverse current is defined as electrons moving from the capacitor to the bit line.

8.1. Ternary DRAM Reading Operation

1) The reading operation of +1 for the ternary DRAM

The specific operation steps are as follows: firstly, the row address is decoded and the row line is activated; the row decoder selects the required row according to the row address signal (RAS), pulls the row line to a high voltage, turns on the transistor on the row, and connects the capacitor and the bit line. When reading +1, because the internal storage state is "+1", the ungrounded end of the capacitor carries positive charge at this time, and the bit line voltage is pulled to 0V, then

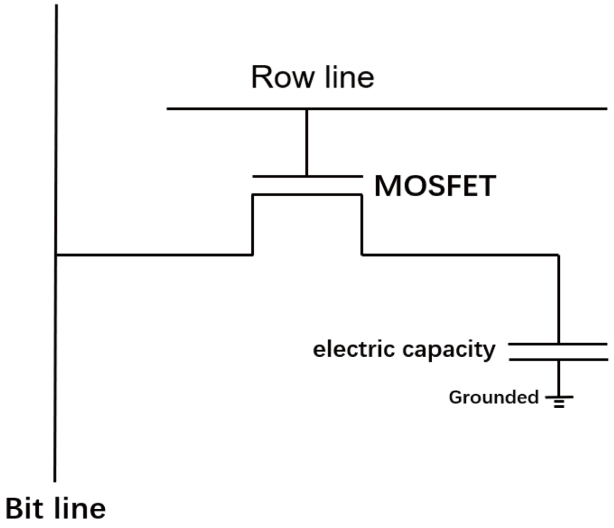

Figure 9. The structure diagram of ternary DRAM.

the capacitor discharges to the bit line and a forward current appears, and the sense amplifier detects a weak forward current, which pulls the bit line voltage to a positive voltage representing the signal "+1", and the amplified signal "+1" is transmitted to the outside through the data bus to complete the operation of reading "+1". Because the capacitor discharges to the bit line, the positive charge is reduced, and the sense amplifier rewrites the read-out data to the capacitor, so that the capacitor can recover its charge state and ensure that the data is not lost after the reading operation. The row line voltage is reduced to 0V again, and the field effect transistor is turned off, and the connection between the capacitor and the bit line is disconnected, as shown in Figure 10.

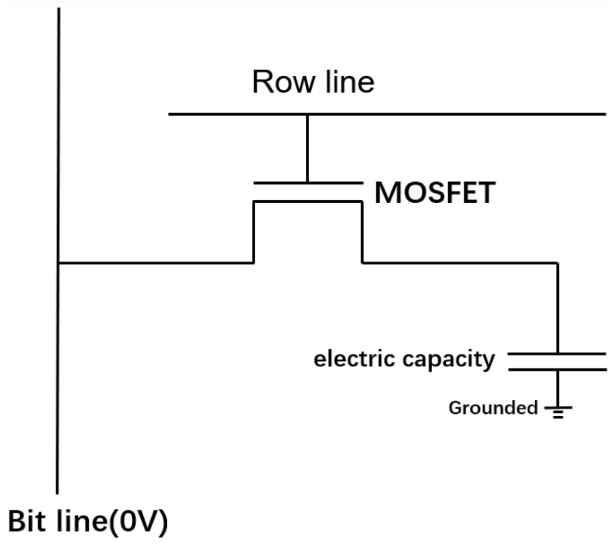

Figure 10. The structure diagram of ternary DRAM for reading operation.

2) The reading operation of −1 for the ternary DRAM

The specific operation steps are as follows: Firstly, the row address is decoded and the row line are activated. The row decoder selects the required row according to the row address signal (RAS), pulls the row line to a high voltage, turns on the transistor on the row, and connects the capacitor and the bit line. During the reading operation of −1, since the internal storage state is "−1", at this time, the ungrounded end of the capacitor carries negative charges. The bit line voltage is pulled down to 0V, causing the capacitor to discharge to the bit line. A reverse current occurs, and the sense amplifier detects the weak reverse current, pulling the bit line voltage down to the negative voltage representing the signal "−1". The amplified signal "−1" is transmitted through the data bus to the outside, completing the operation of reading "−1". Due to the discharge of the capacitor to the bit line, the negative charges decrease, and the sense amplifier rewrites the read−out data back to the capacitor, restoring the capacitor's charge state, ensuring that the data is not lost after the reading operation. The row line voltage is then lowered to 0V, turning off the field−effect transistor, and disconnecting the connection between the capacitor and the bit line, as shown in Figure 10.

3) The reading operation of 0 for the ternary DRAM

The specific operation steps are as follows: Firstly, the row address is decoded and the row line are activated. The row decoder selects the required row according to the row address signal (RAS), pulls the row line to a high voltage, turns on the transistor on the row, and connects the capacitor and the bit line. When performing a reading operation of 0, the bit line voltage is pulled to 0V. Since the internal storage state is "0", the capacitor does not carry any charge, so there is no charging or discharging phenomenon in the capacitor, and the bit line voltage does not change significantly. The sense amplifier cannot detect a significant current at this time. At this point, the bit line voltage is pulled to the low level representing the signal "0". The amplified "0" signal is transmitted through the data bus to the outside, completing the operation of reading "0". The row line voltage is then lowered to 0V, the field-effect transistor is turned off, and the connection between the capacitor and the bit line is disconnected, as shown in Figure 10.

8.2 Ternary DRAM Writing Operation

1) The writing operation of +1 for the ternary DRAM

When performing the writing operation of +1, the bit lines are pre-charged to the reference positive voltage as shown in Figure 11. The specific operation steps are as follows: First, the row address is decoded and the row lines are activated. The row decoder selects the required row based on the row address signal (RAS), and pulls the row lines up to a high voltage to make the transistors on that row conductive, connecting the capacitor to the bit line. The data to be written externally, "+1", is transmitted to the bit line through the data line. At this time, the bit line voltage is pulled up to the positive voltage. Due to the conductive transistors, the capacitor is connected to the bit line, and the ungrounded end of the capacitor is charged with positive charges, storing the data "+1". After the capacitor is fully

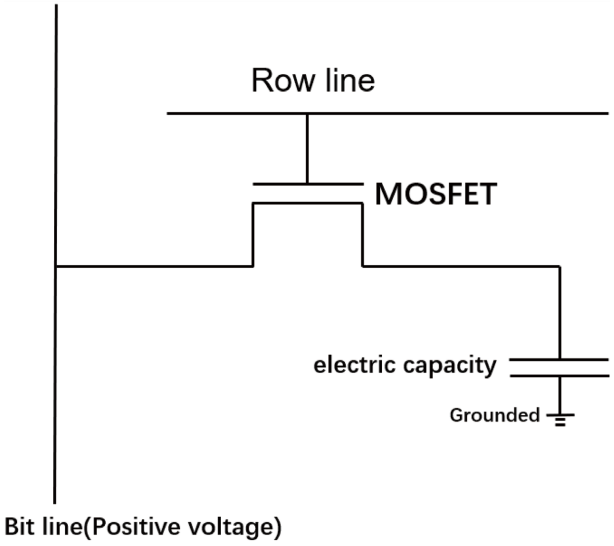

Figure 11. The structure diagram of ternary DRAM for writing +1 operation.

charged, the row line voltage drops to 0V, the transistors are turned off, and the capacitor is disconnected from the bit line. The capacitor retains the current state representing "+1".

2) The writing operation of −1 for the ternary DRAM

When performing the writing operation of −1, the bit lines are pre−charged to the reference negative voltage as shown in Figure 12. The specific operation steps are as follows: First, the row address is decoded and the row lines are activated. The row decoder selects the required row based on the row address signal (RAS), and raises the row lines to a high voltage to make the transistors on that row conductive, connecting the capacitor to the bit line. The external data to be written "-1" is transmitted to the bit line through the data line. At this time, the bit line voltage is pulled down to the negative voltage. Due to the conductive transistors, the capacitor is connected to the bit line, and the ungrounded end of the capacitor is charged with negative charges, storing the data "−1". After the capacitor is fully charged, the row line voltage drops to 0V, the transistors are turned off, and the capacitor is disconnected from the bit line. The capacitor retains the current state representing "−1".

3) The writing operation of 0 for the ternary DRAM

When performing the writing operation of 0, the bit line voltage is pulled to 0V or grounded, as shown in Figure 13. The specific operation steps are as follows: First, the row address is decoded and the row line is activated. The row decoder selects the required row based on the row address signal (RAS), and raises the row line to a high voltage to make the transistors on that row conductive, connecting the capacitor to the bit line. The external data to be written as "0" is transmitted via the data line to the bit line. At this time, the bit line voltage is pulled to 0V. Since the transistors are conductive, the capacitor is connected to the bit line. Regardless of whether the state inside the capacitor is "+1" or "−1", the bit line will

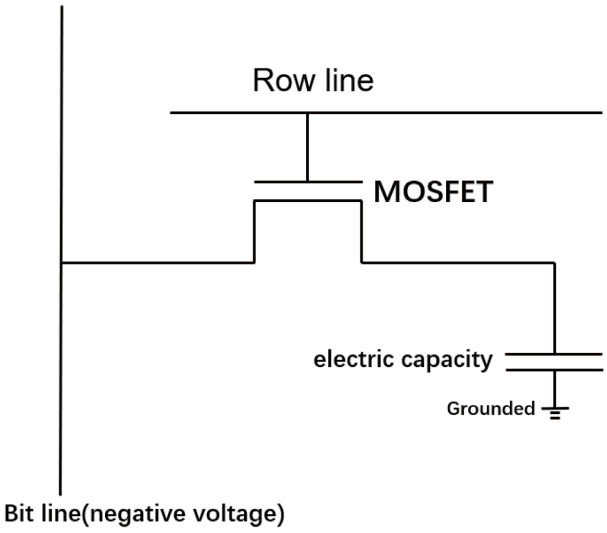

Figure 12. The structure diagram of ternary DRAM for writing -1 operation.

clear the positive or negative charge at the ungrounded end of the capacitor, thereby ensuring that there is no charge in the capacitor, indicating that the written signal is "0". After the capacitor charge is cleared, the row line voltage drops to 0V, the field-effect transistor is turned off, and the connection between the capacitor and the bit line is cut off, allowing the capacitor to retain the charge state representing "0".

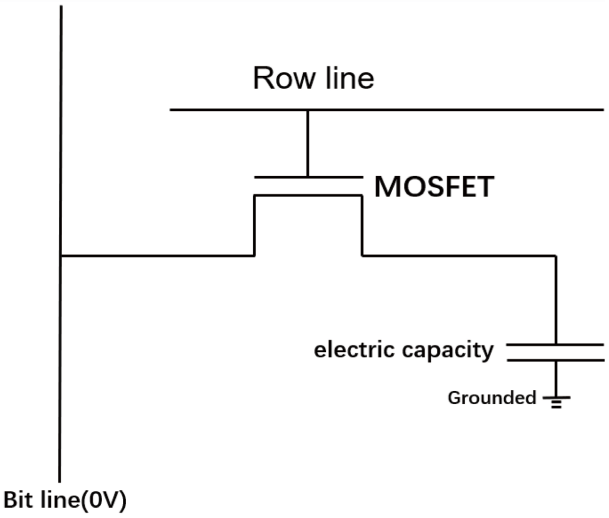

Figure 13. The structure diagram of ternary DRAM for writing 0 operation.

8.3. The Refresh Mechanism of Ternary DRAM.

In a single DRAM memory cell, due to the physical characteristics of the capacitor, the charge will be gradually lost due to the leakage of the transistor or environmental factors, and the data may be lost within several milliseconds. In order to

solve this difficulty, before the charge is completely leaked (usually every 64ms), the capacitor charge will be restored to the correct state by re-reading the internal state and writing back its internal state data. Its refresh mechanism is in the unit of Row.

The external memory controller sends refresh commands periodically, and all rows need to be refreshed within 64 ms. If DRAM has 1000 lines, each line needs to be refreshed every $64\ \text{ms}/1000 \simeq 64\ \mu\text{s}$. First, the refresh controller provides the address of the row to be refreshed, activates the row address strobe signal (RAS), and selects the target row. The bit line is precharged to an intermediate voltage, and the capacitance of the memory cell of the selected row is connected with the bit line. If the state inside the capacitor is +1, the sense amplifier detects a weak forward current. If the state inside the capacitor is −1, the sense amplifier detects a weak reverse current. If the state inside the capacitor is 0, the sense amplifier can't detect any current. This process is the same as the read operation, but it does not output data to the outside. Then the sense amplifier amplifies the detected weak signal, and rewrites the amplified weak signal into the storage capacitor through the bit line to restore its charge to the original state. After the refresh, the bit line is disconnected from the current storage capacitor and precharged to the intermediate voltage to prepare for the next operation.

9. Design of Ternary NAND Flash Memory

The floating gate transistors of ternary NAND flash memory utilize ternary MOSFETs, which employ three N-type semiconductors and two P-type substrates, with insulation isolation between the two P-type substrates. The structural diagram is shown in Figure 14. The right drain D2 is subjected to a relatively high positive voltage, the middle drain D1 to a relatively low positive voltage, and the left source to 0V voltage. The middle drain D1 serves as the signal output terminal. If the signal output terminal detects an upward forward current and converts it into a positive voltage signal after passing through resistor R, it represents the digital signal +1. If the signal output terminal detects a downward reverse current

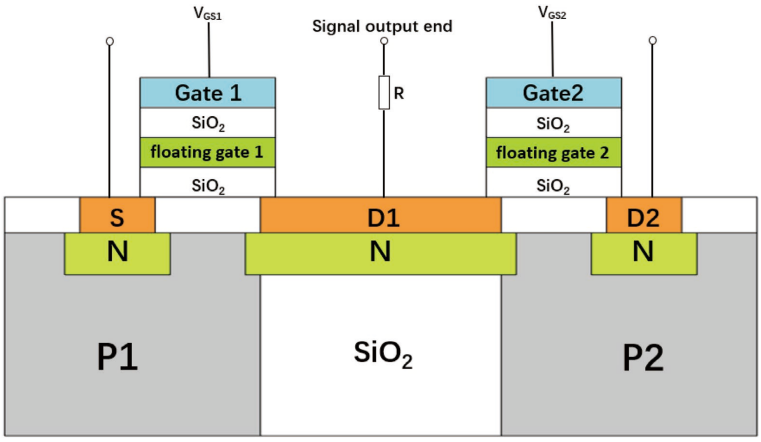

Figure 14. The structure diagram of floating gate transistor of ternary NAND flash memory.

and converts it into a reverse voltage signal after passing through resistor R, it represents the digital signal −1. If the signal output terminal detects no current at all, it represents the digital signal 0.

9.1. Erasing Operation of Floating Gate Transistors for Ternary NAND Flash Memory

1) Erasing operation of −1.

The operation schematic is shown in Figure 15. Firstly, the controller selects the target block and prohibits other operations to ensure data integrity. The substrate P1 is applied with a high voltage, and the word line 1 above the substrate P1 is grounded, that is, the gate 1(G1) does not apply voltage. Electrons tunnel from the floating gate back to the substrate through Fowler-Nordheim tunneling, and the threshold voltage drops to the erase state (assuming that the areas of the left floating gate 1 and the right floating gate 2 have completed the Programming Operation previously). Then, all pages within the block are read. At this time, the signal output terminal detects a downward reverse current, and after passing through the resistor R, it is converted into a reverse voltage signal. At this point, the state is −1. If some units are not erased completely (with residual electrons), the erasure operation needs to be repeated.

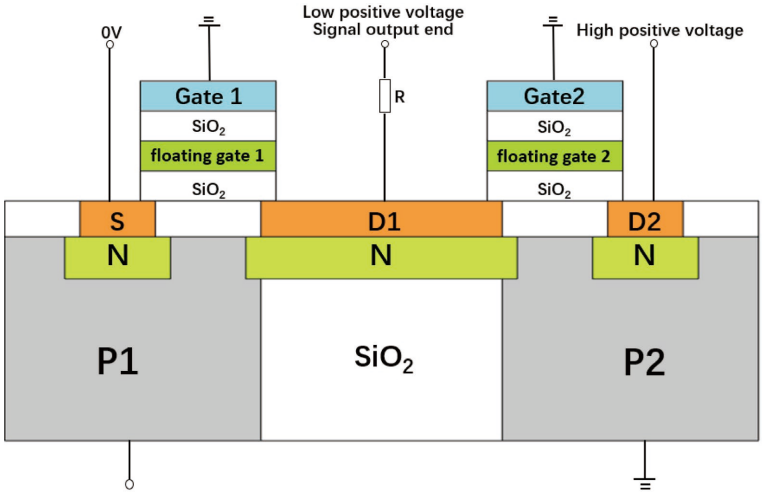

Figure 15. The diagram of −1 erasing operation.

2) Erasing operation of +1.

The operation schematic is shown in Figure 16. Firstly, the controller selects the target block and prohibits other operations to ensure data integrity. The substrate P2 is applied with a high voltage, and the word line 2 above the substrate P2 is grounded, that is, the gate 2(G2) does not apply voltage. Electrons tunnel from the floating gate back to the substrate through Fowler-Nordheim tunneling, and the threshold voltage drops to the erase state (assuming that the areas of the left floating gate 1 and the right floating gate 2 have completed the Programming Operation previously). Then, all pages within the block are read. At this time, the

signal output terminal detects an upward forward current, and after passing through the resistor R, it is converted into a positive voltage signal. At this point, the state is +1. If some units are not fully erased (with residual electrons), the erasure operation needs to be repeated.

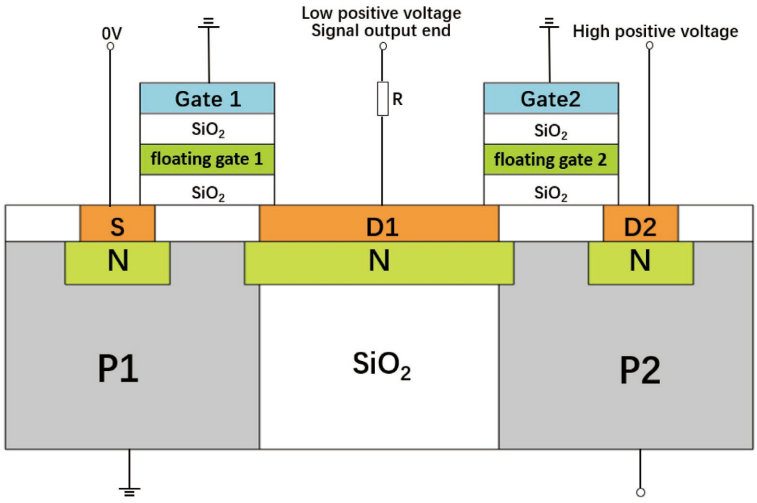

Figure 16. The diagram of +1 erasing operation.

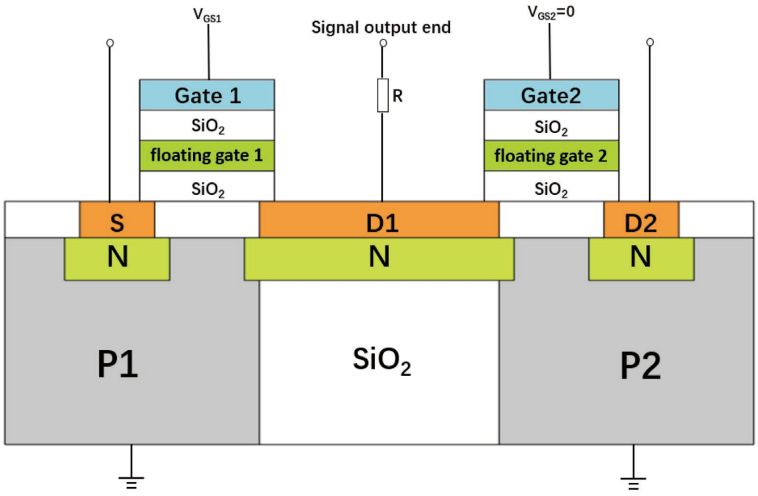

Figure 17. The diagram of programming operation from -1 to 0.

9.2. Programming Operation of Floating Gate Transistor for Ternary NAND Flash Memory

1) Programming operation from −1 to 0.

The operation schematic is shown in Figure 17. Firstly, confirm that the block where the target page is located has been erased. If the block is not erased, the erase operation needs to be performed first. The data is transmitted to the Page Buffer through the I/O interface. The substrate P1 is grounded, and the word line 1 above the substrate P1 is applied with a high voltage, that is, the gate 1 is applied with a high voltage. The electrons tunnel through Fowler-Nordheim from the sub-

strate into the floating gate 1, increasing the threshold voltage, and the MOSFET is turned off. The entire state of the floating gate transistor changes from "−1" to "0".

2) Programming operation from +1 to 0.

The operation schematic is shown in Figure 18. Firstly, confirm that the block where the target page is located has been erased. If the block is not erased, the erase operation needs to be performed first. The data is transmitted to the Page Buffer through the I/O interface. The substrate P2 is grounded, and the word line 2 above the substrate P2 is applied with a high voltage, that is, the gate 2 is applied with a high voltage. The electrons tunnel through Fowler-Nordheim from the substrate into the floating gate 2, increasing the threshold voltage, and the MOSFET is turned off. The entire state of the floating gate transistor changes from "+1" to "0".

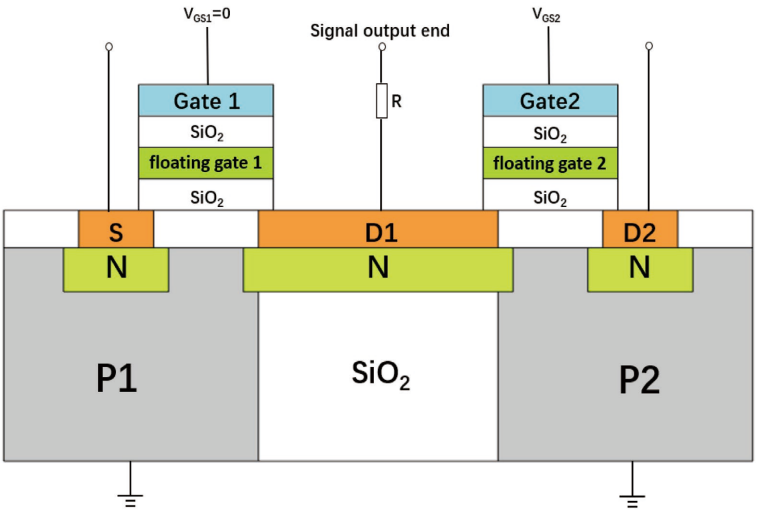

Figure 18. The diagram of programming operation from +1 to 0.

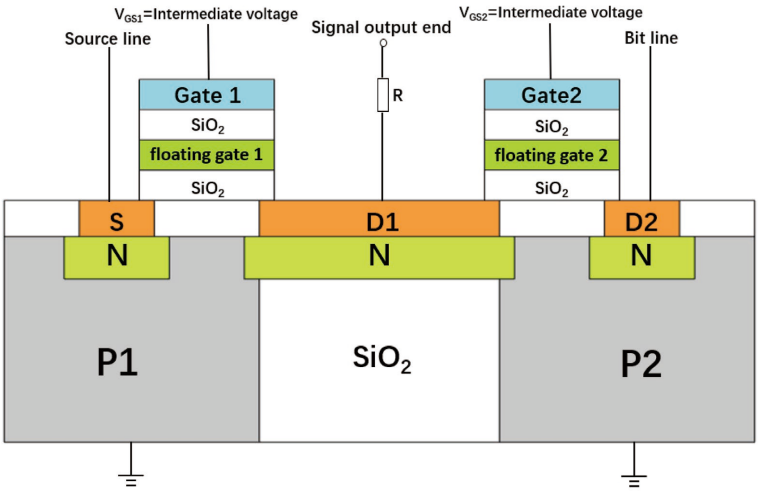

Figure 19. The operation schematic of reading operation of floating gate transistor in ternary NAND flash memory.

9.3. Reading Operation of Floating Gate Transistor for Ternary NAND Flash Memory

The structure diagram is shown in **Figure 19**. Firstly, based on the input address signal, the page to be read is determined. The read voltage is applied to word lines 1 and 2 (usually between the threshold voltage of Programming Operation and the threshold voltage of Erasing Operation), a higher positive voltage is applied to bit lines, a lower positive voltage is applied to the signal output terminal D1, and a 0V voltage is applied to the source line. If the state is +1, the signal output terminal detects an upward forward current, and after passing through resistor R, it is converted into a positive voltage signal. If the state is −1, the signal output terminal detects a downward reverse current, and after passing through resistor R, it is converted into a reverse voltage signal. If the state is 0, no current or voltage is detected at the signal output terminal.

9.4. The Advantages of the Ternary DRAM and NAND Structures

At present, the technology of DRAM and NAND flash memory is based on binary, but the ternary DRAM and NAND flash memory designed in this paper will improve the unit storage density of information to some extent. Because each ternary memory cell can represent three states, while binary can only represent two states. According to Shannon's information theory, the information content of a single ternary unit is $\log_2 3 \simeq 1.58$ bits, which is about 58% higher than that of a binary unit (1 bit). When reading and writing data, the ternary unit can transmit 1.58 bits per operation, while the binary unit can transmit 1 bit. Theoretically, when transmitting the same amount of data, the bus access times of ternary DRAM can be reduced by about $37\%\left(1-1/\log_2 3\right)$, thus reducing the data transmission delay and bus power consumption.

More precisely, if the computer is based on the R-ary system and stores n bits, it can accommodate information bits $N = R^n$. Then the maximum information content of ternary DRAM and NAND flash memory will be increased by $(3/2)^n$ times. If the computer is 16 bits, the maximum information bit of ternary DRAM and NAND flash memory is $(3/2)^{16} = 656$ times. If it is a 64-bit computer, its capacity will increase considerably. Therefore, if the same amount of data is stored, the address space of ternary system can be smaller (because each unit carries more information), thus simplifying the address decoding circuit and saving hardware resources.

If ternary logic is adopted in the future computing system, ternary DRAM and NAND flash memory can directly store and transmit the multi-state data needed for computing, thus avoiding the overhead of converting multivalued data into binary code in binary system, improving the efficiency of integration of storage and computing, and symmetric ternary (−1, 0, +1) is naturally suitable for processing signed or balanced data (such as Ternary Weight Networks in neural networks), reducing the overhead of binary complement conversion.

10. Conclusions

Chips fabricated in a ternary system possess powerful computing capabilities and exponentially increasing storage space. The significance of the transition from binary to ternary is substantial. It not only manifests in the superior energy efficiency and computing power enhancement of Soc or other processor platforms, but also represents a breakthrough in the current bottleneck of AI computing power development. AI is an important technological industry in the international development, but the main obstacle in its development process is that the binary system seriously affects its computing power. The transistors made with a ternary system will enable a breakthrough in the AI computing power bottleneck and may significantly improve the energy efficiency of processor platforms under the same performance. With the decrease in cost and transistor scale, Moore's Law continues to hold. Therefore, the research on ternary systems and ternary computers is very necessary. In this paper, we have respectively designed ternary 0, +1, −1 digital signals using the improved MOSFET and FinFET field-effect transistors. Based on the binary MOSFET and FinFET field-effect transistors, we have added one gate, one drain and one drain-source. When a gate voltage V_{GS1} is applied to gate G1, a downward reverse output current I_{DS1} is generated between the source S and the low-voltage drain D1, representing the digital signal −1. At this time, the gate voltage V_{GS2} is not applied to gate G2. When a gate voltage V_{GS2} is applied to gate G2, an upward forward output current I_{DS2} is generated between the high-voltage drain D2 and D1, representing the digital signal +1. When the gate voltage is not applied to gates G1 and G2, the output current is not generated at the output terminal, representing the digital signal 0. On this basis, we have given the design principle and structure of ternary DRAM memory, that is, the reading +1, −1 and 0, and writing +1, −1 and 0 respectively, and also given NAND flash memory, which include erasing operation, programming operation and reading operation. In addition, the arithmetic and logical operation rules of ternary are given. All the above works will lay a very important foundation for the development of ternary computer.

Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

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