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Simulation Study of Nanoscale FDSOI MOSFET Characteristics

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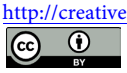


Abstract

Silicon on insulator (SOI) technology permits a good solution to the miniaturization as the MOSFET size scales down. This paper is about to compare the electrical performance of nanoscale FD-SOI MOSFET at various gate lengths. The performance is compared and contrasted with the help of threshold voltage, subthreshold slope, on-state current and leakage current. Interestingly, by decreasing the gate length, the leakage current and on-state current are increased but the threshold voltage is decreased and the sub-threshold slope is degraded. Silvaco two-dimensional simulations are used to analyze the performance of the proposed structures.

Keywords

Fully Depleted, Silicon on Insulator, Threshold Voltage, Subthreshold Slope, Leakage Current, Gate Length

1. Introduction

The intense evolution of information technology (IT), electronics and communications industry is possible because of the continuous advancement in silicon based MOS technology. This continuous advancement has been maintained with a decrease in device density and chip area without sacrificing the electrical performance. The price of the device has been reduced continuously. It enhances economic productivity with new generation of technology.

In addition to its downscaling, the device properties such as high input resistance, fast switching, low output resistance and low power dissipation have made MOS transistors as the principal elements of the current integrated circuits (ICs). Today MOS ICs are absolutely necessary in our life ranging from compact electronics to communication systems [1] [2].

The problems associated with current MOS technology are its Vth roll-off, sub-threshold swing, off-state leakage current, drain-induced barrier lowering, parasitic resistances and capacitances that severely hamper the performance of these devices [3] [4]. Due to the mentioned effects conventional deeply scaled MOSFETs have limited subthreshold swing, high Ioff and reduced Ion/Ioff ratio. Reduction in Ioff is essential to reduce power dissipation and for low leakage currents. Amplification and maximum output voltage swing are important parameters for MOS transistors [5]. Higher drive current and frequency response is another issue in the design of current CMOS technology. The floating body effects (FBEs) and body potential effect should also be considered while designing any MOS transistor [6]. To conquer these issues, the new device technology has been proposed by several engineers such as Junctionless MOS transistors, Fully depleted (FD) and Partially depleted (PD) Silicon-on-Insulator (SOI) MOSFETs, multigate MOSFETs (FinFET) etc. [7] [8] [9]. Of these devices, FD-SOI MOSFETs has been regarded as a promising substitute to bulk MOS transistors in the scheme of digital ICs [8] [9] [10]. In this paper, electrical characteristics such as threshold voltage, subthreshold slope, on-state current and leakage current of FD-SOI MOSFET structure have been investigated. The proposed structure has been simulated and studied using Silvaco TCAD device simulator.

2. Methodology

To study the electrical parameters of FD SOI MOSFET a schematic cross-sectional view of the SOI MOSFET is simulated using Silvaco TCAD device simulator, is shown in **Figure 1**. Lombardi CVT mobility model, bandgap narrowing model, Shockley-Read-Hall recombination and impact ionization model from Selberherr [11] are used for the simulation. Newton methods is used for Numeric methods. We assumed n channel device and simulated the device for different gate length of FD SOI MOSFET.

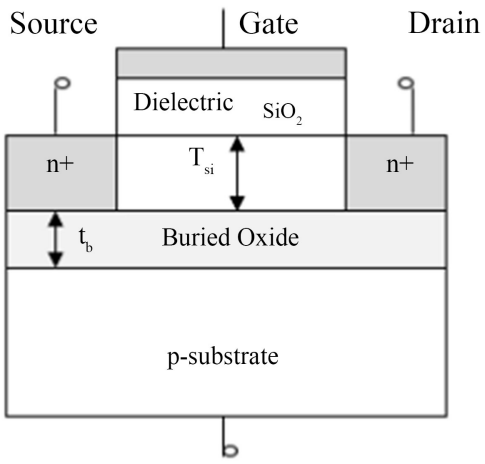


Figure 1. Schematic view of FD-SOI MOSFET.

3. Results and Discussion

The simulation and investigation of electrical parameters of n-channel FDSOI has been carried out by using Silvaco TCAD simulation software. Atlas syntax is used to create the FD SOI structures and TonyPlot is used to display the simulation results. In this study, n-channel FDSOI MOSFET structure has been designed and simulated using DeckBuild.

In Table 1 device structure of FD SOI n-MOSFET at different gate length is shown.

By changing the gate length, the electrical parameters of SOI MOSFET are recorded as shown in Table 2. The results in Table 2 are analysed and graph of electrical characteristics versus gate length are plotted.

Figures 2(a)-(d) show the Ids/Vgs characteristics of FDSOI at various gate lengths. As gate length increases from 25 nm to 100 nm, threshold voltage increases from 0.0192157 V to 0.144959 V. With technology scaling, smaller value of threshold voltage is needed to satisfy high performance of device [12]. A low threshold voltage and steeper sub-threshold slope allows MOSFET to switch rapidly [13].

By varying the gate length, the result of threshold voltage has been recorded and the graph of threshold voltage versus gate length is plotted and shown in Figure 3. From Figure 3, it can be said that the smaller the gate length, the lower the threshold voltage.

A high subthreshold value indicates that the device responses slowly when switching from off to on state. The graph of subthreshold slope versus gate length is shown in Figure 4. As gate length increases, the steeper subthreshold slope becomes as from Figure 4 which is responsible for high speed of device.

Table 1. Device structure of FD SOI n-MOSFET at different gate length.

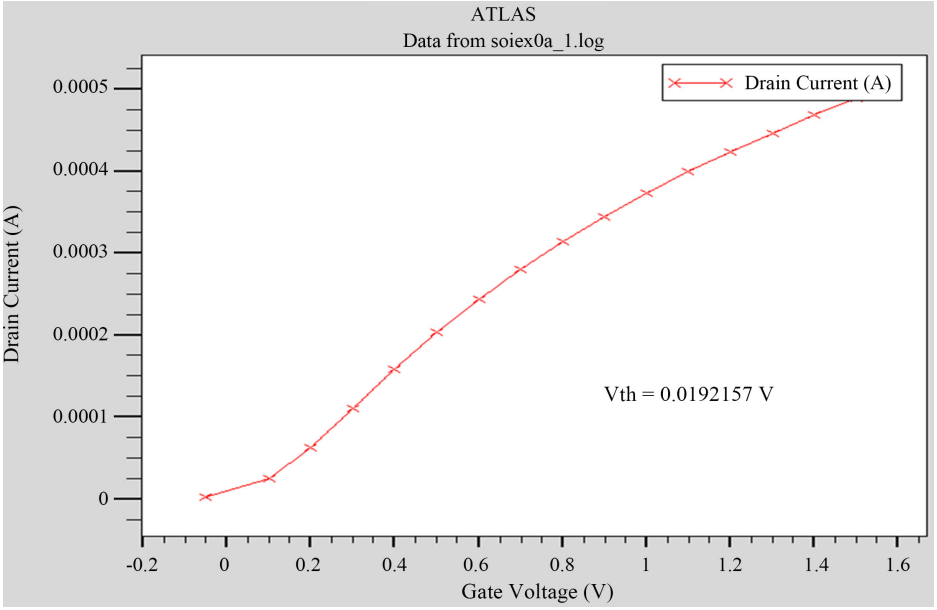
Gate Length L_{gate} (nm)	Oxide Thickness t_{OX} (nm)	Source/Drain Length $L_{S/D} = L_{gate}$ (nm)	Silicon Layer Thickness $t_{si} = 0.4L_{gate}$ (nm)	BOX Thickness t_{BOX} (nm)	Source/Drain Doping Concentration N_D (m^{-3})	Channel Doping Concentration N_A (m^{-3})
25	2	25	10	50	1×10^{21}	3×10^{18}
60	2	60	24	80	1×10^{20}	1×10^{18}
80	2	80	32	100	1×10^{20}	1×10^{18}
100	2	100	40	140	1×10^{19}	1×10^{18}

Table 2. Electrical characteristics of FD SOI n-MOSFET at different gate length.

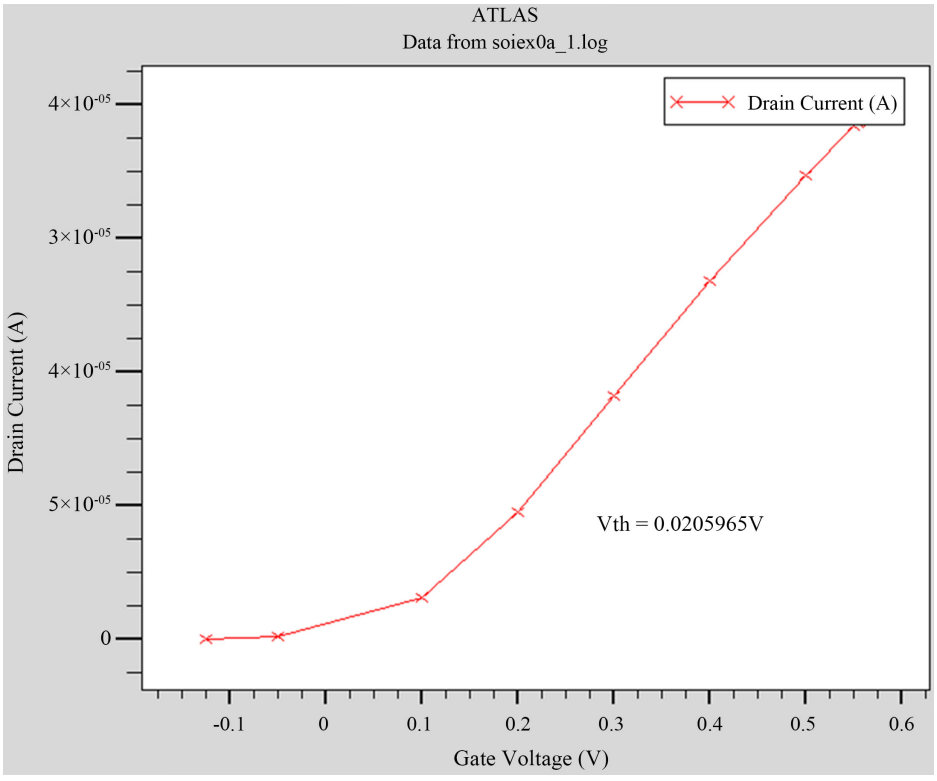
Gate Length L_{gate} (nm)	Threshold Voltage, Vth (V)	Subthreshold slope (mV/dec)	On-state current, I_{on} (A)	Leakage current, I_{off} (μA)
25	0.0192157	151.544	0.00357	219.98
60	0.0205965	98.6043	0.00113	3.67
80	0.091869	73.484	0.00088	0.39
100	0.144959	69.6673	0.00057	0.031

Figures 5(a)-(d) show the subthreshold slope of FDSOI at various gate lengths. As gate length increases from 25 nm to 100 nm, subthreshold slope improves from 151.544 mV/dec to 69.6673 mV/dec.

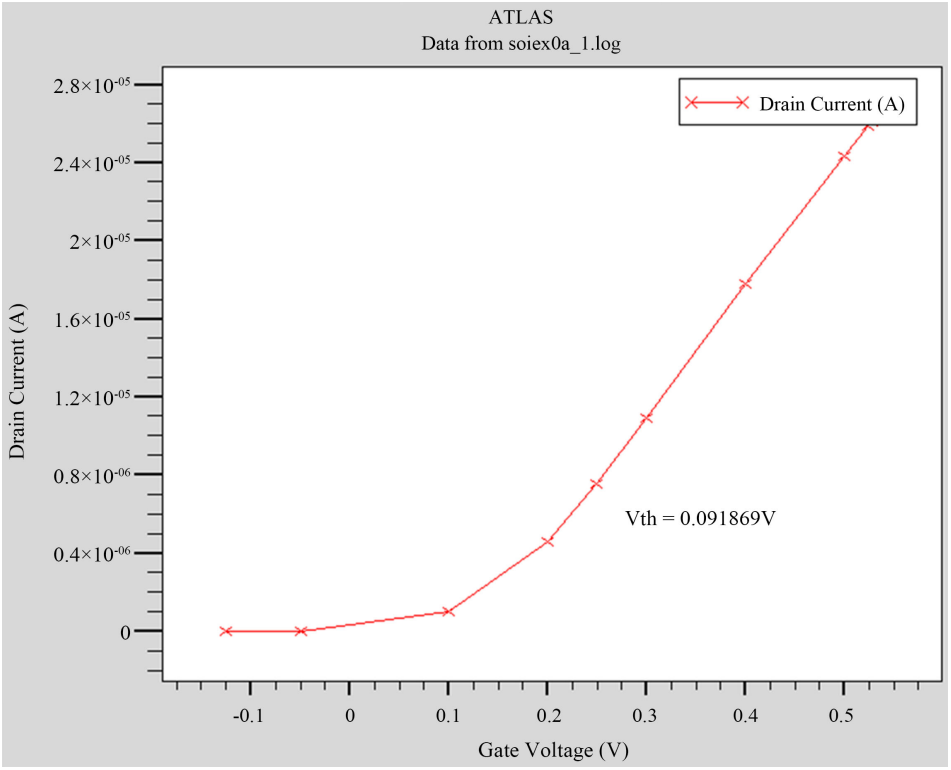
The device achieves high speed if it has a high on-state current (I_{on}). The graph of I_{on} versus gate length is shown in Figure 6. From Figure 6, it can be said that the smaller the gate length, the higher the on-state current.



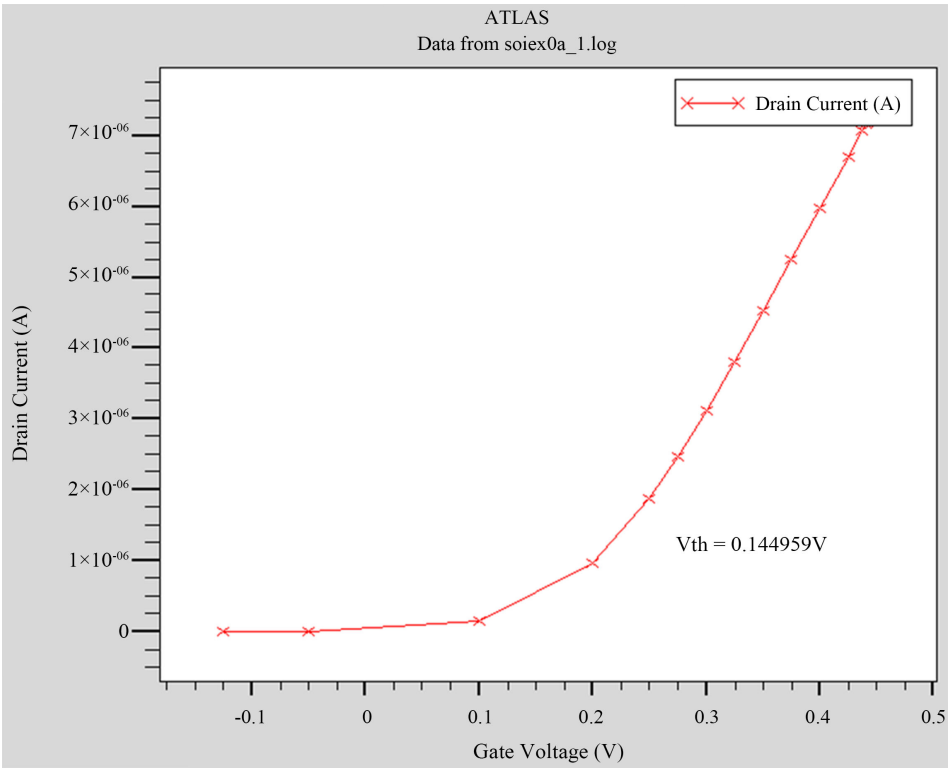
(a)



(b)



(c)



(d)

Figure 2. (a) Ids/Vgs characteristics of FD SOI n-MOSFET of L_{gate} = 25 nm; (b) Ids/Vgs characteristics of FD SOI n-MOSFET of L_{gate} = 60 nm; (c) Ids/Vgs characteristics of FDSOI n-MOSFET of L_{gate} = 80 nm; (d) Ids/Vgs characteristics of FD SOI n-MOSFET of L_{gate} = 100 nm.

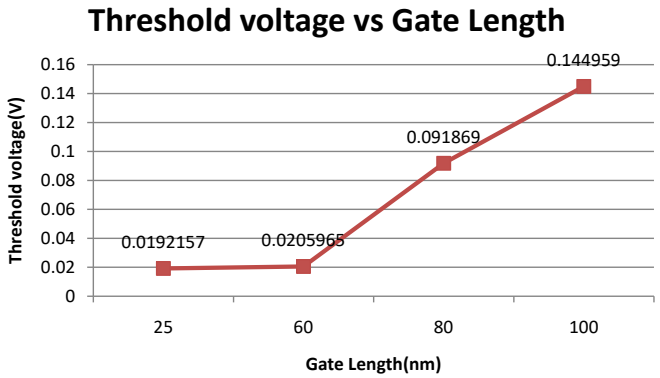


Figure 3. Graph of threshold voltage versus gate length of FD SOI n-MOSFET.

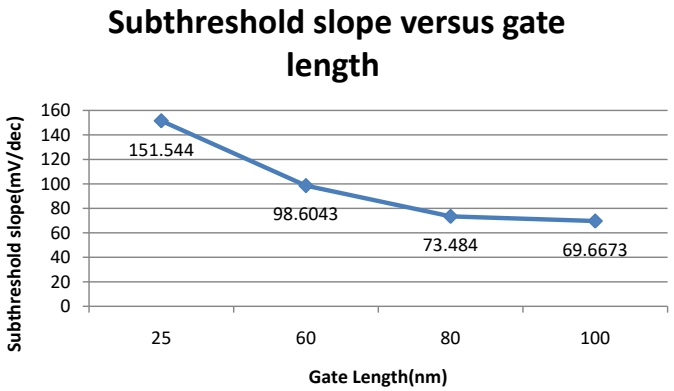
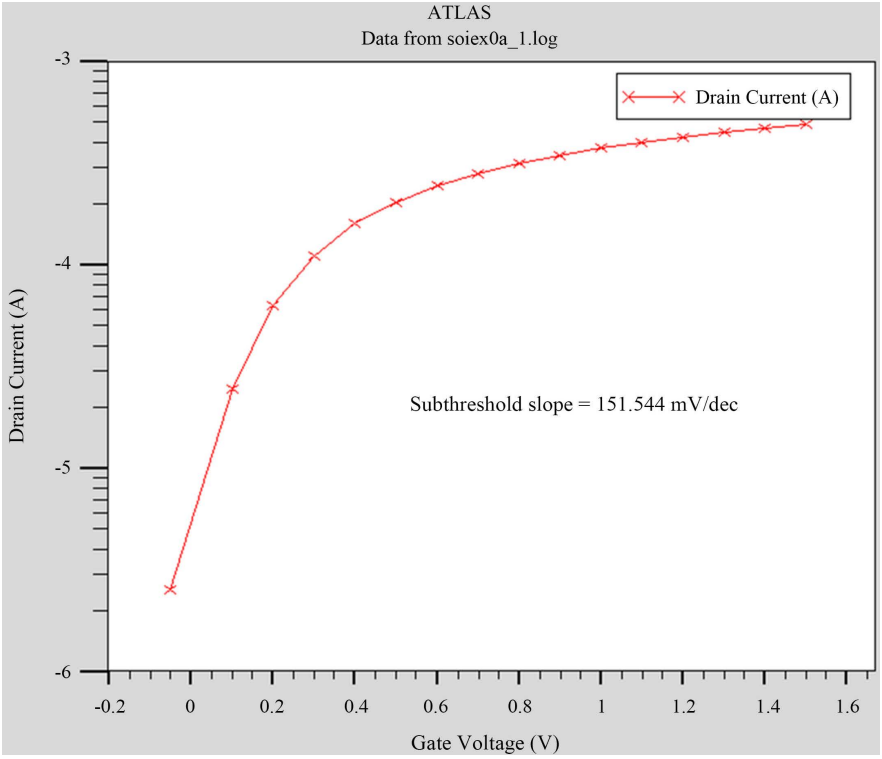
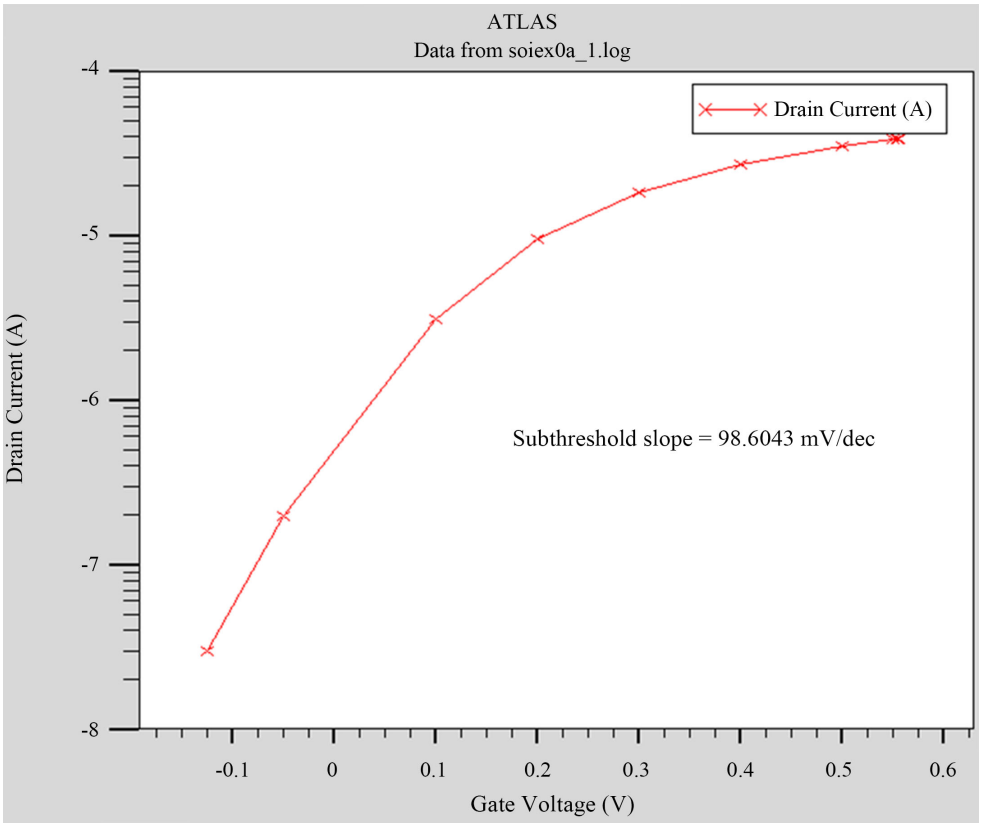


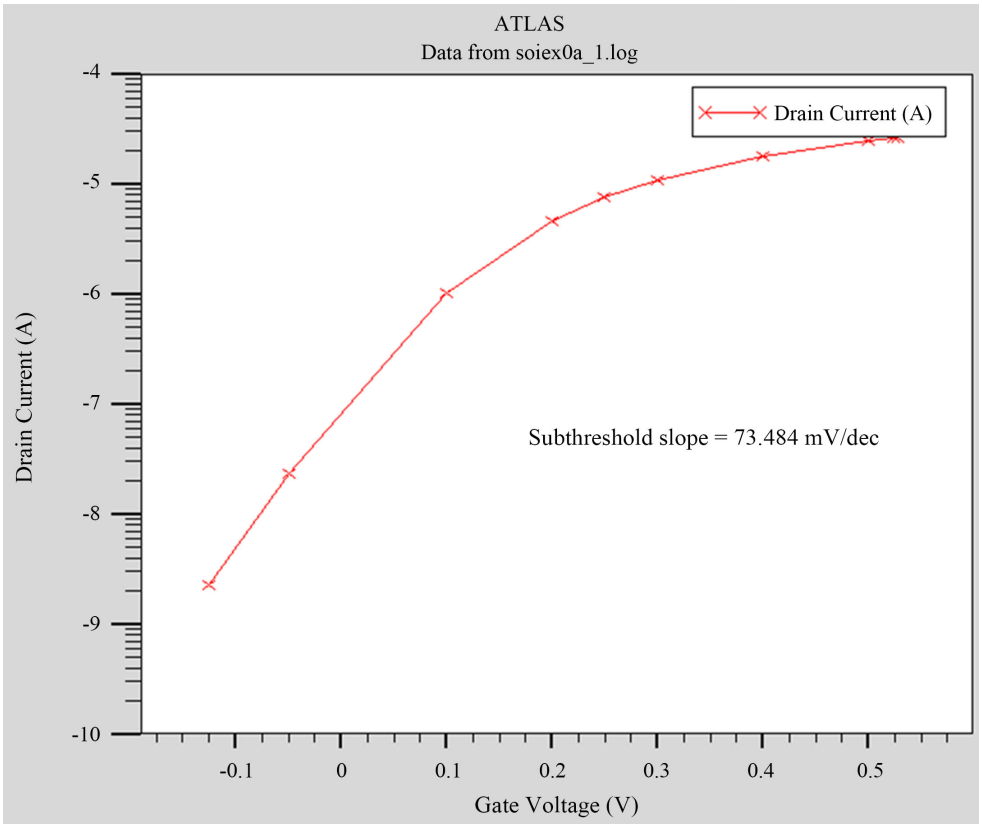
Figure 4. Graph of sub threshold slope versus gate length of FD SOI n-MOSFET.



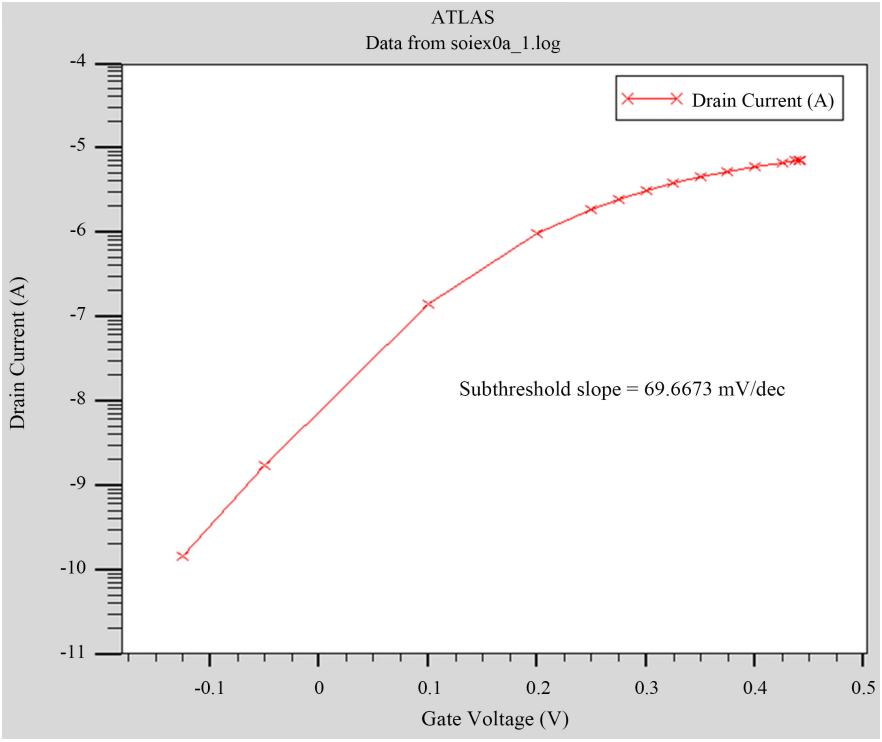
(a)


ATLAS
Data from soiex0a_1.log
Drain Current (A)
Subthreshold slope = 98.6043 mV/dec
Drain Current (A)
Gate Voltage (V)
-4
-5
-6
-7
-8
-0.1
0
0.1
0.2
0.3
0.4
0.5
0.6

(b)


ATLAS
Data from soiex0a_1.log
Drain Current (A)
Subthreshold slope = 73.484 mV/dec
Drain Current (A)
Gate Voltage (V)
-4
-5
-6
-7
-8
-9
-10
-0.1
0
0.1
0.2
0.3
0.4
0.5

(c)



(d)

Figure 5. (a). Subthreshold slope of FDSOI n-MOSFET of L_{gate} = 25 nm; (b). Subthreshold slope of FDSOI n-MOSFET of L_{gate} = 60 nm; (c). Subthreshold slope of FDSOI n-MOSFET of L_{gate} = 80 nm; (d). Subthreshold slope of FDSOI n-MOSFET of L_{gate} = 100 nm.

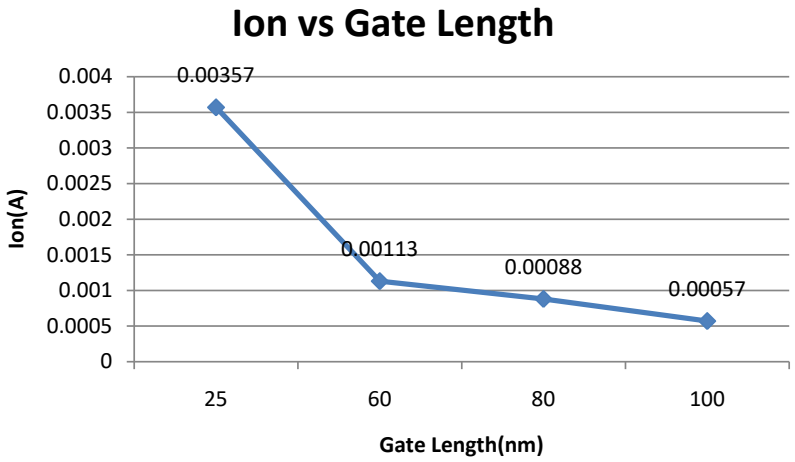


Figure 6. Graph of I_{on} versus gate length of FD SOI n-MOSFET.

The value of threshold voltage and leakage current (I_{off}) is inversely related [14]. So high value of threshold voltage results in low value of leakage current. If leakage current crosses a limit MOSFET device fails. The graph of leakage current versus gate length is shown in **Figure 7**. From **Figure 7** as gate length increases, leakage current decreases. Static power dissipation is caused by leakage current. When input transition is absent, static power dissipation is resulted by current flow[15]. So static power dissipation will be smaller if leakage current value is

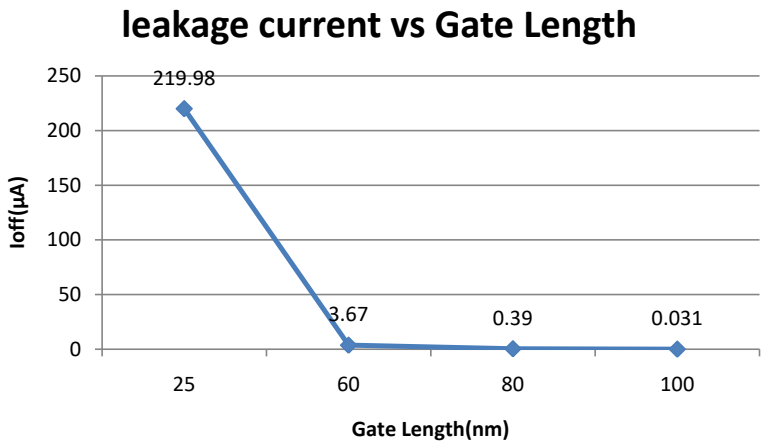


Figure 7. Graph of leakage current versus gate length of FD SOI n-MOSFET.

lower. Thus, from the result the FD SOI with higher gate length will have static power dissipation of lower value.

4. Conclusion

Nanoscale FDSOI has been investigated in terms of electrical characteristics using Silvaco T-CAD Simulator. It is found that the threshold voltage decreased with decrease in gate length. So the device can be used for low power application. The subthreshold slope is degraded and on-state current increased with decrease in gate length which determines the device speed. The leakage current decreases with increase in gate length which results in decrease in static power dissipation. So depending on application the gate length and device structure of FD SOI should be chosen.

Conflicts of Interest

The author declares no conflicts of interest regarding the publication of this paper.

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