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Research on Multi-System Ultra-High Speed Optical Signal Access System

Yao Bai, Zhiping Huang, Yong Ding

College of Artificial Intelligence, National University of Defense Technology, Changsha, China
Email: huangzhiping65@nudt.edu.cn

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Abstract

In view of the small transmission capacity and single signal modulation format of the existing optical transmission system, this paper proposes an ultra-high-speed optical signal access scheme based on NEL0670, which can realize the transmission of 100 G DP-QPSK, 200 G DP-16QAM and 400 G DP-16QAM signals, and realize flexible and intelligent reception of multi-system optical signals.

Keywords

Optical Communication, High-Speed Signal, Field Programmable Array

1. Introduction

With the popularization of new multimedia technologies such as network high-definition television, video on demand, IPTV, etc., the demand for network traffic and network bandwidth is increasing day by day. In 2002, British research scholars proposed a system communication design with a transmission rate of 100 Gbps and a modulation code of DQPSK [1]. In 2004, R. Noe studied how to lock the initial phase of the local oscillator signal and the input signal to simplify the coherent optical communication transmission system. In 2007, Coreoptics first implemented a coherent optical communication system with a DP-QPSK modulation pattern transmission distance of 1600 at a transmission rate of 100 Gbps. In 2010, American AT & T Company announced that it successfully tested the first single-carrier 100 Gbps DP-QPSK real-time coherent optical communication system, and achieved the first 1800 km transmission on site. Now, 100 G coherent optical communication system has begun to be commercialized [2]. However, the existing coherent optical transmission system can only transmit signals with a single modulation format of 100 G, which cannot meet the bearing

requirements of massive high-rate services. In order to increase the network communication capacity to a greater extent, this paper proposes a dual-channel 100 Gb/s coherent detection system, which can realize the transmission of 100 G, 200 G and 400 G optical signals.

2. Overall Design

The overall hardware structure of the coherent detection platform is shown in **Figure 1**. The 128 G ultra-high-speed optical signal on the line side passes through the polarization beam splitter (PBS) and becomes two single-polarized optical signals, which are mixed with the local oscillator light emitted by the local oscillator light source (LO) at 90 degrees in the mixer, and then Into electrical signals. The electrical signal is then sampled and quantized by an ultra-high-speed ADC. The signal is converted from an analog electrical signal to a digital electrical signal. Because the signal is damaged during transmission, the signal is compensated and calibrated in the DSP. The recovered signal is output to the interface. Because NEL0629 can output 100 G DP-QPSK signals or 200 G DP-16 QAM signals, the entire system can realize the transmission of 100 G, 200 G, 400 G signals.

As can be seen from **Figure 1**, the main components of the entire coherent detection platform are: coordinated laser (ITLA), integrated coherent optical receiver (ICR), high-speed digital signal processor (DSP) and FPGA.

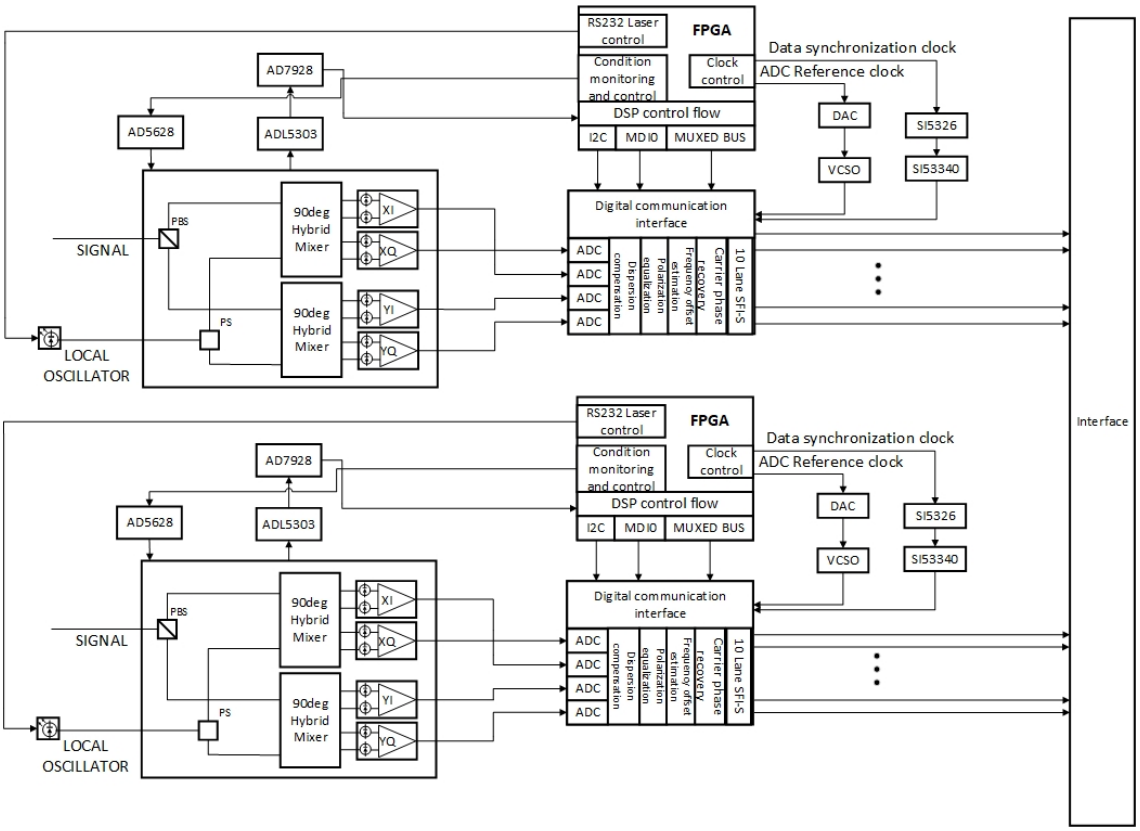

Figure 1. Overall hardware structure diagram.

3. Core Components of the Hardware Platform

3.1. Photoelectric Conversion Module

The role of the tunable laser (ITLA) in digital coherent detection is to provide local oscillator light (LO) to receive coherently with the light on the line side. During this process, the linewidth of the laser has a significant impact on performance [3]. ITLA follows the OIF specification, including pin definitions and the definition of various functions of internal registers, which greatly facilitates the selection and replacement of ITLA by designers. This article selects EM core's TTX1994ITLA, the laser has a line width of up to 100 kHz, and very low intensity noise (RIN). In the actual application process, ITLA uses RS232 serial port to communicate with the controller. The integrated coherent optical receiver (ICR) mainly realizes the mixing of signal light and local oscillator light. ICR also follows the OIF specification, and this article selects UICR.

3.2. Digital Signal Processing Module

The maturity of digital signal processing technology allows people to process digital signals at the receiving and sending ends of optical communications through relevant algorithms of digital processing technology, thereby overcoming various problems caused by the transmission process, such as dispersion and nonlinear effects These technological advancements have brought a qualitative leap for the development of optical signal coherent detection technology. At present, Clariphy, NEL, Acacia and other companies have launched commercial 100 G dedicated DSP chips. This article selects the NEL0670 chip from NEL. NEL0670 is suitable for digital coherent transmission systems of various modulation formats, such as 100 G DP-QPSK and 200GDP-16 QAM signals, with a wide range of applications.

3.3. Clock Module

The clock circuit is equivalent to the "heart" of the entire module and is the source of power for the operation of each logic function module [4]. If the "heart" can continue to beat smoothly and forcefully, it will provide a stable and reliable working foundation for the entire module, so the importance is evident. The clock requirements of the coherent detection platform are relatively complex and can be divided into two major categories. One is the low-speed clock, which is mainly used for auxiliary circuits around the core device. Not very sensitive; the other is high-speed clocks, mainly clocks related to data processing. These clocks have very high requirements on frequency and accuracy, and clock jitter is also required at femtosecond level.

3.4. Control Module

The entire coherent detection module is controlled by field programmable gate array (FPGA) [5]. At present, most of the international FPGA chip market is occupied by the products of Xilinx and Altera, mainly because of its strong

comprehensive strength. It can be said that the two have their own characteristics in terms of product model and software development environment, which is no different. This design will use Altera's FPGA chips. Because the design is only for control and normal signal processing, and does not involve high-speed data processing, it is enough to choose low-end FPGA products. The design chooses Cyclone series chips, the specific model is 5CEFA9U19.

3.5. Power Module

The power supply is the most basic and critical part of the coherent detection platform, and it is the prerequisite for ensuring the normal and stable operation of other hardware [6]. When designing the power system, power consumption, heat dissipation and other issues must be considered first, because the circuit board area of the coherent detection module is limited, and space allocation must also be considered.

4. Clock Module Design

The clock requirements of the coherent detection module are shown in **Table 1**. The low-speed clock can be divided and output by the internal PLL of the FPGA. This article mainly designs the high-speed clock.

4.1. RF ADC Clock Design

As can be seen from **Figure 2**, this is an adaptive closed-loop control structure. The adaptive equalization module (AEQ) inside the DSP compares the reference clock of the ADC, calculates the error between the current clock signal and the reference clock signal, and adjusts the adaptive equalization module (the filter

Table 1. Clock requirements of the coherent receiving module.

Classification	Use	Frequency requirements	Accuracy requirements
1. Low speed clock	1. Low-speed ADC, DAC, various auxiliary circuits	Less than 100 MHz	Lower
2. High-speed clock	2. RF ADC clock	0.993 GHz	Less than 50 femtoseconds
	3. DSP TX clock	698.81 MHz	Less than 100 femtoseconds
	4. DSP RX clock	698.81 MHz	Less than 100 femtoseconds

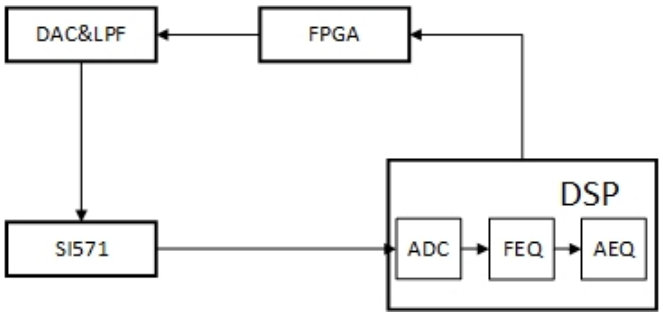

Figure 2. ADC reference clock functional block diagram.

coefficient of the AEQ) according to the value Control, iterate repeatedly and finally reach a balance. During this process, if the input clock does not meet the frequency and phase requirements, the DSP will send out a serial code to instruct the external device to adjust the clock signal. After receiving the adjustment signal, the FPGA sends the data to the DAC after format conversion. After receiving the voltage control data, the DAC chip generates the corresponding control voltage and controls the VCSO to output the clock signal corresponding to the frequency. The clock signal then enters the ADC to provide the reference clock, and the DSP will compare it again, make adaptive adjustments, and repeat the above steps until the clock is locked to 0.993 GHz.

This module selects the SI571 clock chip from Silicon Labs to provide the clock for the system. SI571 is an oscillator with a programmable output frequency. Through the operation of the I2C interface, a device can generate any output frequency from 10 MHz to 1.4 GHz. The rms jitter amplitude is reduced to about 0.3 ps.

4.2. Special DSP Chip RXO Side Clock Design

As can be seen from **Figure 3**, the RXOREF clock is directly provided by the interface, and the RXOGEN clock is generated by the clock chip SI5326, which is a precision clock multiplier for jitter attenuation. It is suitable for applications that require high jitter performance. When the input clock frequency of the chip is from 2 kHz to 710 MHz, two output clocks in the range of 2 kHz to 945 MHz are simultaneously generated to meet the needs of this system.

5. Power System Design

The clock requirements of the coherent detection module are shown in **Table 1**. The low-speed clock can be divided and output by the internal PLL of the FPGA. This article mainly designs the high-speed clock.

It can be seen from **Figure 4** that the power requirements of the coherent detection platform are relatively complex. In order to facilitate device selection and procurement, the power modules selected in this paper are all from LINAR's LTM series power switches and LTC series linear regulated power supplies. The power architecture is shown in **Figure 4**.

For the analog power supply, a linear regulated power supply (LDO) is used

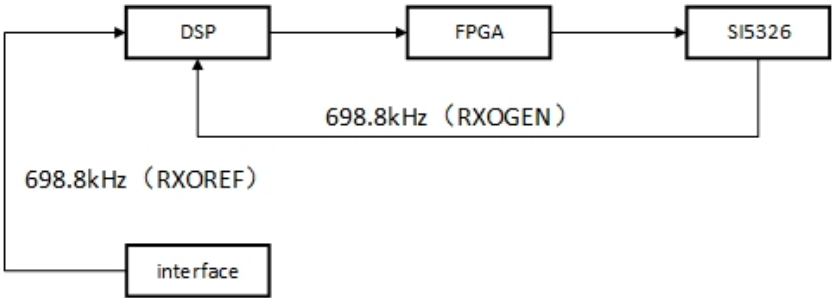

Figure 3. RXO reference clock functional block diagram.

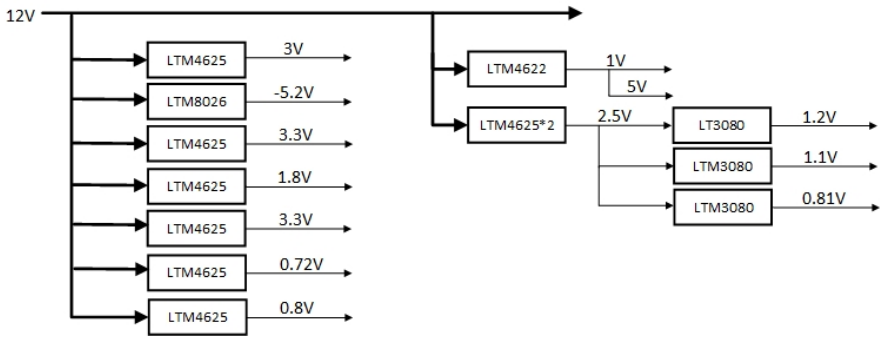

Figure 4. Power structure.

for design. Since the input current and output current of the linear regulated power supply are basically the same, the voltage drop from the input end to the output end causes energy loss, so it should be minimized. Voltage drop improves power supply efficiency and reduces energy loss. For this purpose, two-stage power supply can be used. Switching power supply is selected for the first stage power supply, which can maintain high energy conversion rate while realizing high voltage drop, and second stage selects linear regulated power supply to obtain corresponding analog voltage.

6. Conclusion

This paper proposes a dual-channel 100 Gb/s OTN signal access method. Using the characteristics of the NEL0670 chip, two signals are arranged on a board to achieve 100 G, 200 G and 400 G transmission, which solves the existing optical transmission. The system has a small transmission capacity and a single modulation format. The article details the framework and core components of the dual 100 Gb/s optical signal transmission system, and focuses on the design process of the clock and power supply test. The test results show that the system can normally transmit 100 G, 200 G and 400 G signals, which lays the foundation for the subsequent work of related processing equipment.

Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

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