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Optimizing Factory Performance for Unit Cost in Semiconductor Manufacturing

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Abstract

The integrated circuit (IC) manufacturing process is capital intensive and complex. The production process of unit product (or die, as it is commonly referred to) takes several weeks. Semiconductor factories (fabs) continuously attempt to improve their productivity, as measured in output and cycle time (or mean flow time). The conflicting objective of producing maximum units at minimal production cycle time and at the highest quality, as measured by die yield, is discussed in this paper. The inter-related effects are characterized, and a model is proposed to address this multi-objective function. We then show that, with this model, die cost can be optimized for any given operating conditions of a fab. A numerical example is provided to illustrate the practicality of the model and the proposed optimization method.

Keywords

Semiconductor Manufacturing, Cycle Time, Die Cost, Unit Cost, Yield, Optimization, Productivity

1. Introduction

The integrated circuit (IC) manufacturing process is highly capital intensive and complex. It takes a few weeks to fabricate a wafer in a typical semiconductor factory because of the length of the manufacturing process and its complexity. A breakdown of wafer cost by financial elements is shown in [1] where the data illustrates the capital-intensive nature of semiconductor manufacturing. Depreciation on equipment represents 32% of the wafer cost. The process itself is long and complex, typically comprising of hundreds of process steps with manufacturability restrictions such as queue time windows that inevitably increase the production cycle time. As explained in [2], queue time windows are restrictions

imposed on the process to control the quality, as measured in yield and level of defects, by ensuring that wafers go through a series of sequential sensitive steps in a pre-defined flow time. However, such restrictions come at the price of increased production cycle time and reduced equipment utilization and productivity—see for example [3] or [4].

The reduction of production cycle times for faster delivery of products to market has become increasingly important in the last two decades across many industries, including the semiconductor industry. As stated by [5], cycle time is an equally important component of manufacturing performance because it enables semiconductor manufacturers to increase output quickly. Moreover, the "clock-speed" of new product development is now a well-accepted measure for any high-tech industry [6] and it is highly impacted by production cycle time.

Numerous papers have been published on the importance of cycle time. For example, a discussion on the importance of cycle time and quality in the software industry can be found in [7]; in [8], they do the same in the context of MRP-based assembly facilities; and in [9] a proposal of a stochastic model for determining the production cycle time for serial production in the metal processing industry is discussed; lastly, in [10] the focus on cycle time improvements for a photolithography process in semiconductor manufacturing.

When attempting to reduce cycle time, the inherent conflict between equipment utilization and its productivity and quality must be considered since they all affect cycle time in different ways. Per the fundamental law named after John Little [11], which simply refers to steady state cycle time in queuing systems, the cycle time (CT) is linearly correlated with work-in-progress (WIP), given that the manufacturing system is in steady-state. Therefore, as WIP goes up so is CT. In line with Little's Law, the well-known operating curve (see [12] [13]) implies a relationship between volume (of input or output) and CT. The operating curve is shown in **Figure 1**.

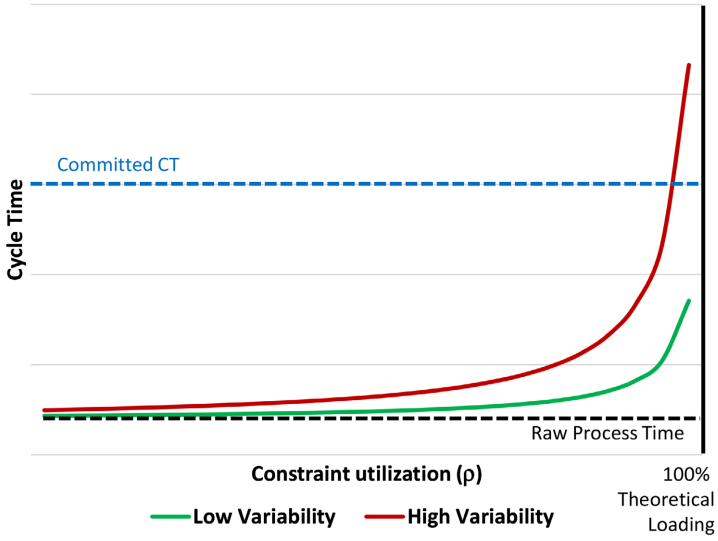

Figure 1. The operating curve (based on G/G/m queuing model).

The operating curve, which emerges from basic queuing theory, suggests that as production volume increases towards the factory capacity (determined by its actual constraints), CT increases exponentially. The nature of the increase in CT, as depicted by the shape of the curve, is dependent on the factory characteristics, especially variability in equipment availability and WIP/operational policies.

On the other hand, the pioneering work of Wein [14] on the relationship between yield and CT in semiconductor wafer fabrication, has shown that in order to improve output there is a need to increase the amount of WIP as well, then each lot in the process would have to wait longer in queues and therefore yield would deteriorate. Wein has shown that there is an optimal solution for production start rate of raw material for maximum good output (*i.e.*, non-defective).

In Wein's model a key component has been left out, and that is cost. In considering the best operating conditions for a semiconductor fab, not only CT and yield must be considered for maximum output. Output itself must be considered for optimal cost. Therefore, the incorporation of CT, yield, and output is needed with respect to cost, and ultimately unit cost. In this paper, we extend the previous works made in the area of semiconductor manufacturing operational performance optimization and integrate all the relevant components in a unified framework. A model is developed to address this multi-parametric function and derive the unit (die) cost optimized fab operating conditions. A numerical example is provided to illustrate the practicality of the proposed model.

This paper is organized as follows. A literature review of related work is included in the next section. In Section 3, notation, problem description and derivation of the fundamental formulae of the proposed model are given. Section 4 contains insights and a solution approach to the problem, followed by a numerical example. Summary and conclusions are in Section 5.

2. Literature Review

The relationships and trade-offs between yield and CT has been a topic for occasional research over the past two decades since the pioneering work by [14]. Cunningham and Shanthikumar [15] provide empirical results on the relationship between Die Yield (DY) and CT in semiconductor wafer fabrication. They examine the hypothesis that long cycle times cause low die yields owing to the extended exposure to particles and environmental damage in the fab by using data from four high volume production facilities. They conclude that there is some evidence for the association of yield and CT but the correlations that they observed at the time were not strong. Up-to-date correlations, considering the increased sensitivity of the current manufacturing processes in advanced tech nodes, are provided in this paper.

Tirkel *et al.* [16] tackle the aspect of relationships between CT and yield as affected by in-line metrology inspections of production lots. They focus on single operation monitors and investigate their sampling rate and scheduling. They apply dynamic policies for metrology inspections via simulation and analytical

methods. Their results show that most of the policies present a concave curve of yield versus CT, implying that there is an optimal inspection rate for maximum yield.

Similar to the research on relationships between yield and CT, some work can also be found also with respect to the relationships between yield and cost and between yield and output loss. van Roijen *et al.* [2] show a curve for the trade-off between yield and output, depicting capacity (output) loss as a function of the number of wafers allowed within a queue time in a segment of the process flow. Pileggi *et al.* [17] emphasize that yield loss occurs not only due to manufacturing defects and reliability faults, but also as higher performance is pursued and, therefore, IC design and manufacturing can be made more cost-affordable by removing some design for performance limitations. Weber [18] proposes a model for identifying the high-leverage variables associated with yield improvement, given that the cost of learning is enormous before the yield ramp, in order to improve overall profitability. But profitability or cost are not considered within a quantitative objective function framework. A more quantitative cost-oriented approach is taken in dealing with specific problems such as for lot scrapping decisions of small lots in low yield high price scenario by Wu *et al.* [19] or for the evaluation of three-dimensional integrated circuit (3D IC) cost-efficient design by Dong and Xie [20]. Lastly, an optimization framework is presented in [21] for yield improvement and test cost reduction for 3D ICs. Two yield improvement schemes are covered: wafer matching and layer redundancy.

In the broader context, optimization in manufacturing has been discussed extensively in the literature. Aranoff [22] proposes a model for manufacturing and production economics with demand and cost curves. His analysis also utilizes curves for optimization. However, the demand and cost curves introduced there are different than the CT and output curves used in this work. Another example is by [23]. They employ a mathematical model to derive the optimal manufacturing batch size for a vendor-buyer integrated economic production quantity with scrap. Lastly, global optimization is of essence in problems with multiple criteria. Ozan *et al.* [24] have recently proposed a novel approach based on Reinforcement Learning (RL) for finding global optimum. Yet, in all the work to-date, from Wein's model incorporating CT and yield to the work of recent years on cost and optimized manufacturing via advanced techniques of RL, a unified model that considers all major aspects of manufacturing—CT, yield, and output—altogether for optimized cost, and ultimately unit cost, has not been developed. In this paper, such a model is presented in order to close this gap.

3. Problem Statement

The problem at hand can be stated as follows: what are the operating conditions for a fab in terms of CT and WIP (and consequently capacity, yield and output) that produce optimal unit (die) cost?

Relationships between these various components are known and will be formulated within an optimization framework.

The following notation is used throughout the paper:

Variables:

CT: Mean cycle time in days for a wafer in the fab.

RPT: Raw Process Time, the fastest (lowest) CT possible.

WIP: Amount of work-in-progress.

WSE: Wafer starts equivalent, a measure of fab output rate.

DY: Average die yield in die per wafer.

WC: Wafer cost in dollars.

TC: Total cost, including fixed and variable costs.

DC: Die cost in dollars.

Constants:

K_i: calibrating constants

$\mathrm{WSE}_{\min}$: minimal WSE, corresponding to the minimum WIP in the system.

$\mathrm{WSE}_{\max}$: maximal WSE, corresponding to maximum WIP in the system.

Y_b, Y_w, CT_b, CT_w = best/worst die yield values, corresponding to best/worst CT values.

Typically, output rate by each tool-group in a fab is measured using a "Wafer Starts Equivalent" (WSE) indicator. This is done in order to account for the re-entrant process over multiple different tool-groups. WSE for fab is simply a measure of average output across all tool-groups in terms of wafer starts into the fab. It is highly dependent on the amount of WIP in the fab and its distribution across the tool-groups. In general, as WIP increases so is the WSE, because more opportunities exist for running more efficiently at each tool-group, processing larger batches and cascades. That is true so long as the increase in WIP has not reached a peak from which any additional WIP would not be useful for more output. A proper function that represents the behavior of WSE as a function of WIP can be prescribed as follows:

$$\mathrm{WSE} = \mathrm{WSE}_{\min} + \left(\mathrm{WSE}_{\max} - \mathrm{WSE}_{\min}\right) \cdot \left(1 - \mathrm{e}^{-K_1 \cdot \mathrm{CT}}\right) \tag{1}$$

This is a monotonically increasing function that reaches an asymptotic value, in line with the explanation above for the nature of WSE.

The DY in current advanced technology nodes has been found to be approximately linearly inverse-correlated with CT. Supporting data for this argument is given in **Figure 2**, based on recent data collection from a real fab of fully processed production lots over a long period of high-volume manufacturing. This relationship between DY and CT can be expressed as follows:

$$\mathrm{DY} = Y_w + \frac{Y_b - Y_w}{\mathrm{CT}_w - \mathrm{CT}_b} \cdot \left(\mathrm{CT}_w - \mathrm{CT}\right) \tag{2}$$

Equation (2) approximates the relationship as an inverse linear correlation. For a more accurate approximation, a polynomial regression may be fitted but, for the simplicity of the optimization in this paper, it is kept as a first order approximation.

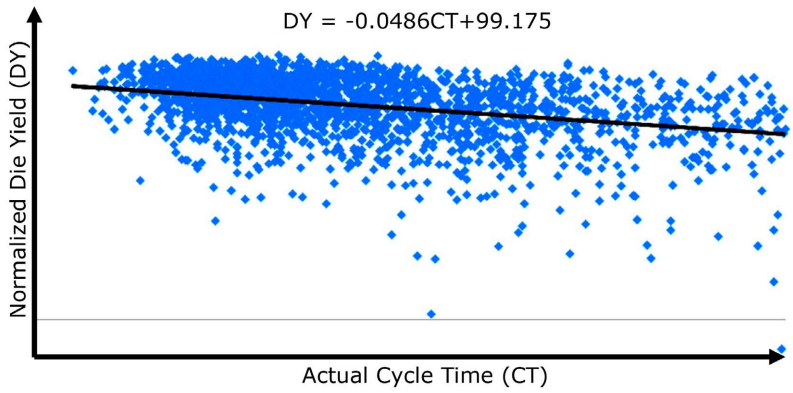

Figure 2. Die Yield (DY) as a function of Cycle Time (CT).

The cost per die (unit) is calculated by dividing the total cost per wafer by the number of good die per wafer (*i.e.*, by the die yield). The total cost per wafer equals to the total cost, fixed and variable, divided by the average amount of wafers produced, *i.e.*, by WSE.

$$\mathrm{DC} = \frac{\mathrm{TC}}{\mathrm{WSE} \cdot \mathrm{DY}} \tag{3}$$

The numerator in Equation (3) is the total cost, measured in dollars. The denominator is the multiplication of wafers produced by good die per wafer which gives total good die produced, making the result be the average die cost. Note that from (1) and (2), both WSE and DY, which are in the denominator of (3) are a function of CT. Hence, by prescribing them in (3), we get die cost as a function of CT as well.

$$\mathrm{DC} = \frac{\mathrm{TC}}{\left[\mathrm{WSE}_{\min} + \left(\mathrm{WSE}_{\max} - \mathrm{WSE}_{\min}\right) \cdot \left(1 - \mathrm{e}^{-K_1 \cdot \mathrm{CT}}\right)\right] \cdot \left[Y_w + \frac{Y_b - Y_w}{\mathrm{CT}_w - \mathrm{CT}_b} \cdot \left(\mathrm{CT}_w - \mathrm{CT}\right)\right]} \tag{4}$$

Note that DC can be viewed as a multiplication of the two inverse functions of WSE and DY. It is straightforward to show that the inverse WSE is a monotonically decreasing convex function and the inverse DY is monotonically increasing convex function. This makes it difficult to determine conditions upon which the result is a strictly convex function with a global unique minimum. Nevertheless, finding the optimal solution is easy via simple (binary) search over the continuous CT values.

Before we continue to discuss solutions and a numerical example to this problem, we shall illustrate the problem via two schematic charts which highlight subsequent emerging questions. **Figure 3** illustrates why this is an optimization problem. It highlights the possibility that while a fab may be running at relatively large CT in order to get maximum output on the equipment and from the fab, this also results in a lower DY and consequently the unit (die) cost is very high.

On the other hand, if the fab attempts to run close to the theoretical Raw Process Time (RPT) it may be that too much compromise is needed on output

such that, again, the die cost ends-up very high. Hence the operating points of maximum output or of minimum CT may not be the optimal operating points for optimal die cost. However, if the fab slightly reduces the loading and thus compromises some of the output, this can lead to an overall better die cost.

Figure 4 highlights a different aspect of the problem. When considering tool reductions for the sake of capital productivity, how should a tool be selected for reduction? Traditionally, the criterion has been to release any tool with excess capacity to the required volume. But we postulate that it may not be best to do so since the reduced WSE behaves differently on the DC objective function than the current WSE, *i.e.* tool reductions should be considered for reduction based on their impacts on CT and consequently on DC, rather than just on capacity. As shown in Figure 4, as WSE gets lower, TC gets lower (per potential capital/expense savings), thus a new WSE curve emerges (different equipment-base). Hence, the true question becomes as follows: For the new WSE, is CT lower or higher than original and how does this affect DC?

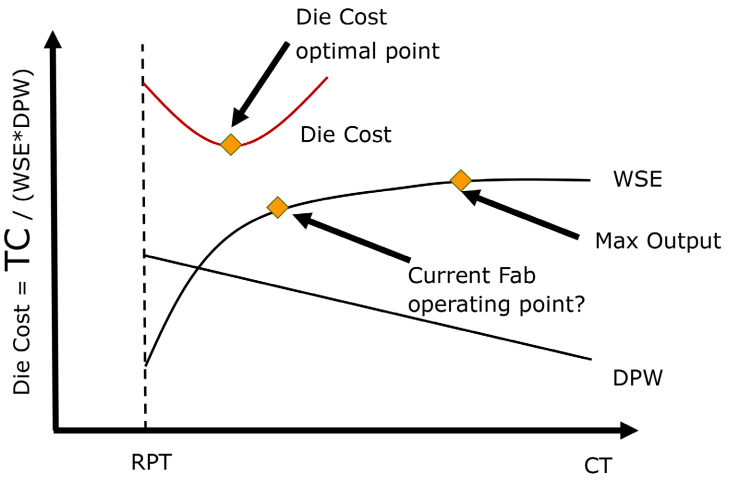

Figure 3. Die Yield (DY) as a function of Cycle Time (CT).

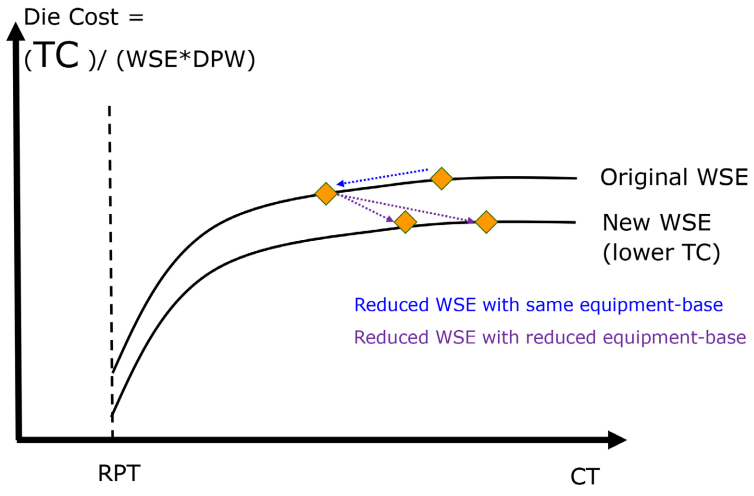

Figure 4. Effects of reduced WSE on die cost.

4. Solution Approach and Numerical Example

In the previous section, DC is formulated as a function of CT in Equation (4). It turns out that despite the fact that DC appears to be convex in our experiments with actual data, it cannot be proven in general. We show that next by taking the second derivative of DC. For brevity, the following notation shall be used for the constants in the equations:

$$A = Y_w + \frac{Y_b - Y_w}{\mathrm{CT}_w - \mathrm{CT}_b} \cdot \mathrm{CT}_w, \quad B = \frac{Y_b - Y_w}{\mathrm{CT}_w - \mathrm{CT}_b} \tag{5}$$

The second derivative of DC is as follows:

$$\begin{aligned} \frac{\partial^2 \mathrm{DC}}{\partial(\mathrm{CT})^2} = & \frac{2B^2 \cdot \mathrm{TC}}{(A - B \cdot \mathrm{CT})^3 \left(\mathrm{WSE}_{\max} - \mathrm{WSE}_{\max} \cdot \mathrm{e}^{-K_1 \cdot \mathrm{CT}}\right)} \\ & + \frac{2 \cdot \mathrm{TC} \cdot k_1^2 \cdot \mathrm{WSE}_{\max}^2 \cdot \mathrm{e}^{-2K_1 \cdot \mathrm{CT}}}{(A - B \cdot \mathrm{CT})\left(\mathrm{WSE}_{\max} - \mathrm{WSE}_{\max} \cdot \mathrm{e}^{-K_1 \cdot \mathrm{CT}}\right)^3} \\ & + \frac{\mathrm{TC} \cdot k_1^2 \cdot \mathrm{WSE}_{\max} \cdot \mathrm{e}^{-K_1 \cdot \mathrm{CT}}}{(A - B \cdot \mathrm{CT})\left(\mathrm{WSE}_{\max} - \mathrm{WSE}_{\max} \cdot \mathrm{e}^{-K_1 \cdot \mathrm{CT}}\right)^2} \\ & - \frac{2B \cdot \mathrm{TC} \cdot k_1 \cdot \mathrm{WSE}_{\max} \cdot \mathrm{e}^{-K_1 \cdot \mathrm{CT}}}{(A - B \cdot \mathrm{CT})^2 \left(\mathrm{WSE}_{\max} - \mathrm{WSE}_{\max} \cdot \mathrm{e}^{-K_1 \cdot \mathrm{CT}}\right)^2} \end{aligned} \tag{6}$$

Given that the original functions were positive in the domain, it can be noted that while the first three elements of the second derivative are also positive in the domain, the last element is strictly negative, thereby making the entire second derivative require certain assumptions on the relationships between the parameters in order to declare convexity of the entire DC function.

But, as indicated earlier, this is no obstacle to obtaining the optimal solution for the problem since even without a closed form expression for the optimal solution it can be easily attained via a search over the CT values.

Next, we demonstrate how to obtain an optimal solution via a numerical example. Table 1 contains data of the operating curve for a fab with a given equipment base (and subsequently TC). The fab is limited to WSE of up to 7650 wafers [per period, e.g., a week] as indicated by the maximum WSE in the table and this is achieved with a CT of 55 days. When lower WSE is introduced, CT becomes lower accordingly and DY improves as well, as indicated by the Die Per Wafer (DPW). The DPW is multiplied by a factor of 10 in order to be in scale with the WSE for the graphical representation of the problem.

In Figure 5, the DC function is depicted in this case along with the WSE and DPW functions. As can be observed, the optimal DC is attained for a CT of 40 days at a value of $1.46. Any change in the CT relative to 40 days would result in a higher die cost. For example, running faster at 35 days improves DPW by 3.1% but requires WSE to be lower by 6.7%, resulting in an overall DC that is higher by 3.9%. Similarly, an attempt to increase output by moving to the right with a higher WSE and a CT of 45 days would indeed improve the WSE by 0.7% but degrade the DPW by 3.1%, resulting again in an overall DC that is higher by 2.5%.

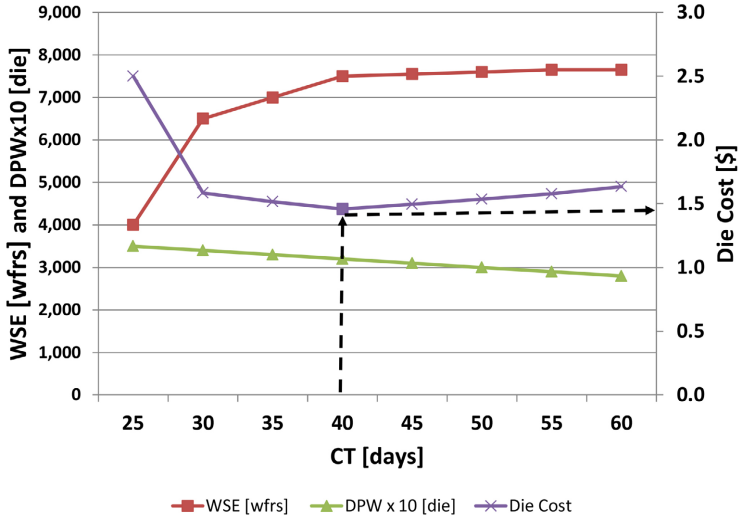

Figure 5. Results of a numerical example.

Table 1. Data for numerical example.

CT [d]	WSE [wfrs]	DPW × 10 [die]
25	4000	3500
30	6500	3400
35	7000	3300
40	7500	3200
45	7550	3100
50	7600	3000
55	7650	2900
60	7650	2800

5. Solution Approach and Numerical Example

In this paper, we have proposed a unified framework for the consideration of output, yield and cycle time for optimized die (or unit) cost. It has been demonstrated that the ultimate measure of die cost can be linked directly to cycle time through the relationships between cycle time, output, and yield. For the sake of simplicity, we assumed an inverse linear relationship between die yield and cycle time. Surely, a more accurate relationship can be fitted and utilized, and this constitutes one direction for further work. Another direction for further work is to incorporate Average Selling Price (ASP) curves for the output in die units, which are a function of supply and demand, within the model. This will of course alter the objective function from being a cost objective to being a profit objective.

Conflicts of Interest

The author declares no conflicts of interest regarding the publication of this paper.

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