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Literature Review of Electronic Packaging Technology and Residual Stress

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Abstract

The rapid development of the electronic information industry brings to the irreplaceable role of electronic components, therefore the search of a more reliable packaging material has become increasingly important. In the electronic packaging system, the failure phenomenon caused by residual stress is one of the key factors restricting the development of electronic packaging technology. In order to use the *in-situ* characterization technology to explore the residual stress inducing mechanism and failure mechanism of epoxy-based advanced packaging materials, this paper gives a review of related previous research, and lays a theoretical foundation for the upcoming research. The classification and generation mechanism of residual stress are clarified in this paper, which provides data support for future related research.

Keywords

Electronic Packaging Material, Residual Stress, Epoxy, Failure Mechanisms

1. Introduction

The semiconductor industry is the most competitive and rapidly developing sector in today's high-tech industries. Semiconductor products find extensive applications in fields such as satellite communication, new energy vehicles, computers, and healthcare, making them crucial for the national economy and defense security [1].

Packaging emerged with the development of integrated circuit (IC) manufacturing technology. During the era of vacuum tubes, there was no concept of packaging, and the method of assembling electronic tubes onto bases to create circuit devices was known as "electronic assembly or assembly". Starting from the 1950s, with the inventions of the germanium and silicon integrated circuits by Jack Kilby and Robert Noyce respectively, the semiconductor industry has

been progressing in accordance with Moore's Law, striving for smaller, faster, and more reliable devices [2].

Packaging refers to the use of membrane technology and micro-fabrication techniques to arrange chips and other components on a frame or substrate, affix them, and establish connections. Wire terminals are encapsulated and fixed within a plastic insulating material. The core of the semiconductor industry is integrated circuits, where the realization of IC chip functionality relies on packaging to form semiconductor devices. Effective IC packaging facilitates the supply of electrical power, signal transmission, and provides thermal pathways, structural support, and protection for the components.

The role of electronic packaging includes: 1) Mechanical Protection: Electronic packaging structures offer reliable mechanical protection for chips and other components, enabling them to withstand various environmental challenges and conditions, ensuring the proper functioning of the devices. 2) Signal Distribution: To minimize signal delay, it is essential to reduce the interconnect distance between the chip and I/O pins during the layout. Proper routing is also needed to mitigate issues like signal crosstalk, especially for high-frequency signals. 3) Thermal Dissipation: Virtually all electronic packaging structures need to address heat dissipation concerns during prolonged operation. Different packaging types and material combinations have varying thermal dissipation effects. For high-power devices, additional measures like heatsinks or cooling methods such as air or liquid cooling may be considered to ensure the system operates within the required temperature range [3].

The fundamental principles driving the development of packaging technology are to enhance signal transmission speed, achieve higher integration levels to accommodate the demands of large chips, improve heat dissipation capabilities, reduce device dimensions, and lower packaging costs, all while ensuring reliability [4].

The idealized microelectronics packaging would involve the creation and packaging of an entire system or subsystem on a single silicon wafer, followed by the cutting of individual devices. However, in the current state of the industry, the process typically involves slicing silicon wafers into individual chips, packaging each chip separately, conducting relevant reliability testing, and then assembling them into a system. The electronics industry classifies packaging into four hierarchical levels based on different fabrication processes, flows, and system structures [5] [6] [7].

The first level of packaging, also known as chip-level packaging, involves connecting the integrated circuit chip to a substrate, affixing and forming a complete device, and conducting a series of performance and reliability tests to ensure the quality of the integrated circuit. The second level of packaging involves assembling multiple devices that have undergone the first-level packaging and other electronic components onto a printed circuit board to create an electronic card. The third level of packaging involves plugging multiple individually packaged single chips from the second level onto a circuit board, turning them

into a subsystem or complete component. The fourth level of packaging refers to assembling several subsystems into a complete electronic product.

2. Development of Electronic Packaging Technology

Electronic packaging technology has been in development for several decades. Its primary purpose is to systematically arrange the various components that constitute electronic devices, bond them, and establish connections according to specific requirements while isolating them from the external environment. To prevent the internal circuits of chips from being corroded by impurities in the air and affecting their electrical performance, it is necessary to isolate the chips from the external environment. Additionally, properly packaged chips are easier to store and transport. Therefore, electronic packaging plays a crucial role in ensuring the integrity and functionality of chips.

The development trends in electronic packaging technology primarily manifest in the following two aspects: 1) The Proliferation and Advancement of BGA Packaging Technology: BGA, or Ball Grid Array packaging, features input/output terminals in the form of solder balls arranged in an array. When dealing with a higher number of I/O ports, BGA packaging becomes necessary [8]. An analysis of BGA packaging reveals that it not only accommodates multiple I/O ports but can also be used for Multi-Chip Module (MCM) packaging by incorporating passive components on the substrate and packaging multiple ICs on the same substrate. When flip-chip technology is applied during the packaging process, it eliminates the need for wire bonding, thereby effectively increasing packaging speed and reducing complexity. According to investigations by relevant departments in China's electronics industry, the global production value of BGA packaging reached $10.5 billion in 2013, showing a 12.2% year-on-year growth. However, BGA packaging remains less prevalent due to its relatively high cost. Therefore, it is essential to intensify research efforts in BGA packaging technology. This can be achieved by exploring and optimizing each step of the packaging process, ultimately reducing packaging costs and expanding its applications, making this packaging technology widely applicable in the electronic packaging industry. 2) Focusing on 3D Packaging Technology: Development is centered around 3D packaging, green packaging, and packaging reliability testing. Building on the foundation of 3D packaging, it extends research efforts into LED packaging, packaging materials, and packaging equipment. This is accomplished with major initiatives, guided by industry demand to drive packaging technology research and promote industrial outcomes, thereby achieving technological innovation in packaging and testing industries. Research efforts are heightened in key System-in-Package (SiP) technologies to expedite research on ultra-thin chip packaging and fine pitch packaging. Additionally, 3D Dynamic Random-Access Memory (3D-DRAM) packaging is incorporated into the development plan for electronic packaging technology. This involves stacking multiple DRAM core chips with Through-Silicon via (TSV) technology, enhancing chip power per-

formance and data transfer rates. Through support for TSV and 3D-SiP technology development, the industrialization of electronic packaging technology is realized.

3. Residual Stress in Electronic Packaging

Various manufacturing processes, such as casting, cutting, welding, heat treatment, assembly, and others, can introduce varying degrees of residual stress within components. Residual stress has a significant impact on the physical and mechanical properties of materials and can pose a substantial threat to the structural integrity. Furthermore, as materials science continues to advance, electronic packaging technology evolves, and the variety of electronic packaging types expands, the quality and performance of packaging materials continue to improve. Residual stresses present in electronic packaging materials have a notable influence on the overall device performance, bond strength, thermal cycling resistance, corrosion resistance, fatigue strength, and other properties. This makes residual stress a significant factor leading to packaging failure. Therefore, researching and detecting residual stress in packaging materials is of great importance for both production and scientific experimentation.

3.1. Classification of Residual Stress

Residual stress is stress that exists within an object when there is no external force acting on it [9] [10]. When no stress is transmitted from the object's surface to its interior, the stress system that maintains internal equilibrium is referred to as internal stress, inherent stress, or initial stress. Residual stress is a type of internal stress.

The classification of internal stress can vary depending on material properties, production conditions, and other factors. One common way to classify internal stress is based on the range of its effects, which can be broadly categorized into two classes: 1) Macroscopic Internal Stress: Also known as residual stress (referred to as the first type of internal stress), it is distributed at the macroscopic scale. Its magnitude, direction, and characteristics can be measured using standard physical or mechanical methods. 2) Microscopic Internal Stress: This type of stress falls within the microscopic range and can be further divided into two subcategories based on its range of effect. One is microstructural stress, also known as the second type of internal stress, it is distributed within the range of individual grains or microstructural components. The other is intragranular substructural stress, also known as the third type of internal stress, it operates within the boundaries of a single grain, affecting the internal substructures of the grain.

These classifications help in understanding the nature and extent of internal stresses, which are of great importance in various fields, including materials science, engineering, and manufacturing, as they can impact the performance and integrity of materials and components.

3.2. Causes of Macroscopic Residual Stress

Residual stress, also known as macroscopic internal stress, can be categorized into three main types based on their origins [11]:

1) Residual Stress from Non-Uniform Plastic Deformation:

Materials often undergo non-uniform plastic deformation due to processing, resulting in different parts of the material experiencing varying degrees of plastic deformation. This non-uniform plastic deformation leads to relative compression or tensile deformation between different sections, thereby creating residual stress. Processes such as rolling, drawing, extrusion, cutting, and shot peening can induce non-uniform plastic deformation.

2) Residual Stress from Thermal Effects:

Residual stress induced by thermal effects is complex. During the heating or cooling process, temperature gradients can exist within the material. The non-uniform heating or cooling results in non-uniform thermal expansion and contraction, generating thermal stress. Additionally, when changes in the material's structure cause non-uniform volume changes within the material, phase transformation stress can occur. When plastic deformation occurs due to thermal effects, it can impact the material's mechanical properties, including yield strength and elastic modulus, thereby affecting stress changes.

3) Residual Stress from Chemical Actions:

Residual stress arising from chemical actions is a result of chemical or physical changes transmitted from the surface to the interior of a material. For example, in the case of ceramics, a glaze material is applied to the surface, and then it is heated to form the glaze layer. Because the glaze layer has a higher coefficient of expansion, it generates tensile stress on the surface during cooling, leading to cracking. These cracks are typically regular, and most of them connect to each other, allowing the tensile stress along their vertical direction to disappear. Cracks formed by soil cracking exhibit a star-shaped pattern with angles of 120 degrees.

When steel undergoes ammonia gas carburization, a surface compound layer with a larger volume is formed. This results in significant residual compressive stresses on the surface. A similar situation occurs during carburization processes involving carbon. These residual stresses are primarily due to density changes resulting from chemical transformations.

3.3. Causes of Microscopic Residual Stress

Microscopic internal stress falls within the microscopic range and can be divided into two categories based on their range of effect: the second type and the third type of internal stress. One is second type of internal stress (microstructural stress). This stress operates at the level of individual grains or subgrains, typically within the range of 0.01 to 1 mm. It represents the average stress within this range and acts on grain boundaries, subgrains, or other microstructural components. The other is third type of internal stress (intragranular substructural

stress). This stress operates within individual grains, typically within the range of 10^{-6} to 10^{-2} mm. It affects the internal substructures of a single grain and is responsible for stress variations within a grain.

Microscopic internal stress can be attributed to various factors based on the cause of its generation, and these can be categorized as follows:

1) Microscopic Internal Stress Due to Crystal Anisotropy:

This type of internal stress arises from the anisotropy of crystal properties, such as differences in thermal expansion coefficients, elastic moduli, and crystal orientations within grains. For example, single crystals of lead can exhibit a 1 to 3-fold variation in elastic modulus with different crystal orientations, while single crystals of zinc can show a 1 to 4-fold variation in elastic modulus. Most metals exhibit anisotropy in their elastic moduli, with the <111> crystallographic direction having the maximum modulus and the <100> direction having the minimum. In polycrystalline materials, due to variations in grain orientations, even when uniform external forces are applied, each grain may deform differently. This discrepancy can lead to internal stresses, especially when plastic deformation occurs.

2) Microscopic Internal Stress Due to Plastic Deformation Inside and Outside Grains:

This category of microscopic internal stress is generated as a result of plastic deformation processes inside grains. It includes phenomena such as slip deformation within grains, dislocation accumulation at grain boundaries, dislocation penetration across grain boundaries, and the formation of twin boundaries. For example, when slip deformation occurs inside grains, dislocations accumulate at grain boundaries, and they may even penetrate grain boundaries and propagate over a broader range, resulting in features like dislocation slip bands. As dislocations pass through grains, they do not disappear but may create various internal defects within the microstructure. These processes are the main reasons for the generation of microscopic internal stresses after the removal of external loads.

3) Microscopic Internal Stress Due to the Presence of Inclusions, Precipitates, or Phase Transformations:

When inclusions, precipitates, or phase transformations occur within the microstructure of metal materials, they can introduce significant microscopic internal stress. This is primarily due to volume changes and the development of thermal stresses during the presence of different phases or the occurrence of phase transformations within the material's microstructure.

4. Current Research Status on Stress in Electronic Packaging Systems

Various factors influence packaging defects and failures, with material composition, properties, packaging design, environmental conditions, and process parameters all playing a role. Identifying these factors is a fundamental requirement for preventing packaging defects and analyzing their triggering mechan-

isms. Due to the thermosetting nature of epoxy-based advanced packaging materials, the generation of residual stress can be broadly divided into two stages: physical changes and chemical changes, as illustrated in **Figure 1** [12] [13] [14] [15] [16].

To determine these influencing factors, researchers often employ experimental or simulation methods. Typically, they use physical models (Formula 1-1) and numerical parameter-based approaches. For more complex defect and failure mechanisms, an empirical approach is frequently used to identify key influencing factors. However, this method is time-consuming, requires equipment modifications, has low efficiency, and involves high costs. Moreover, these methods lack a direct connection with practical application scenarios and cannot accurately characterize the evolution and distribution of internal stress in epoxy-based advanced packaging materials throughout the curing and packaging processes [17] [18] [19].

$$Stress = k\int_{T_1}^{T_2} \Delta CTE \cdot E \cdot \mathrm{d}T \tag{1-1}$$

Formula (1-1): Stress calculation formula (k: Proportionality constant T_1, T_2: Temperature range E: Young's Modulus) [17].

This necessitates a means of directly characterizing stress conditions in electronic packaging systems through *in-situ* observations. Mayer and others designed an ambient temperature stress sensor to analyze the bonding process, monitoring stress levels in the gold ball bonding locations. Trigg and colleagues developed a silicon piezoresistive sensor that precisely measures stress changes, offering high resolution and accuracy. Nevertheless, as advanced packaging

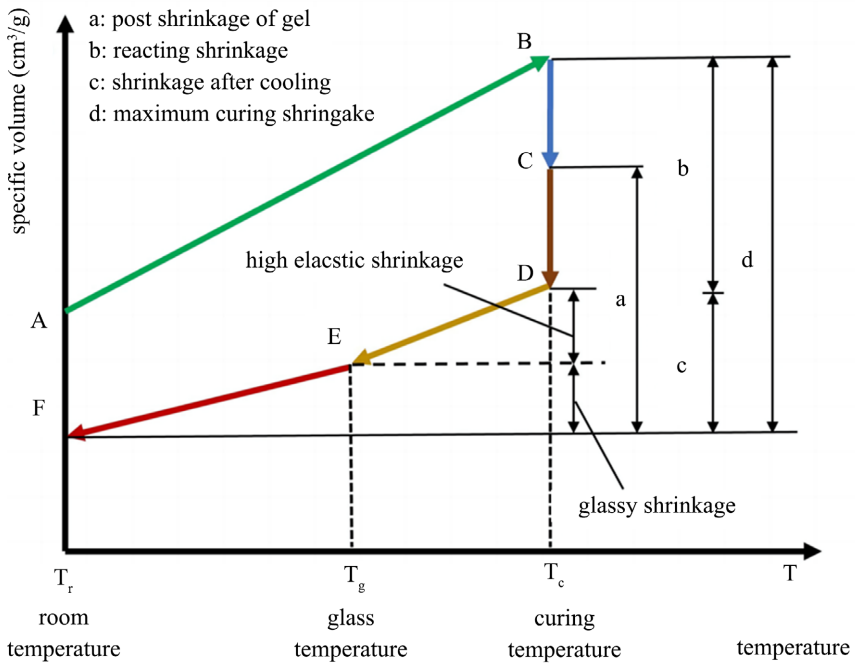

Figure 1. Schematic diagram of volume changes during the curing process of epoxy-based advanced packaging materials [11].

technologies have evolved, 3D packaging has emerged as the forefront of research. The earlier methods exhibit several limitations and cannot accurately represent the changes in stress and their distribution within the packaging materials themselves and within the complex and variable packaging systems [20] [21] [22].

With the development of electronic packaging technology, packaging systems have become more complex, miniaturized, and diversified, leading to increased demands on packaging materials. One of the primary failure phenomena caused by residual stress in integrated circuit systems is warping, which is also one of the main challenges in electronic packaging systems. Warping primarily occurs during the curing and cooling processes of packaging materials due to the mismatch in coefficients of thermal expansion (CTE) between different materials.

Controlling warping is challenging, especially in the case of large and thin packages. Post-packaging warping can also pose a reliability issue as it carries risks of passivation cracking, aluminum metallization deformation on the mold, wire bonding breakage, mold cracking, and EMC cracking, among others.

In addition to warping, failure phenomena resulting from residual stress include solder ball fracture, solder fatigue, and packaging cracking. Some researchers have conducted comparative discussions on the performance of epoxy plastic sealing materials and their failure characteristics during the device packaging process, focusing on reliability, flowability, and internal stress. Through related experiments and defect analysis, they aim to ensure the quality and reliability of products.

Apart from chip failures, excessive stress loads can also lead to a decline in the performance of semiconductor devices. For example, when a device is subjected to a compressive stress of 100 MPa, its electrical conductivity can decrease by approximately 18%.

Finite element analysis is typically an indispensable tool when analyzing residual stress and failure phenomena in a packaging system. Kohta *et al.* [23], for instance, used a three-dimensional finite element simulation method to analyze the impact of underfill material's mechanical properties on the structure of flip-chip packages. They summarized the influence of packaging material properties on chip delamination. Lin *et al.* [24] employed finite element simulations to analyze stress and strain conditions during power cycling and thermal cycling of flip-chip lead-free packaging systems. They also discussed the reliability of second-level interconnects based on some experimental results. Long *et al.* [25] conducted research on the effects of different fillers on the mechanical properties of materials using finite element simulation technology and nanoindentation. They also conducted reliability assessment and analysis. Furthermore, researchers like Chou *et al.* [26] have explored similar aspects.

However, finite element methods can only provide approximate computer models that represent the approximate distribution and trends of stress in electronic packaging systems. They cannot entirely reflect the specific stress distribution of the packaging system, especially for certain process steps, such as the

curing of epoxy-based advanced packaging materials, where stress changes cannot be obtained through simulation methods.

5. Conclusions

Through literature research, it has been found that in packaging systems with small pitches and a high number of I/Os, harmful tensile stresses are generated on the top surface of silicon chips when the packaging material cures and contracts. The stress during packaging is a function of packaging processes, packaging materials, and curing processes. Therefore, the choice and processing of packaging materials are crucial for device performance and reliability. So far, *in-situ* characterization methods for residual stress in epoxy-based packaging materials are scarce and inaccurate. Thus, embedding stress sensors is the most effective means to characterize the numerical values and distribution patterns of residual stress in epoxy-based advanced packaging materials and device applications, which cannot be achieved by other methods.

Accurately measuring and characterizing the residual internal stress of advanced packaging materials are the focus of future work. Through the characterization of residual stress, the reliability and performance of advanced packaging materials can be improved.

Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

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