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An Adaptive Slope Compensation Circuit for Peak Current Mode of Boost Switching Power Supply

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Abstract

Based on the analysis of the basic principle of slope compensation, a high-precision adaptive slope compensation circuit for peak current mode boost DC/DC converter is designed. The circuit dynamically detects the input and output voltage of the boost circuit to realize automatic adjustment of the compensation amount with the change of duty ratio, which makes the ramp compensation slope optimized. The design uses a high-precision subtracter to improve the accuracy of slope compensation. While eliminating sub-slope oscillation and improving the stability of boost circuit, the negative impact of compensation on boost circuit is minimized, and the load capacity and transient response speed of boost circuit are guaranteed. The circuit is designed based on SMIC 0.18um CMOS technology, with simple structure, high reliability and easy engineering implementation. Spectre circuit simulator 17.1.0.124 64b simulation results show that the circuit has high compensation accuracy and wide input and output voltage range. When the working voltage is 3.3 V, the compensation slope can be adjusted adaptively under different duty cycles, and the minimum error between the compensation slope and the theoretical optimal compensation slope is only 0.42%.

Keywords

Adaptive Slope Compensation, Boost Circuit, Peak Current Mode, Subtracter, Accuracy

1. Introduction

In modern power electronics systems, direct-current-to-direct-current (DC-DC) converters are widely used in mobile devices, communication systems, industrial

automation, and renewable energy sources as core components for energy conversion and management. However, DC-DC converters often face a variety of disturbances and instability factors in practical applications, one of which is the slope problem. As an effective solution, precise control and stability enhancement of the DC-DC converter output voltage can be realized by introducing a slope compensation circuit.

The peak current mode control technique based on PWM modulation is widely used in DC-DC circuits due to its advantages of fast response speed, simple frequency compensation [1] [2] [3], certain automatic current limiting effect, and good load tuning and linear tuning rates. However, when the duty cycle of the PWM control signal exceeds 50%, the peak current mode control mode is prone to subharmonic oscillations, which leads to system instability and other problems, and a slope compensation circuit needs to be introduced. As a result, compensation techniques such as primary linear slope compensation and segmented linear slope compensation [4] [5] have emerged, but the compensation slope of these methods are fixed and prone to overcompensation problems, resulting in unwanted load carrying capacity and degradation of system transient response. The adaptive slope compensation technique [6] [7] [8] [9] is able to self-adjust the value of the slope compensation slope with the change of the system duty cycle, which avoids the over-compensation phenomenon, improves the inductor current, and ensures the system load carrying capacity and transient response.

In this paper, an adaptive slope compensation circuit is designed for peak current control mode boost converter, according to the duty cycle change, the circuit can automatically adjust the compensation slope, avoiding the generation of subharmonic oscillations while eliminating the overcompensation phenomenon and reducing the negative impact of compensation on the system.

2. Stability of Slope Compensation

2.1. Instability due to Subharmonic Oscillations

When the converter is controlled in peak current mode, as shown in **Figure 2(a)**, when the duty cycle is less than 50%, the disturbance to the inductor current

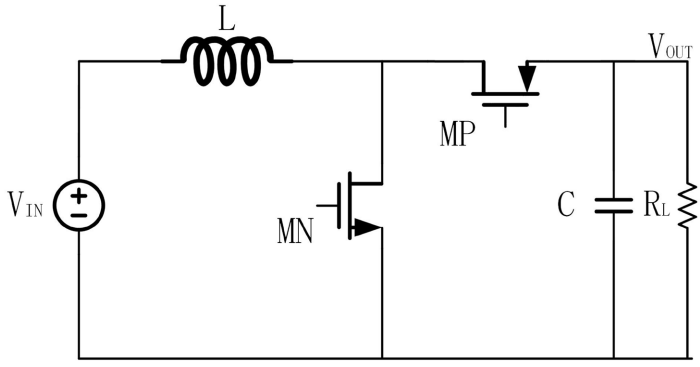

Figure 1. Boost DC-DC converter topology.

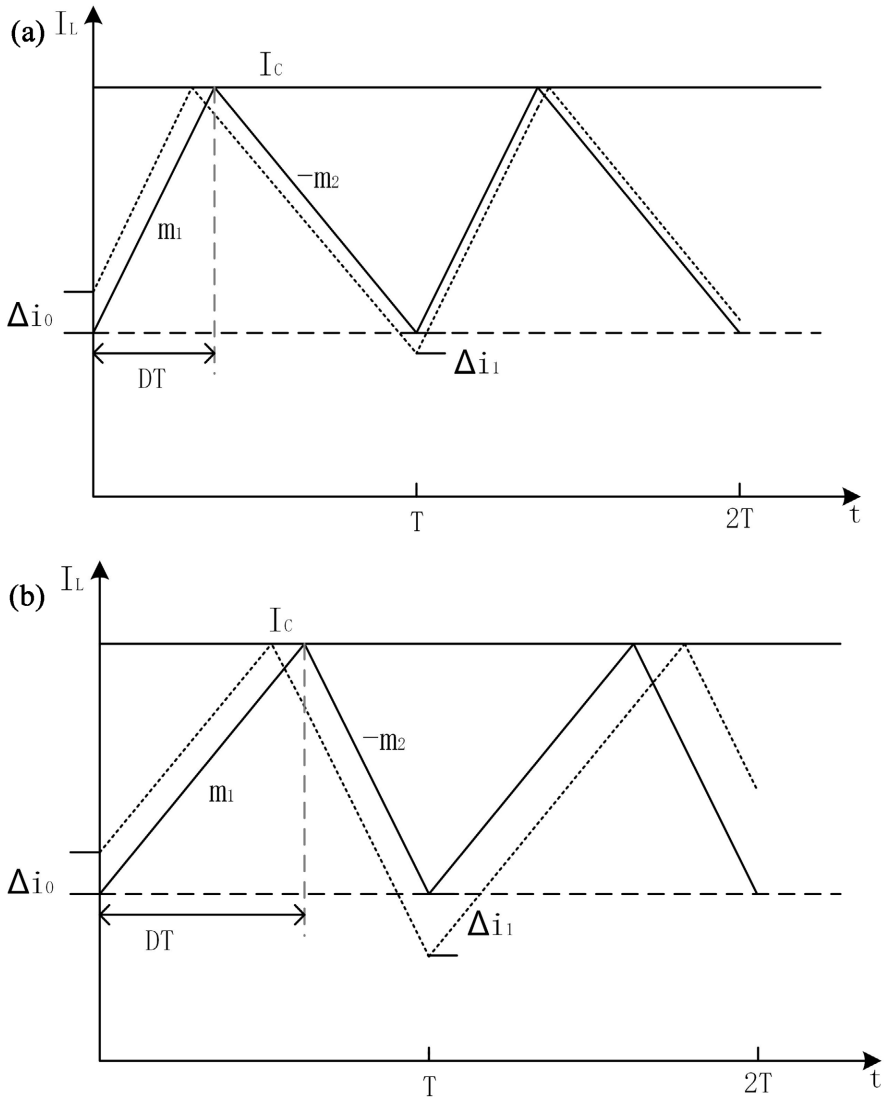

Figure 2. Analytical diagram of subharmonic oscillation generation. (a) Inductor current disturbance at duty cycle less than 50%; (b) Inductor current perturbation at duty cycle greater than 50%.

converges with the cycle; when the duty cycle is greater than 50%, as shown in **Figure 2(b)**, an unstable phenomenon occurs in the system, and the disturbance to the inductor current will increase with the cycle [6] [10] [11], generate sub-slope oscillations [4].

2.2. Calculation of the Compensation Slope

In **Figure 2**, I_C is the control quantity of the current inner loop, Δi_0 is the perturbation quantity of the inductor current, T is the operating period, D is the duty cycle, and m_1 and m_2 are the slopes of change of the rising and falling inductor currents, respectively. In the case where the converter operates in continuous conduction mode without slope compensation, by the volt-second balancing principle, for a boost-type converter:

$$\frac{m_2}{m_1} = \frac{D}{1-D} \tag{1}$$

From the Figure 2, the current error Δi_1 due to perturbation after one cycle is:

$$\Delta i_1 = -\frac{m_2}{m_1} * \Delta i_0 = -\frac{D}{1-D} * \Delta i_0 \tag{2}$$

Then after n cycles, the error due to the initial perturbation amount is:

$$\Delta i_n = \left(-\frac{m_2}{m_1}\right)^n * \Delta i_0 = \left(-\frac{D}{1-D}\right)^n * \Delta i_0 \tag{3}$$

From the Equation (3), when $D < 50\%$,the amount of perturbation to the inductor current decreases with period and decays to 0, stabilizing the system; whereas when $D > 50\%$,the inductor current is affected by the perturbation gradually increases with the cycle, generating subharmonic oscillations, and the system's immunity to interference deteriorates, preventing it from working stably.

In order to eliminate the subharmonic oscillations, a ramp compensation is added to the system, whose inductor current variation is shown in Figure 3, and m_c is the slope of the ramp compensation signal. It can be obtained from Figure 3:

$$\Delta i_1 = -\frac{m_2 - m_c}{m_1 + m_c} * \Delta i_0 \tag{4}$$

After n cycles, the inductor current perturbation with the addition of the compensation signal is:

$$\Delta i_n = \left(-\frac{m_2 - m_c}{m_1 + m_c}\right)^n * \Delta i_0 \tag{5}$$

In order for the inductor current perturbation to converge, it should be satisfied that:

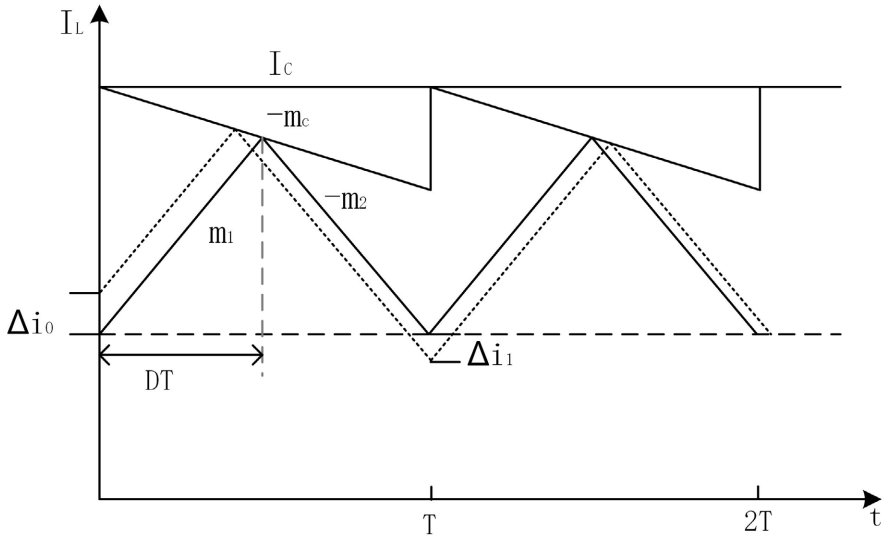

Figure 3. Inductor current disturbance after slope compensation.

$$\frac{m_2 - m_c}{m_1 + m_c} < 1 \tag{6}$$

The above equation reduces to:

$$m_c > \frac{1}{2}(m_2 - m_1) \tag{7}$$

In boost topology [12], we have $m_1 L = V_{in}$, $m_2 L = V_{out} - V_{in}$, which can be obtained by substituting in the Equation (7):

$$m_c > \frac{\frac{1}{2}V_{out} - V_{in}}{L} \tag{8}$$

It can be seen that when the m_c satisfies the above conditions, it is able to eliminate the subharmonic oscillations and avoid the open-loop instability that arises in the peak current control mode.

3. Adaptive Slope Compensation Circuit Design

The circuit proposed in this paper is shown in Figure 4. For the peak current mode controlled boost converter, an adaptive slope compensation circuit is designed using SMIC 0.18um CMOS process. It ensures that the system can automatically adjust the appropriate compensation slope with the change of input and output voltages to realize a fast response while working stably. The circuit

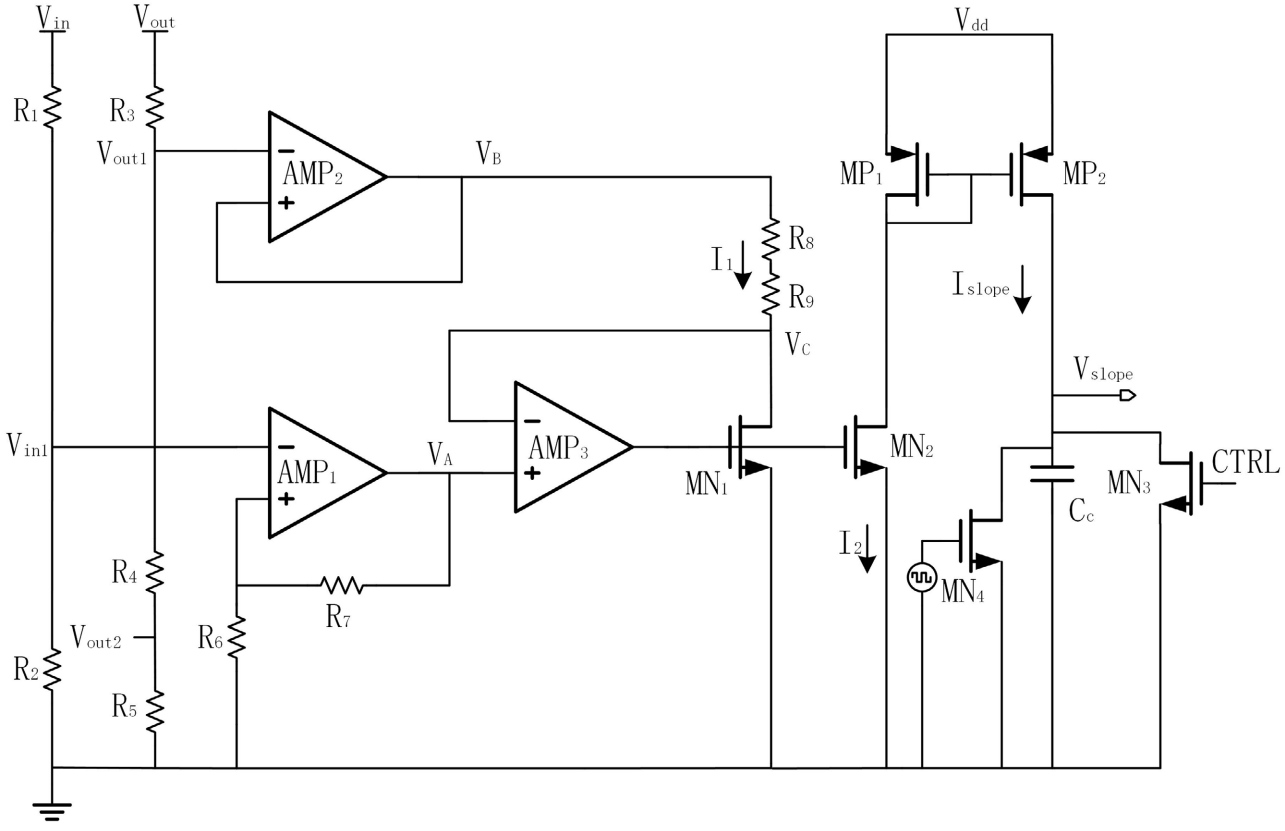

Figure 4. Adaptive slope compensation circuit designed in this paper.

can be mainly divided into voltage acquisition module, ramp voltage generation module and reset module.

3.1. Voltage Acquisition Module

The voltage acquisition module samples V_{in} and V_{out} and converts them to current. Its circuit is shown in Figure 4. The input voltage V_{in} and output voltage V_{out} are first converted to the voltage range that can be handled by the op amp through a resistor divider network. The design takes its sampling scale factor to be $1/N$, thus

$$V_{in1} = \frac{R_1}{R_1 + R_2} * V_{in} = \frac{V_{in}}{N} \tag{9}$$

$$V_{out1} = \frac{R_4 + R_5}{R_3 + R_4 + R_5} * V_{out} = \frac{V_{out}}{N} \tag{10}$$

Voltage acquisition module mainly consists of three op-amps, V_{in1} through the amplifier AMP1 to get V_A, design take $R_6 = R_7$, can be obtained:

$$V_A = \left(1 + \frac{R_7}{R_6}\right) * V_{in1} = 2V_{in1} \tag{11}$$

The same reasoning applies:

$$V_B = V_{out1} \tag{12}$$

V_A is fed into the input of the amplifier AMP3, and the operational amplifier AMP3 and the transistor MN1 are connected to a voltage negative feedback structure so that V_C strictly follows the variation of V_A, so that the currents flowing through the resistors R_8 and R_9 are jointly determined by the voltages V_B and V_C, generating the current I1 that is correlated with the input-output voltage:

$$I_1 = \frac{V_{out1} - 2V_{in1}}{R_8 + R_9} = \frac{V_{out} - 2V_{in}}{R_8 + R_9} * \frac{1}{N} \tag{13}$$

3.2. Ramp Voltage Generation Module

MN2 and MN1 take the same aspect ratio, hence $I_2 = I_1$, the ratio of the aspect ratio of MP1 to MP2 is 2:N. Therefore, the current Islope after the current I_2 passes through the current mirror is:

$$I_{slope} = I_2 * \frac{1}{N} = \frac{\frac{1}{2}V_{out} - V_{in}}{R_8 + R_9} \tag{14}$$

I_{slope} charges the capacitor C_c to produce the ramp signal V_{slope} [4] [5] [6] [11] and the voltage signal slope expression is:

$$T_c = \frac{\mathrm{d}V_{slope}}{\mathrm{d}t} = \frac{I_{slope}}{C_c} = \frac{\frac{1}{2}V_{out} - V_{in}}{R_8 + R_9 * C_c} \tag{15}$$

Setting the appropriate values of resistors R_8, R_9 and capacitor C_c means that the slope compensation can be adjusted adaptively to obtain the optimal com-

pensation slope that stabilizes the system.

3.3. Reset Module

From the analysis in section 2, it can be seen that the system generates subharmonic oscillations when the duty cycle is greater than 50%, so the system does not need adaptive slope compensation when the duty cycle is less than 50%, and a reset module can be added to make the slope compensation signal canceled when the duty cycle is less than 50%. Let $R_4 = R_5$, then $V_{out2} = 0.5\ V_{out1}$, the voltage signals V_{in1} and V_{out2} are connected to the positive and negative terminals of the comparator COM respectively the output signal is connected to the gate of MN3. As shown in Figure 5.

In the boost converter, when the duty cycle is less than 50%, the input and output voltage relationship is:

$$V_{in} > \frac{1}{2} V_{out} \tag{16}$$

At this time, the comparator output high level makes the reset tube MN3 on, and the slope voltage V_{slope} is pulled down, and no compensation signal is generated. The gate signal of MN4 is a narrow pulse signal, so that the compensation signal can be dropped quickly.

4. Simulation Result

Adaptive slope compensation circuit is designed using SMIC 0.18 um CMOS process and pre-simulated in Cadence using Spectre circuit simulator 17.1.0.124 64b. The supply voltage is 3.3 Volts, the clock signal frequency is 1MHertz and the value of inductor L is 2uHenries. The circuit is simulated and verified for different input voltages, output voltages, temperatures and process angles.

When the input voltage is 3.3 Volts, the temperature is 25˚C, the process corner is tt, and the output voltage is between 8 - 15 Volts, the circuit is simulated, and the results are shown in Figure 6. The waveform shows that with the increase of output voltage, the duty cycle gradually increases, and the voltage compensation slope also increases, which is consistent with the theory. Table 1 shows the comparison between the compensation slope shown by the simulation waveform and the theoretical optimal compensation slope. The results show that when the output voltage is 15 Volts, the error between the voltage compensation slope and the theoretical compensation slope is the smallest, and the deviation ratio is only 0.42%.

When the input voltage V_{in} = 3.3 Volts, the output voltage V_{out} = 12 Volts, and the process cornor is typical typical, the simulation verifies the performance of

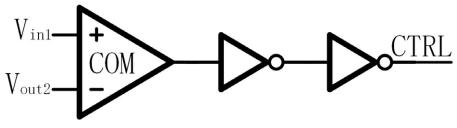

Figure 5. Reset module.

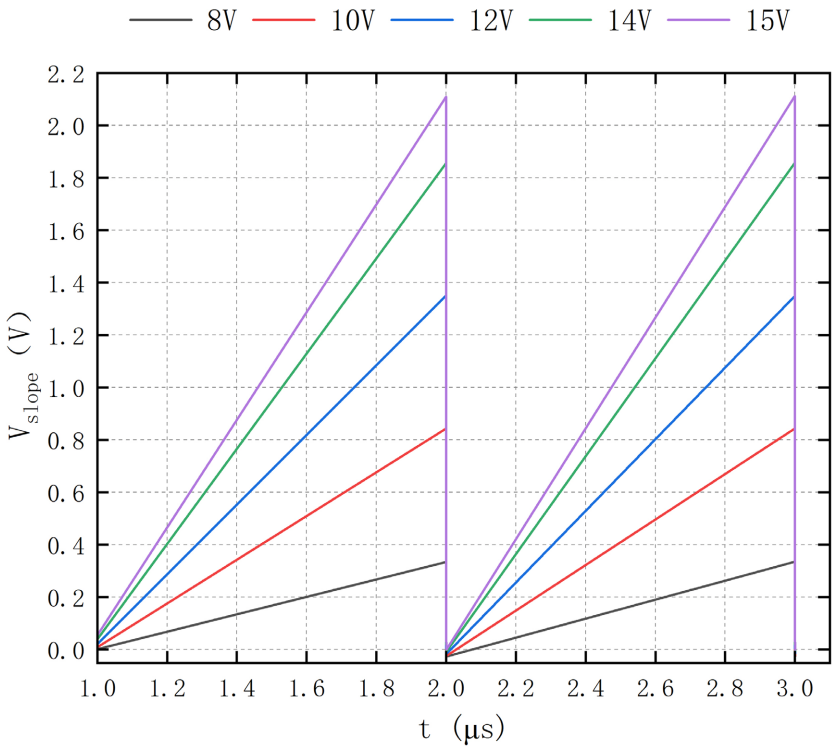

Figure 6. Compensation slope at different output voltages for input voltage 3.3 Volts.

Table 1. Comparison of simulated compensation slopes with theoretical optimal compensation slopes.

Output Voltage/V	Theoretical value/ (V/us)	Simulation results/ (V/us)	deviation ratio
8	0.35	0.3613177	3.23%
10	0.85	0.8667901	1.98%
12	1.35	1.3657274	1.16%
14	1.85	1.8624961	0.68%
15	2.10	2.1088029	0.42%

the slope compensation circuit at different temperatures, and the results are shown in **Figure 7**. Resistor R_8 and resistor R_9 are positive temperature coefficient resistor and negative temperature coefficient resistor, respectively, and by adjusting the ratio of the two, the influence caused by temperature on the circuit is greatly reduced. The minimum difference between the peak values of the ramp compensation voltages is 19 mv when the temperature range is between −40˚C and 85˚C.

When the input voltage V_{in} = 4 Volts, the output voltage V_{out} = 10 Volts, and the circuit operates at 25˚C, the simulation of the slope compensation circuit at different process cornors is shown in **Figure 8**. The simulation results show that the maximum difference between the peak values of the compensated voltages is 61 mv.

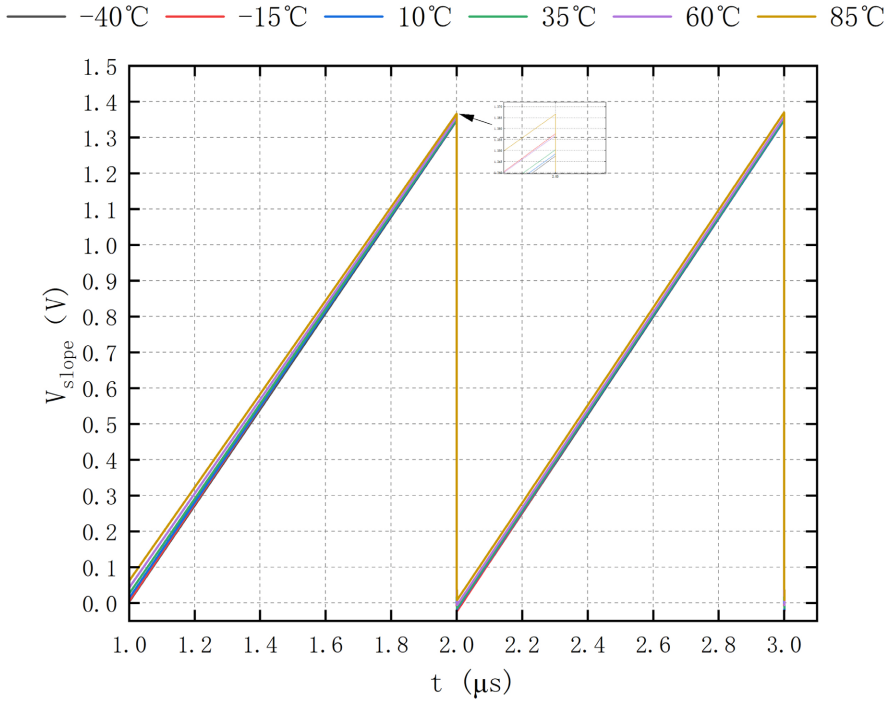

Figure 7. Compensation slope of simulation at different temperatures.

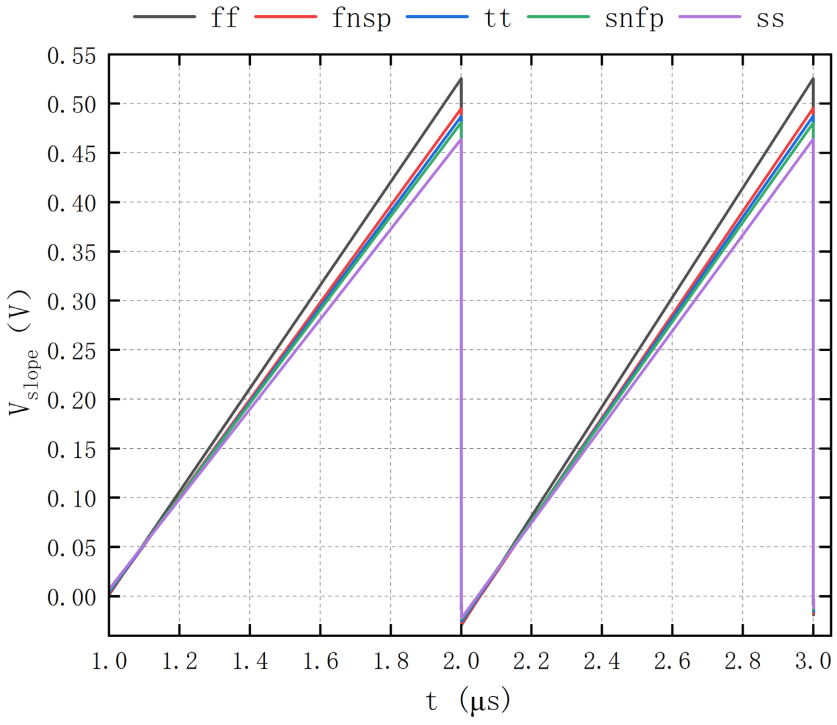

Figure 8. Simulated compensation slopes for different processes corners.

When the circuit operates at different output voltages, the slope compensation slope varies with the duty cycle. By setting the value of resistance, the circuit designed in this paper charges the compensating capacitor and adds the compensating voltage to the circuit when the duty cycle is greater than 50%. The com-

parison between the theoretical slope with the duty cycle change and the compensation slope verified by the circuit simulation in this paper is shown in Figure 9. Where T_c is the simulation value and m_c is the theoretical optimal value. The circuit can achieve the theoretically optimal compensation slope with a small error.

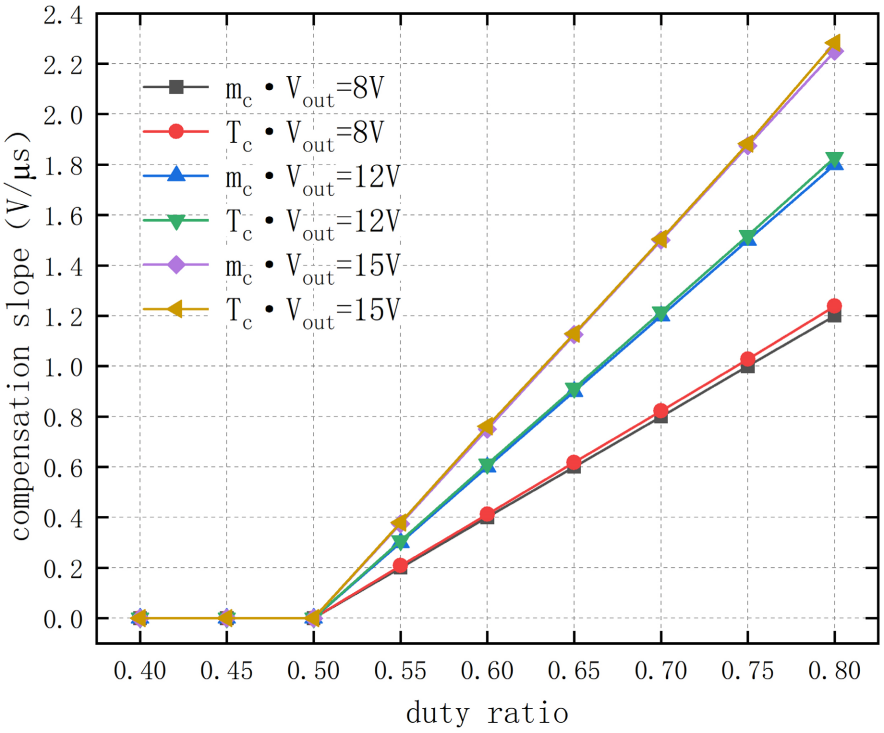

Figure 9. Comparison between theoretical slope and compensation slope verified by circuit simulation in this paper.

5. Conclusion

In this paper, an adaptive slope compensation circuit for PCM controlled boost DC-DC converter is designed. The circuit uses a subtracter circuit to obtain a current proportional to the voltage difference between input and output, and generates a circuit through the ramp to output a suitable compensation voltage. The simulation results show that the adaptive slope compensation circuit can adaptively change the compensation slope with the change of duty cycle, and the error with the theoretical optimal compensation slope is small, the dynamic compensation is realized, and the load capacity and transient response speed of the boost converter circuit are guaranteed. A simple temperature compensation is added to the circuit, which reduces the influence of temperature on the circuit and further improves the compensation accuracy. Influenced by the process, the ramp voltage has a slightly larger range of peak fluctuations at different process cornors, which can be corrected by trimming techniques in subsequent studies, or the circuit can be further improved to minimize the effect of the process.

Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

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