Color Image VGA Display Based on FPGA and OV7725

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Abstract

In order to collect image data in real time, the main control chip based on Cyclone IV is the EP4CE10F17C8 as the main control chip. The image information is obtained through the camera and displayed on the VGA screen. The OV7725 camera is initialized by the SCCB bus, obtained the YUV data stream, and the video flow is cached to the SDRAM. Display through VGA. The YUV data obtained from the OV7725 sensor is used in FPGA to design circuits with Verilog language, convert RAW into RGB signals, and obtain color images.

Subject Areas

Electronic Engineering

Keywords

FPGA, YUV, SDRAM Controller, VGA

1. Introduction

With the rapid development of computer images, computer images are applied to many fields, including hospitals, and military equipment. Compared with the CCD sensor, the power consumption of CMOS sensors is relatively affordable, and it has applications in aviation, aerospace and industrial production.

FPGA has the ability to process video data in parallel, and has low power consumption, which can be used in real-time processing video image data. This article introduces a color image display system based on FPPA. Select EP4CE10F17C8 as the main control chip, Haowei's OV7725 chip can output data in YUV, RAW, and RGB format. Verilog language design drive circuit, converted into RGB color signal, stored through SDRAM, and displayed on the VGA screen [1] [2] [3].

At present, due to the increase of the pixels of the image sensor, the image information data is relatively large; in some specific fields, such as the medical field and the military field, the requirements for processing speed are relatively high. At present, most image processing is developed on the host computer. The rapid development of hardware GPU has greatly improved the efficiency of image processing. However, limited by the serial processing method of software algorithms, real-time image processing cannot be realized. Compared with software processing methods, using hardware for image processing is faster, including FPGA, DSP, etc. FPGA has the characteristics of parallel high-speed data processing, adopts Verilog encoding method, obtains image information through hardware, uses SDRAM to store image data, and realizes the operation and processing of large amounts of data [4] [5] [6].

2. Hardware Circuit Design

2.1. System Block Diagram

The system has three components, as shown in Figure 1: data collecting, data processing, and image display. By setting up the initialization parameters of the OV7725, the acquisition module gathers video data, turns it into RGB color data in the FPGA, saves it in SDRAM Store, and drives VGA to display the monitoring image.

2.2. Sensor OV7725

OV7725 is a single-chip VGA camera with a size of 1/4 inch, which can be used as a high-performance image sensor. OV7725 has a 640×480 photosensitive array, supports VGA video at the fastest 60 fps, and can configure data formats and image effects. It can output video streams in RAW, RGB, and YCBCR formats. We configure the OV7725 through the SCCB interface. It can be seen from the figure that XCLK provides the clock, and the photosensitive components are responsible for sampling data, and then obtain the analog data of 640*480. That is, the original data. Through 12-bit AB conversion, the input analog signal is converted into a digital signal, that is, RAW data. Image processing is performed in the built-in DSP module, and a 10Bit data stream in a specific format is output. We convert it in the FPGA, to generate the RGB video stream data we need.

3. System Software Design

The image data formats that the camera OV7725 can output include YUV422, RGB565, and RAW data. By querying the OV7725 registration manual, you can find that the port COM7 can configure the parameters of the output data. We configure the OV7725 register through the SCCB interface in the FPGA to get our expected video stream format. SCCB belongs to a characteristic IIC protocol, including a data line and a clock line, where the data line is bidirectional.
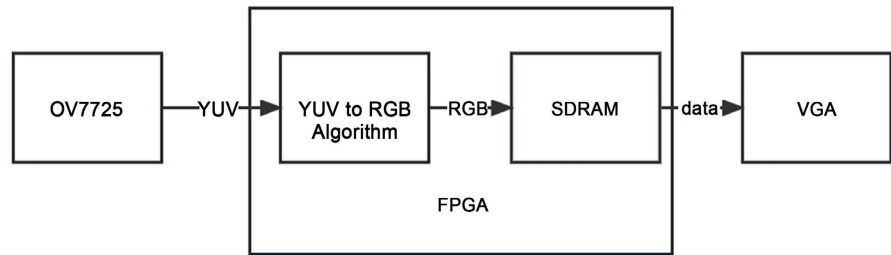
Figure 1. Example of a system block.

3.1. SCCB Communication Protocol

In order for the SCCB bus to send data in a serial manner, send 8 bit data at one time, first send the high-significant bit MCB, and then send the low-significant bit LSB, similar to the data transmission format of the SPI bus; the difference is that SCCB does not require additional chip selection Signal SPI_CS. Send 8 Bit data signal at a time, receive the corresponding signal returned, and judge the completion of data transmission. Figure 2 shows the example of SCCB clock diagram.

We are aware of SCCB's read and write timing. The registers must be initialized for the sensor to operate normally; otherwise, picture data cannot be obtained. OV7725 contains 172 registers in total value. The key registers for the video picture stream, output format, sampling quality, etc. are where we primarily concentrate our attention. In this design, the camera is configured to produce YUY format, with a VGA image output format and a 640*480 resolution.

3.2. SDRAM Storage Module Design

SDRAM, the English full name is Synchronous Dynamic Random Access Memory, that is, dynamic random access memory. Synchronization means that a synchronous clock needs to be used to control the transmission of data and the sending of commands; dynamic means that the storage array keeps refreshing to ensure that data is not lost; random means that data Specify the address to read and write data, not linear storage.

The SDRAM controller is used to drive the SDRAM off-chip memory and cache the image data output by the CMOS sensor. It encapsulates the complex structure of the SDRAM into a FIFO-like interface, outputs the data required by the VGA, and realizes the transmission across frame rates. Since the OV7725 camera collects 640 × 480 data, the data flow is relatively large, and it is not suitable for FPGA on-chip resource storage. This design uses an external SDRAM chip for data caching. It is necessary to initialize the SDRAM chip first, and then perform row activation, Column read and write, precharge and other operations.

3.3. VGA Display Module Design

Read data from SDRAM and output to VGA. Since the VGA interface on the board is in RGB565 format, conversion from RGB888 to RGB565 is required.
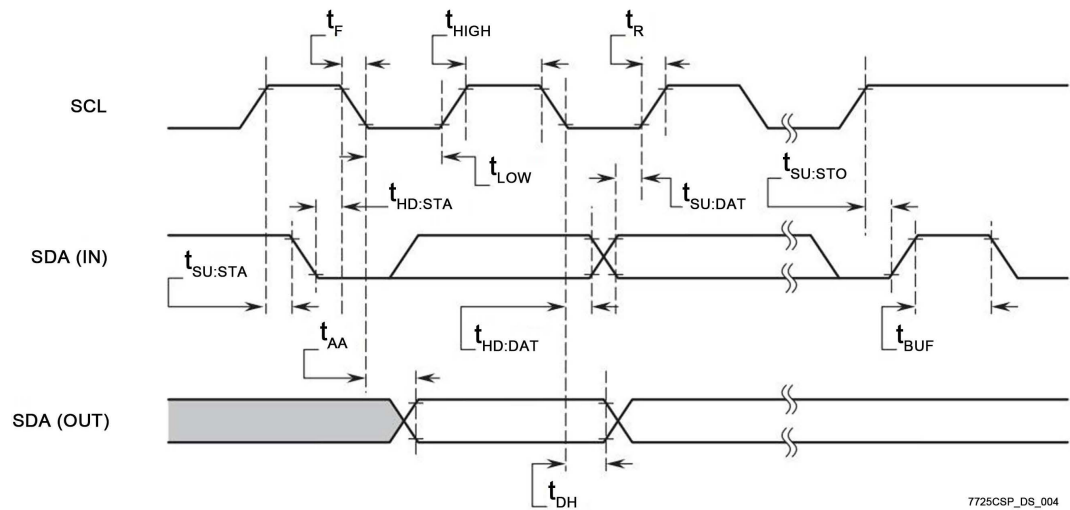
Figure 2. Example of SCCB clock diagram.

Figure 3. Example of image display test.

The full English name of VGA is Video Graphic Array, and the Chinese name is Video Image Array. During VGA transmission, video Image data is divided into three signals of RGB, that is, red, green and blue. Digital-to-analog conversion into model signals.

4. Image Display Test

Verilog program analysis and synthesis based on modified QUARTUS II software. Set its pins after making sure there are no problems, then compile and download the general program to the FPGA circuit board. The data source is obtained by OV7725, which then processes RGB data using an FPGA. 640*480 pixels are displayed with VGA. The display is stable and the image color is clear, according to actual measurement. (Figure 3)

5. Summary

Provide a method based on YUV signal for image acquisition of OV7725, use the customizability of FPGA to convert YUV into RGB signal, and store video data in SDRAM for VGA screen display. This design clearly displays image data, the

next step. The research direction is to obtain RAW data stream, convert it into RGB video stream in FPGA and display it.

Acknowledgements

Conflicts of Interest

The author declares no conflicts of interest.

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