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Reduced Recombination Current Due to Sputtered CdO Nanolayer at CdS/CdTe Interface

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Abstract

In this paper, interface engineering via sputtering of CdO nanolayer at the buffer-CdS/CdTe-absorber interface is demonstrated as an efficient approach to improve the performance of solar cell device. The *i*-CdO interfacial layer with various thicknesses from 5 nm to 35 nm was deposited by DC magnetron sputtering. Comparative studies on TCO/CdS/CdTe and TCO/CdS/CdO/CdTe interfaces have been conducted by current-voltage, capacitance-voltage and admittance spectroscopy measurements. The current-voltage characteristics of the devices with an area of 0.45 cm^2 under 100 mW/cm^2 illumination, at the optimum thickness of CdO intermediate layer in the proposed structures, show increases of the short circuit current density and the open circuit voltage by 5% and 25%, respectively. The efficiency improvement of 3.1% of *p-i-n* cell over *p-n* cell is observed. Results of the temperature-dependent current-voltage and admittance measurements revealed the removing of the deep level defect with the activation energy of 0.43 eV and the reducing of the ideality factor from 1.9 to 1.8 via buffer/absorber interfacial passivation method. Interface passivation appears to be critical to improve the short circuit current density and the open circuit voltage, and CdO thin film is clearly effective for this purpose.

Keywords

CdS/CdTe Photovoltaic Devices, CdO Interface Engineering, Defects

1. Introduction

CdTe solar cells with certified power conversion efficiency of 22.1% have attracted significant attention due to their excellent photovoltaic properties [1]. But there is still much potential for progress towards the 32% Shockley-Queisser limit [2]. The intensive research works are performed across various compo-

nents of a photovoltaic device. For CdTe thin film technology, various buffer and interfacial layers, such as CdS, ZnO, $Zn_{1-x}Sn_xO$ (ZTO) or $Mg_xZn_{1-x}O$, (MZO) have been successfully implemented for the interface engineering, but there is yet significant space for R&D in this direction [3]-[8]. A lot of publications [9] [10] [11] revealed that the CdS/CdTe interface is in the cliff category and is not favorable from the band-offset perspective. Therefore, this type of interface recombination will not be considered in this paper. Also, it is shown that polycrystalline CdTe have been limited to hole density on the order of 10^{14} cm^{-3}, higher carrier recombination in the absorber and interfaces [12] [13] [14] [15] [16]. Among interfaces problems, the one between CdS and CdTe is imperative for efficient extraction, collection and recombination. Shockley-Read-Hall recombination due to defects or mismatches within the crystal lattice can create trap states that are spatially localized and energetically exist between the valence and conduction bands [17] [18] [19]. The mobile free carriers can be captured and bound to the traps. It can also be the case where a hole or an electron in the trap can recombine with a free electron or hole respectively, and then the trap is considered a recombination center. Surface recombination processes are due to defects that exist at semiconductor surfaces and interfaces. These defects create spatially localized states in the energy bands because of broken bonds, extrinsic impurities from the environment or as a result of the semiconductor growth/deposition process. It has been shown in a lot of publications that sulfur and telluride diffusion cannot improve device efficiency, despite minimizing lattice mismatch at the CdS/CdTe interface [20] [21] [22] [23]. This is because the number of misfit dislocations is conserved, and sulfur diffusion shifts the dislocations further into the space charge region, where the SRH recombination rate is higher. A way to increase efficiency of solar cells is by applying an intrinsic semiconductor broadening layer to the depletion region of a *p-n* junction. Literature survey [24] shows that in the amorphous silicon (a-Si) PV cells, the highest performance was realized by introducing the *p-i-n* structure. M. Hossain [25] simulated a CdS/CdTe solar cell with *i*-CdTe layer that improved efficiency to 26.74%. These successes mean the efforts to improve further device performance, and have shifted towards surface physical phenomena, mainly the passivation of surfaces and interfaces. Therefore, in this paper, the lack of interface engineering approach to CdTe will be discussed using sputtered CdO nanolayer. CdO is attracting tremendous attention due to its interesting properties like direct band gap of 2.3 eV [26]. We have found that among metal oxides, high electron mobility of CdO satisfies the essential requirements for a low resistance and high infrared transmission transparent electron layer. We assume that the electron affinity of the CdO film (4.5 eV) is one of the key parameters that tune the device performance. Since the value of ΔE_c depends only by the nature of materials that form the heterojunction, the value of the ΔE_c will change if the new n-window material is applied and, in the case of CdO, equal with −0.1 eV. The $\Delta E_c = -0.1$ eV means there is no barrier against the photo-generated current and the value of the short circuit current density (J_{sc}) is

mainly determined by the band gap of CdTe and is independent of ΔE_c value. A new wider thin band gap material, CdO on the traditional CdS window layer will improve the value of the J_{sc} of CdTe solar cells more than the value of the open circuit voltage. Also, due to the CdO large static dielectric constant (ε_o = 21.9), it has very high electron mobility because of reduced electron scattering through efficient screening of coulomb potentials of ionized donors. The low electrical resistivity of CdO thin films and high electron concentration of 10^{20} cm^{-3} allow high transmittance up to >1200 nm [26].

2. Fabrication Processes and Characterization Methods

The CdS/CdTe heterojunctions were prepared by successive deposition of CdS and CdTe thin films by close space sublimation method onto glass substrates (2 × 2) cm^2 covered with a transparent (~90%) conducting (~10^{-3} Ω·m) ITO layer. For CdS and CdTe thin films deposition, CdS and CdTe *powders* 99.999% purity were *purchased from Alfa Aesar*, Germany. The effects of the source and substrate temperatures on the structure and electrophysical parameters of CdS and CdTe layers were studied to determine the optimum temperatures: T_s = 580˚C and T_{sub} = 390˚C for CdS and T_s = 535˚C and T_{sub} = 450˚C for CdTe. The CdS layer obtained in the optimal technological growth conditions had the thickness of 0.45 μm and the electron concentration of 1.6 × 10^{18} cm^{-3}. The CdTe thin film had the thickness of 10.8 μm and the hole concentrations of 4.2 × 10^{14} cm^{-3}. CdO layers were prepared by DC magnetron sputtering of a cadmium target in an oxygen atmosphere at a direct current. For sample preparation, a Cd target of 99.99% purity was used in the sputtering process. The sputtering chamber was evacuated down to 2 × 10^{-5} mbar. The distance between the target and the substrate was kept constant at 3 cm. The magnetron discharge was done in an O_2 atmosphere via independent mass-flow controller. The working total pressure was kept at 5 × 10^{-3} mbar. The substrate temperature for deposition of CdO thin films was about 90˚C. The CdO layers thickness were controlled by adjusting the deposition time and determined from the calibration curve of the dependence of the CdO layer thickness on the sputtering duration. In all performed experiments the deposition rate was calculated using the dependence of the thickness layer on the deposition time. The CdO film deposition rate was 5 Å/s. At an optimum total pressure of 5 × 10^{-3} mbar, the CdO films were polycrystalline and nearly stoichiometric with Hall mobility of 51 cm^2/V·s, carrier concentration of 1.5 × 10^{19} cm^{-3}, with an average optical transmittance of 85% in the wavelength (400 - 1200) nm region and with a value of the band gap of 2.48 eV. The deposited CdO layer encloses the surface of the CdS layer, smoothers the surface relief and helps block impurities diffusion from CdS in the CdTe layer [27]. Using the optimized growth parameter determined for the individual layers, two different heterostructures (HJs) were prepared: TCO/CdS/CdTe and TCO/CdS/CdO/CdTe. Both devices were subjected to postdeposition chemical $CdCl_2$ treatment in a saturated solution of $CdCl_2$ in methanol on the CdTe surface, fol-

lowed by thermal annealing in air for 30 min at 400˚C temperature. For chemical treatment the $CdCl_2$ powder 99.999% purity was used from Alfa Aesar, Germany. Then, with the aim of illustrating the application of these HJs, solar cell devices were fabricated with both structures by adding a Ni back contact evaporated onto the CdTe surface [26]. Before the deposition of the absorbing layer, a phlogopite mica mask was applied to cover the half of the CdS surface for the deposition of CdO before the deposition of the CdTe (**Figure 1**, left part).

The structure grown in this way, made it possible to obtain two types of structures in a single cycle and measure them separately, despite the fact that all stages of the fabrication were identical.

The surface morphology of the films and chemical composition were investigated using the scanning electron microscope (SEM VEGA TESCAN TS 5130 MM) coupled with energy-dispersive X-ray spectroscope (EDX, INCA OXFORD instruments). The acceleration voltage was 15 kV. AFM studies were performed using the SmartScan™ program with the XE-7 AFM System (Park Systems Corp., Korea) under room temperature. The surface topography images of samples were taken with a piezo scanner and recorded for 5 μm × 5 μm and 10 μm × 10 μm areas. The scanning process was conducted in the tapping mode with a 1 Hz scanning rate. A parabolic diamond cantilever with a radius of curvature approximately 10 nm, a normal force constant of 40 N/m was used for fitting. All analyses, including topography and surface roughness were performed using the XEI-7 Image Processing Program. The device performance was tested with conventional dark/light current-voltage (J-V) characteristics using a standard light source equivalent to AM1.5 (100 mW/cm^2), 300 K. The temperature dependent J-V and capacitance-voltage (C-V) characteristics of TCO/CdS/CdTe and TCO/CdS/CdO/CdTe photovoltaic devices were measured with a KEITHLEY 2400 Source Meter, at frequency of 1 MHz, a.c. amplitude of 30 mV and DC bias scanning from −1.0 V to 1.0 V. The admittance spectroscopy measurements

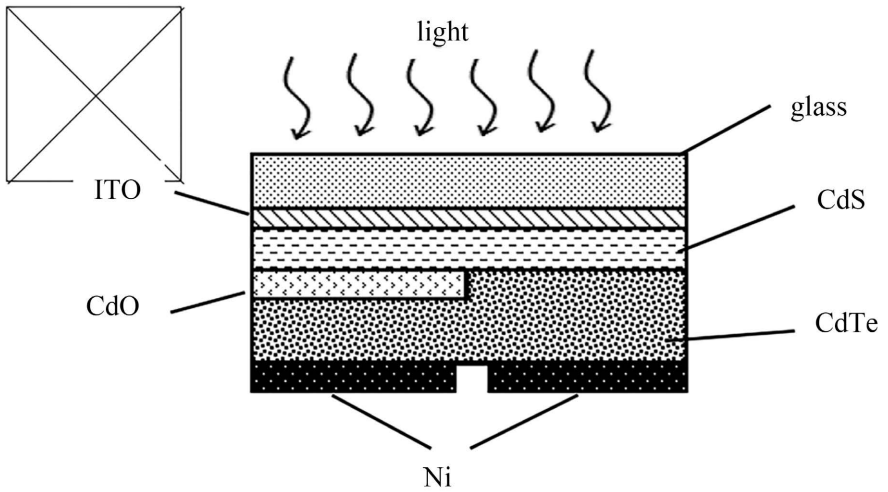

Figure 1. The cross section of a CdS/CdTe photovoltaic device with and without interfacial CdO nanolayer.

(TAS) were performed at temperature varied from 20 K to 320 K with temperature step of $T = 10$ K, using a Wayne Kerr 6500B impedance analyzer. The electrical impedance Z and phase angle of the devices were measured as a function of same temperature interval, frequency—varied from 20 Hz to 10 MHz and AC voltage kept as low as 30 mV, to reduce the background noise. Dark measurements were performed at a DC bias of 0 V. The density of the deep states in CdTe absorber and at the related interface was determined from the demarcation energy concept, as a derivative of the capacitance, according to the model described in [28].

3. Results and Discussion

3.1. AFM and Morphology Studies

The literature investigation shows, that surface and interface in CdTe photovoltaic devices play an important role in the determining of the solar cell efficiency. The morphological characteristics of the CdS thin film were investigated by AFM and SEM. It has been revealed that the morphology of CdS films has a considerable impact on their overall properties. This was especially noted in the devices, wherein the surface roughness and grain boundaries affected the recombination in the films. The 3D AFM image topography was used to investigate CdS topography on different substrates. In **Figure 2**, 3D AFM images of CdS on glass, on CdTe thin film, on CdTe/CdO interface and CdO on CdS thin film are presented.

The surface of all samples reveals a distinct distribution of grains with a uniform granular topography. The surfaces consist of hundreds nano-sized grains when CdS deposited on CdTe and CdTe/CdO, and the root mean square roughness (S_q)

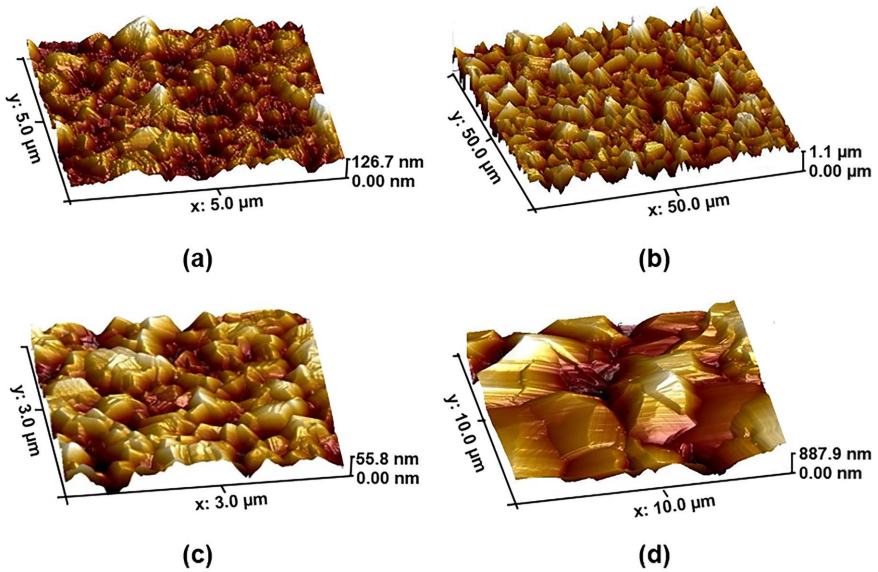

Figure 2. The AFM topography of CdS thin film surfaces on glass substrate (a), on CdTe thin film (b) and on CdTe/CdO interface (c). The AFM of CdO nanolayer surface deposited on CdS thin film (d).

of the deposited CdS thin films was 284 nm and 222.4 nm, respectively, which indicates the formation of smooth and well-connected grains on the film (Table 1). When CdS is deposited on glass and CdO on CdS, the values of S_q are 31.1 nm and 29.3 nm, respectively. A low influence on S_q was found for CdS and CdO samples in comparison with CdS deposited on CdTe and CdTe/CdO surfaces. The same situation is observed and for the average surface roughness (S_a). For all films, skewness (S_{sk}) shows negative values that specify more valleys than peaks, and the surface is more planer. We point out that, when CdS is deposited on glass and CdO on CdS, the films surfaces are more homogenous and flatter. This can be explained by an antireflection effect of the CdO layer. As the refractive index of CdO is about 2.5, of CdS is 2.4 and of CdTe about 3.0, there is better matching of the refractive index at the air/CdS/ CdO/CdTe interfaces (S_q = 29.3 nm) compared to the air/CdS/CdTe interface (S_q = 284.0 nm). Moreover, after CdO nanolayer deposition, additional interference fringes in the CdO appears in the CdTe absorption (300 - 1200 nm) region due to the flat CdO on CdS interfaces, which can impact the light intensity in the bulk of the absorber. Moreover, method for interfacial defect passivation could change the interface morphology and modify recombination rate, one would expect higher recombination for a rough interface (S_q = 284.0 nm) rather than a smooth interface (S_q = 29.3 nm).

We conclude that the surface morphology of the films is influenced by both, the nature of the substrate and CdO on CdS provoked a decreasing of the surface roughness.

The literature analysis suggests that an intrinsic interlayer formed at the interface suppress the surface recombination [29]. Figure 3 displays a plain view SEM image showing the morphology of CdO on CdS surface (a) and a cross-section of a CdS/CdO/CdTe heterostructure (b). After the deposition of CdO thin film of about 8 - 11 nm on the CdS, the surface became more homogeneous. The deposited CdO layer encloses the surface of the CdS layer, smoothers the surface relief and helps block impurities diffusion from CdS in the CdTe layer. The SEM cross-section image of CdS/CdO/CdTe heterostructure (Figure 3(b)) shows the big grains for CdTe that not densely packed.

Also, voids and a non-uniformity of the CdS and CdTe films thickness at the

Table 1. The AFM surface parameters of CdS on different substrates and CdO on CdS surface.

Samples	S_q, nm	S_a, nm	S_{sk}	D, μm
CdS on glass substrate	31.81	30.89	−1.201	0.272
CdS on CdTe thin film	284.00	266.10	−1.196	1.342
CdS on CdTe/CdO thin film	222.4	208.3	−1.337	1.128
CdO on CdS thin film	29.3	27.5	−1.326	0.254

The root means square roughness—S_q, The average surface roughness—S_a, Skewness—S_{sk}, Bearing Mean diameter—D.

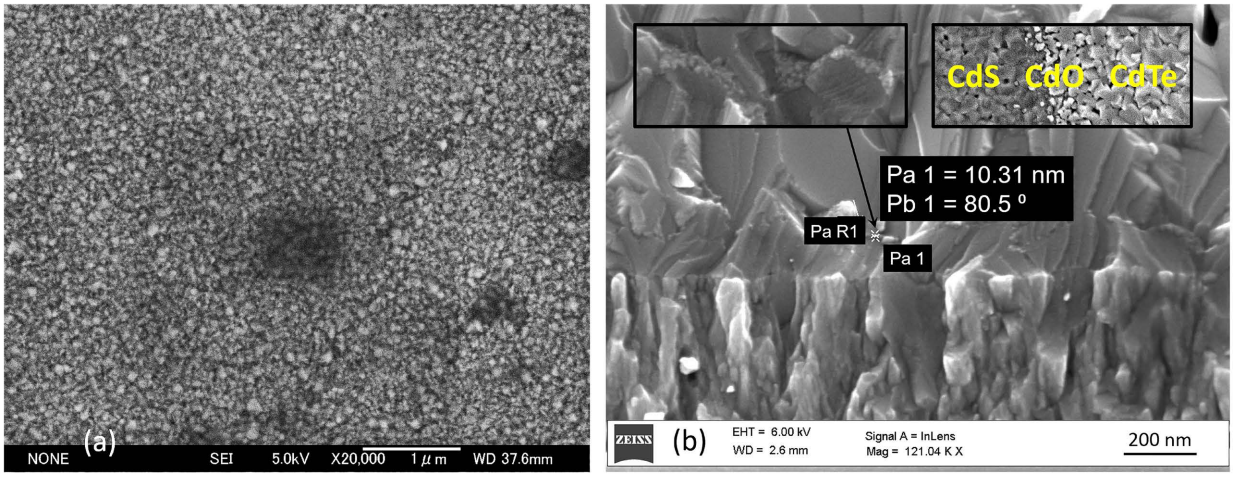

Figure 3. The SEM image of CdO deposited on CdS (a) thin film and cross-section image of TCO/CdS/CdO/CdTe structure (b). The insets in cross-section image of a CdS/CdO/CdTe heterostructure present the non-uniform accumulation of CdO at the interface.

interface are observed. The cross-section inset confirms the non-uniform accumulation of CdO at the interface of CdS/CdTe. The presence of the void's at CdS internal surface (**Figure 3(b)**) indicates that the CdO penetrate within the voids and reduce the imperfections on its surface. The evolutions of the elemental distribution across the depth of CdS/CdTe and CdS/CdO/CdTe devices are shown in **Figure 4**.

The EDX elemental distribution profiles of both CdTe devices show the Cd-L, Te-L, S-K lines. The EDX signals of Cd (Lα1) and S (Kα1) at 3.1 eV and 2.3 eV were observed. In addition, CdS/CdO/CdTe devices show O-K line (yellow) at 0.5 eV. The results of EDX line scans of cross-section of the CdS/CdO/CdTe device show non-uniform distribution of Cd-L (blue) and Te-L (green) lines in the elemental profile compared to CdS/CdTe heterostructure, where distinct regions can be seen. The image of CdS/CdO/CdTe device reveals complex interfacial chemistry, with a bilayer in place of the CdS. CdO film on the CdS layer suppresses the S interdiffusion from CdS into CdTe film and prevents the formation of solid solution with a lower bandgap that results in poor quantum efficiency.

3.2. The Impact of Sputtered CdO Nanolayer on Device Performance

The J-V characteristics for the best SnO_2/CdS/CdTe and SnO_2/CdS/CdO/CdTe devices under 100 mW·cm^{-2} illuminations, 300 K are shown in **Figure 5(a)**.

The photovoltaic parameters, the fill factor (FF), short circuit current density (J_{sc}), open circuit voltage (V_{oc}) and the efficiency of the conversion (η), estimated from these dependencies are presented in **Table 2**. Comparison of the photovoltaic parameters of solar cells based on CdTe revealed that solar cells with *i*-layer are the best. To further show the utility of *i*-CdO approach on short circuit current density, FF and open circuit voltage, a number of nine CdS/CdTe structures with different thicknesses of CdO insulating layer were compared. According to

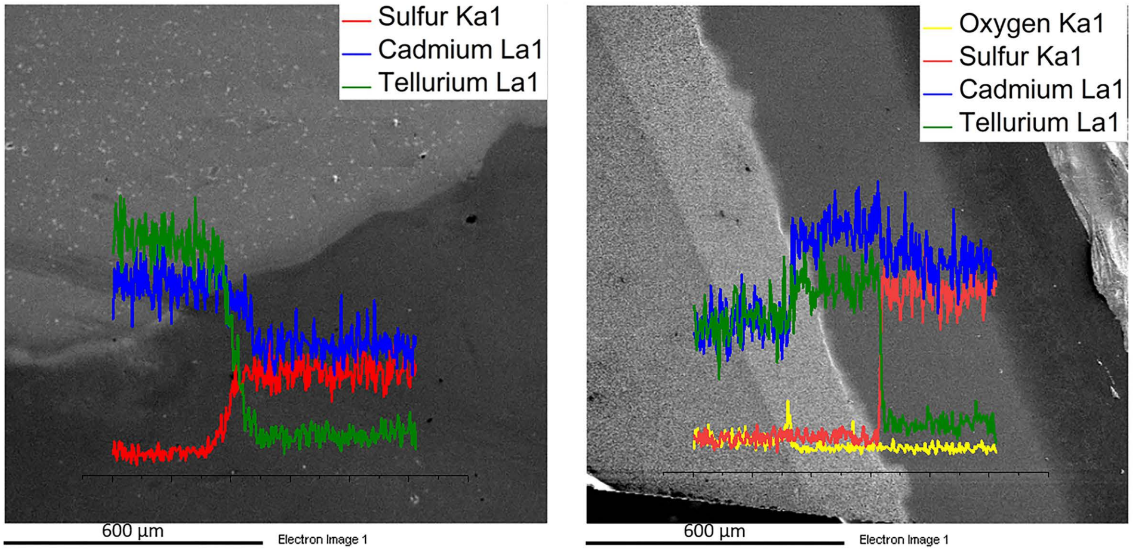

Figure 4. EDX line scan of cross section of Cd, S, Te and O profile, CdS/CdTe, (left), CdS/CdO/CdTe (right).

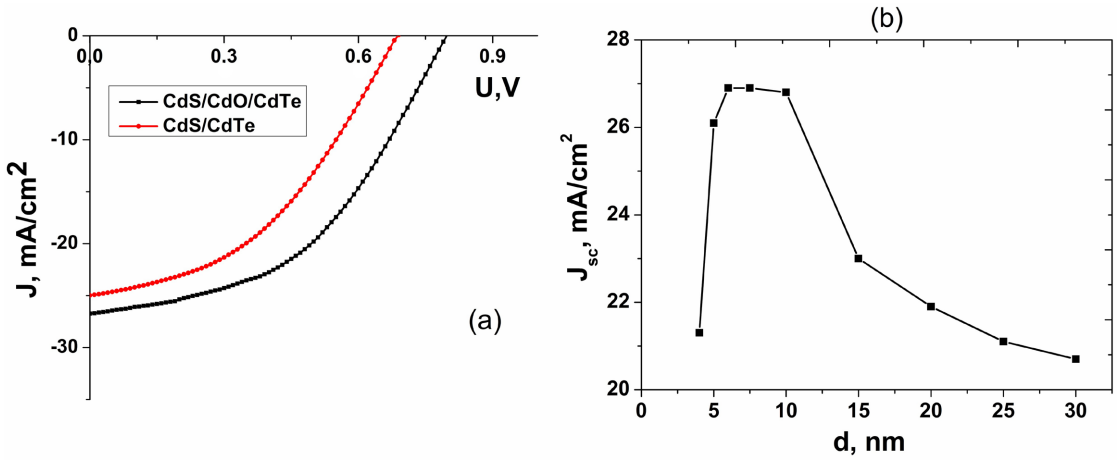

Figure 5. The J-V characteristics of the CdS/CdTe and CdS/CdO/CdTe heterostructures under 100 mW/cm^2, 300 K (a) and dependence of J_{sc} in function of the CdO insulating layer thickness (b).

Table 2. The photovoltaic parameters of CdS/CdTe and CdS/CdO/CdTe devices.

Samples	V_{oc}, V	J_{sc}, mA/cm^2	FF	η, %	$R_s \times 10^2$, Ω·cm^2	$R_{sh} \times 10^3$, Ω·cm^2
CdS/CdTe	0.69	24.9	0.44	7.5	8.8	0.54
CdS/CdO/CdTe	0.80	26.8	0.55	11.6	1.1	0.5

Figure 5(b), for a thicker *i*-layer than 11 nm, J_{sc} decreases because degrades the drift electric field for carrier transport.

Through the theoretical analysis it is shown that the insertion of a thin insulating layer between the two semiconductors of an n^+-p structure improves the efficiency in the same way as for a metal-insulator semiconductor (MIS) solar cell, if the discontinuity in the conduction bands constitutes a barrier for excited electrons. In our devices, the CdO interfacial layer with thickness greater than 11

nm modifies the morphology and composition of CdS and either plays no role or is disadvantageous.

For the open circuit voltage (Figure 6(a)), a sharp increase is observed at 5 - 11 nm thicknesses of the CdO layer and at thickness greater than 11 nm, it remains constant at 0.79 V. From these dependencies, for *p-i-n* heterojunction devices it follows that the optimal thickness of *i*-CdO is between 8 nm and 11 nm. It can be assumed that when CdO is too thin, it acts as a tunneling layer for the current, while when it is thicker, it acts as a blocking layer. So, sputtered *i*-CdO nanolayer as an interface engineering approach led to an enhancement of both J_{sc} and V_{oc} by 5% and 25%, respectively. The series (R_s) and shunt (R_{sh}) resistances in this paper were calculated from the line slope of the J-V curves at the open-circuit voltage and short-circuit current points, respectively. The values of the R_s for both CdS/CdTe and CdS/CdO/CdTe devices are equally with 8.8×10^2 $\Omega \cdot cm^2$ and 1.1×10^2 $\Omega \cdot cm^2$, respectively, while the shunt resistances reached the values of 0.54×10^3 $\Omega \cdot cm^2$ and 0.5×10^3 $\Omega \cdot cm^2$. The R_s value for CdS/CdO/CdTe device was decreased. The R_{sh} value for both devices has about the same value and smaller than of the series resistance because of the non-idealities, mainly impurities near the p-n heterojunction, which cause partial shorting of the heterojunction.

Low shunt resistance causes power losses in the photovoltaic devices by providing an alternate current path for the light-generated current. Such a diversion reduces the amount of current flowing through the photovoltaic device junction and reduces the voltage. The low values of shunt resistance usually result from manufacturing defects.

Analysis of the dark current-voltage characteristics (Figure 6(b)) show that the introduction of *i*-CdO nanolayer between the CdS and CdTe layers leads to a shift in the I-V curves but not of the changing of the current transport mechanism. The built-in voltage increases from 0.51 V to 0.65 V but the reverse saturation

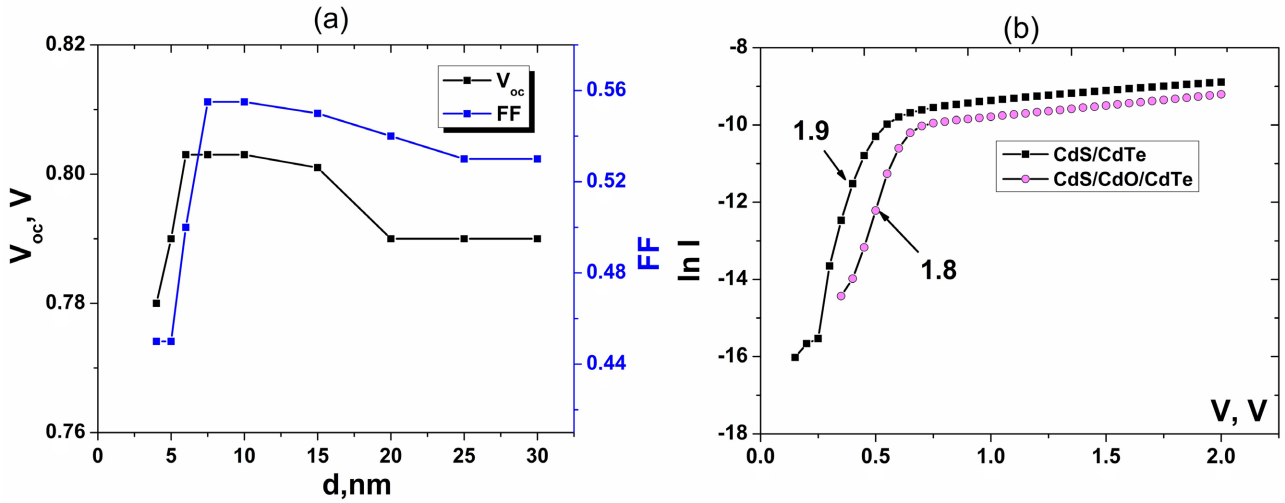

Figure 6. Dependencies of V_{oc}, FF parameters of CdS/CdO/CdTe devices in function of the CdO insulating layer thickness (a) and the dark I-V characteristics of CdS/CdTe and CdS/CdO/CdTe heterojunctions at room temperature (b).

current decreases from 7.5×10^{-10} A to 1.5×10^{-10} A. The increase in the built-in voltage of the devices with *i*-CdO nanolayer is due to the change of the work function of the n-doped electron transport layer. Finally, we can conclude that the same model current mechanism can be applied for both CdS/CdTe and CdS/CdO/CdTe heterojunctions solar cells as the diode quality factor is $n = 1.9$ and $n = 1.8$, respectively. The decrease of n by 0.1 for CdS/CdO/CdTe solar cell is indication of the enhancement of open circuit voltage and current density values, with 0.11 V and 1.9 mA/cm^2, respectively. It is therefore suggested that the recombination mechanism of CdS/CdTe photovoltaic cells is primarily SRH mechanism, achieved by deep trap states in space charge region of CdTe. The energy level can provide both electrons and holes. When n varies from 1 to 2, defects play the role of deep trap level. When the change of n is getting closer to 1, the recombination mechanism begins to fall in inter-band recombination, mostly in the neutral region. Surface recombination will make the change of n value more than 2. The recombination at grain boundaries should also be considered, causing the loss of carrier collection and reducing the voltage value. At the CdS/CdTe interface, there is a 9.7% lattice mismatch between the cubic CdS and the cubic CdTe. Such a high lattice mismatch causes considerable defects at the CdS/CdTe interface. Therefore, both devices exhibit SRH recombination as the dominant current transfer mechanism across the interface because the large conduction (ΔE_C = (0.23 … 0.3) eV and valence (ΔE_C = (0.67 and 0.74) eV bands offsets block thermal currents [30]. ΔE_C is a vital factor affecting carrier transport and recombination.

To identify the nature of traps from J-V-T measurements, we briefly present analysis of the dark J-V-T characteristics. **Figure 7(a)**, **Figure 7(b)** presents the Arrhenius plots of the saturation current density (J_s) of both devices, measured in the temperature range of 173 K - 331 K. The temperature dependencies revealed in **Figure 7(a)**, **Figure 7(b)** by the slopes of Arrhenius plots provide useful insight into the presence of two defect levels for CdS/CdTe and one defect

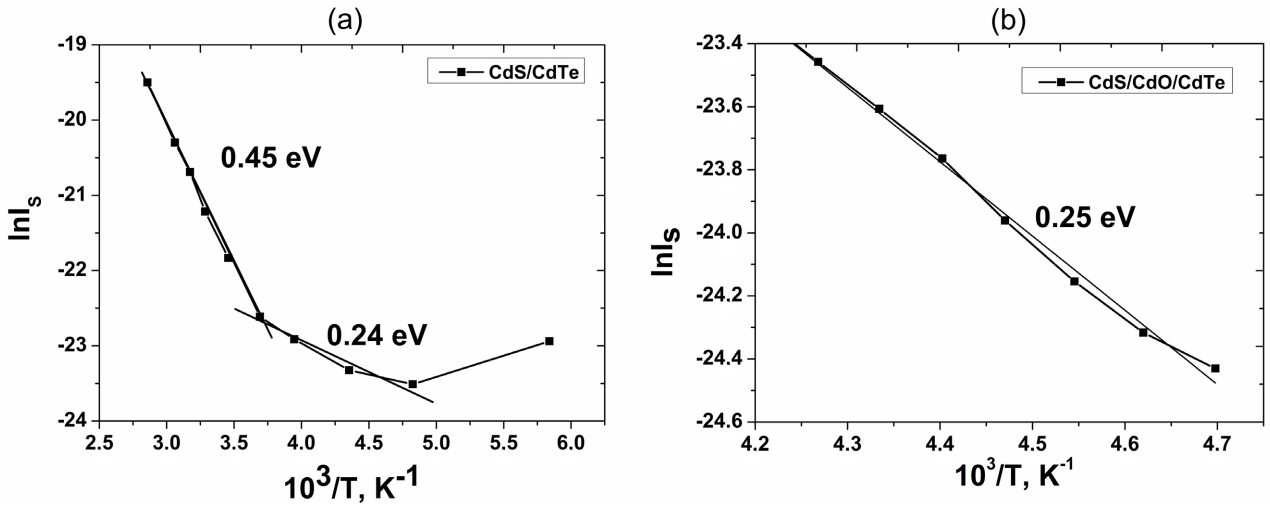

Figure 7. The saturation current density dependency on 1000/T for CdS/CdTe (a) and for CdS/CdO/CdTe devices (b).

level for CdS/CdO/CdTe devices. By analysis of J_s evolution with reciprocal temperature, we distinguish regions where J_s changes were fitted by linear function. In both CdS/CdTe and CdS/CdO/CdTe devices, in the lower temperature region of J_s, the defect level with activation energies of 0.24 eV and 0.25 eV was revealed, while in the higher J_s temperature region of CdS/CdTe, device a defect level with activation energies of 0.45 eV is depicted.

The saturation current density reveals that their changes with temperature in CdS/CdTe device follow the rule of recombination as a dominant carrier transport mechanism, via the defect levels located at 0.45 eV and 0.24 eV above the valence band edge of CdTe, while in the CdS/CdO/CdTe device only via the defect level located at 0.25 eV. Therefore, to gain better understanding into the carrier density and deep defects in the CdTe absorber, as well as, the effect of possible defects at the heterojunction interface for the devices with and without CdO interface nanolayer, CV and TAS measurements were conducted. The CV and TAS results were compared only for the reference CdTe/CdS device (*i.e.*, without CdO interface layer) and for the best cell, employing an 8 - 11 nm thick CdO interface nanolayer.

3.3. Carrier Concentration and Defect Density in CdTe Absorber

There are three main interfaces for CdTe thin-film photovoltaic devices: TCO/CdS interface, CdS/CdTe interface, and CdTe/Ni interface. As the main p-n junction of CdTe thin-film photovoltaic devices, the CdS/CdTe interface depletion region is the key in photoelectric conversion of CdTe thin film photovoltaics, and is the core of the entire device. To understand the J_{sc} and V_{oc} CdS/CdTe photovoltaic devices improvements by engineering of very thin insulating CdO wide-bandgap semiconducting material presented in previous paragraph, J-V-T and C-V measurements at different temperatures has been applied to both CdS/CdTe and CdS/CdO/CdTe devices. Also, admittance measurements C-ω-T give information on the widths of the space charge region of the device and on the contribution of trap levels to the capacitance of the device. High-frequency and low-temperature value of capacitance provide the total width of the depletion region, while the low frequency—the depletion width diminished by the response of traps, which are fast enough to respond to the AC signal of the admittance meter [26]. From bulk capacitance we extract the depletion layer width and the apparent free carrier density according to the equations: [30]

$$w = \frac{\varepsilon A}{C}, \tag{1}$$

$$N(W) = -\frac{2}{q\varepsilon A^3}\left[\frac{\mathrm{d}\left(1/C^2\right)}{\mathrm{d}V}\right]^{-1} \tag{2}$$

where $\varepsilon = \varepsilon_o \cdot \varepsilon_r$, ε_r is the dielectric constant of CdTe, ε_o is the permittivity of free space, q is the electron charge, W is width of the depletion region, A is the area of the device. We assume a one-sided device, in which the dominant capacitance

response originates from the edge of the depletion region in the more intrinsic layer, and assumes that the temperature is high enough that the carriers can be rapidly transported into and away from the edge of the depletion region at the applied AC frequency. The application of DC bias (V) changes the value of the depletion width in CdS/CdO/CdTe device because at the interface appear a material with the relative permittivity ε different from of CdS and with a higher N_{CV} density concentration. Figure 8(b) shows $1/C^2 = f(V)$ for the CdS/CdO/CdTe structures at 100 kHz and 1 MHz frequencies. Evidently, from this figure, the (C^2-V) relation is generally nonlinear. However, each curve can be fitted approximately with a broken line consisting of one linear region. The slopes of the straight lines increase with frequency. The interception of the lower voltage straight lines with the voltage axis results in different values for the built-in voltage. As the N_{CV} density concentration is not constant throughout the depletion layer, the different values for the built-in voltage were obtained. The results from the experimental measurements listed in Table 3 show that at 0.1 MHz frequency the main charge carriers transport processes take place in the depletion region of (5.2 - 5.3) μm width for CdTe/CdS thin film devices. The CdO nanolayer passivates the shallow defects resulting in a higher N_{CV} density concentration at both low and higher frequencies and the carriers transport processes take

Table 3. Electrical parameters of of CdTe/CdS thin film photovoltaic device, without and with a CdO layer at the interface between CdTe and CdS.

Samples	0.1 MHz			1 MHz		
	V_{bi}, V	$N_{cv} \times 10^{13}$, cm^{-3}	W, μm	V_{bi}, V	$N_{cv} \times 10^{13}$, cm^{-3}	W, μm
CdS/CdTe	0.51	1.1	5.3	0.83	4.5	5.6
CdS/CdO/CdTe	0.58	3.8	5.0	1.02	5.3	4.7
CdS/CdTe	0.54	2.4	5.2	0.87	4.5	4.9

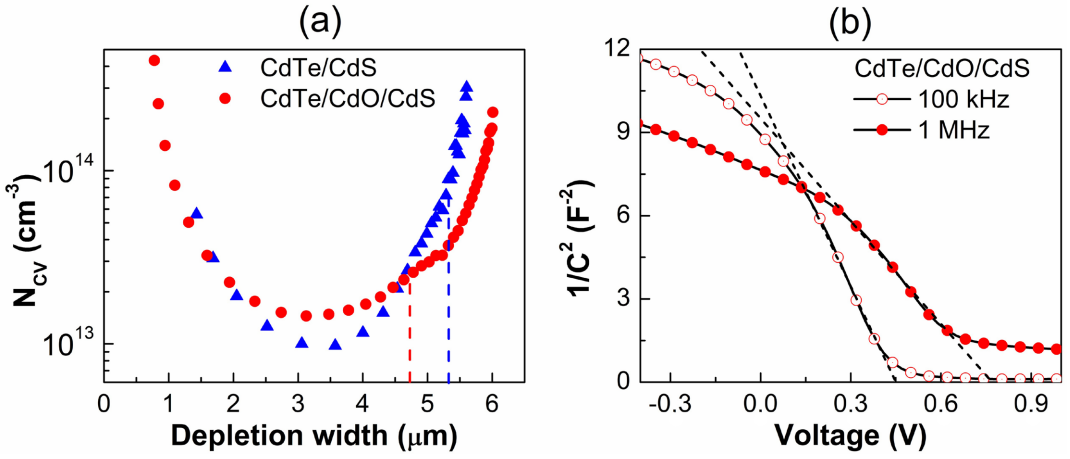

Figure 8. Depth carrier density profile versus depletion width of absorber films in CdTe/CdS and CdTe/CdO/CdS devices, calculated from capacitance-voltage (C-V) measurements (vertical dashed lines indicating 0 V) (a) and $1/C^2$-V dependence for/CdO/CdS best device measured at 100 KHz and 1 MHz, at 300 K (b).

place in the narrower depletion region of 4.7 μm width. If the depletion region width, at 1 MH_Z frequency, for one of the CdTe/CdS thin film device slightly increases but for another decrease, then for the device with *i*-CdO nanolayer for both lower and higher frequencies, the depletion region width decreases. A more interesting feature is with built-in voltages at 1 MHz, for both types of devices, the V_{bi} values are increased. An increase of about 0.5 V was observed in the case of the device with *i*-CdO nanolayer. It is well known that in a semiconductor, V_{bi} equals the potential difference across the depletion region in thermal equilibrium. In thermal equilibrium, no external voltage is applied to the device. Moreover, the Fermi energy is constant throughout the heterostructure and the built-in voltage equals the difference between the Fermi energies, respectively in the buffer and the absorber, divided by the elementary charge. **Figure 8(a)** presents the defect profiles that show the typical U-shaped form commonly reported in literature [31] [32], with a minimum at a profiling distance of 2.0 - 5.5 μm. Both profiles exhibit a significant increase in the defect profile toward the junction and toward the bulk of the sample. Trying to understand differences between the low frequency and high frequency profiles, it can be seen that the curves have an almost identical shape, but seem to be shifted by a distance.

An apparent depth dependence of the resulting doping concentration is often attributed to charge contributions of deep trap levels because their charge state depends on the band bending. The minimum N_{CV} densities concentration is in the range of ~9×10^{13} cm^{-3} to ~1×10^{14} cm^{-3} and increases toward negative bias voltages, that is, toward higher apparent depth within the CdTe. The N_{CV} densities were determined from the bottom of the U-shaped curve at zero bias. For the CdS/CdO/CdTe devices there is an observable increase in the N_{CV} density profile inside the device and a decrease of a value of the width in comparison with non-engineering of the interface devices. Also, when the depletion region enters the front and the back-contact regions, the N_{CV} concentration there rapidly rises. Another observation is a difference between the built-in voltages (V_{bi}). From one side, this suggests that performance degradation of CdS/CdTe without not-engineering interface can arise from lower N_{CV} density due to $CdCl_2$ treatment.

According to the previous investigation [33], $CdCl_2$ activation treatment is responsible for the formation of a V_{Cd} shallow acceptor complex, which leads to an increase in the doping densities in CdTe devices.

However, the excess of *Cl* can lead to the formation of self-compensating Cl_{Te} donors [34] [35]. This effect could explain the decrease in the N_{CV} density concentration which can be directly translated into the V_{OC} decreases, as presented previously. Through the deposition of *i*-CdO nanolayer when the device is reverse biased the majority charge carriers are stopped to push away from the junction and less ions are left at the junction. This beneficial situation reduced the available V_{Cd} (shallow acceptor centers) and the doping density of the CdS increases, which lead to an increase in V_{OC}. Since C-V technique gives information about the kinetics of carrier transport, then with AS, the characteristics of

the majority carrier trapping defects can be determined for solar cell materials and devices. If deeper carrier traps are present, the band bending in the SCR causes the Fermi level E_F to cross the trap level E_t at some distance from the interface, at the crossing point x_t shown in Figure 9.

An applied small AC voltage with the frequency $f = \omega/2\pi$ causes the electric charge accumulated by traps to oscillate in the vicinity of crossing point x_t. In the case of low frequency, the trap related capacitance is $C_t = C_{lf}$, where C_{lf} is the low frequency capacitance, while at high frequency measurements give the junction capacitance, *i.e.* depletion area capacitance $C_d = C_{hf}$, where C_{hf} is the high frequency capacitance. Accordingly, in the case of a single majority carrier trap level, the total junction capacitance can be described by the equation:

$$C_d + \frac{C_{lf} - C_d}{1 + \omega^2 \tau^2} \tag{3}$$

where τ is the characteristic trapping time that depends of the trap density N_t [36]. Figure 10 presents the C-f-T curves measured in the temperature range from 50 K to 320 K. The values of the capacitances for the device without *i*-CdO nanolayer are slightly smaller and temperature dependent in comparison with of the device with nanolayer at the interface.

The inflection frequency ω_o can be obtained from the analysis of the first derivative of the capacitance, $\mathrm{d}C/\mathrm{d}\omega$, which demonstrates a maximum at the frequency ω_o. A small AC oscillating voltage with the frequency 0.2 MHz causes the electric charge accumulated by traps to oscillate in the vicinity of this crossing point. The trapped electric charge follows the applied voltage oscillations and contributes to the total capacitance only if their frequency does not exceed the trap characteristic frequency ω_o. In the case of a small trap concentration N_t, the characteristic frequency ω_o for the charging and discharging of defect levels is $\omega_o = 1/\tau$ [37]. The temperature dependence of the inflection frequency ω_o is determined by the following equation [37]:

$$\omega_o(T) = 2e_t(T) = 2N_{C,V} v_{th} \sigma_{n,p} \exp\left(-\frac{E_A}{kT}\right) = 2\xi_0 T^2 \exp\left(-\frac{E_A}{kT}\right) \tag{4}$$

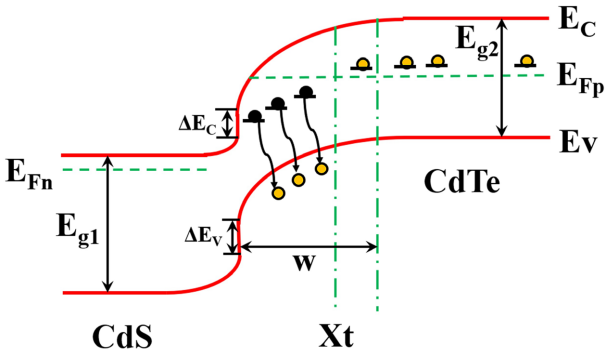

Figure 9. Energy band diagram of solar cell for reverse bias conditions (at $\tau = \infty$) consisting of a CdTe absorber with interface states and deep levels. The symbols represent their usual meanings.

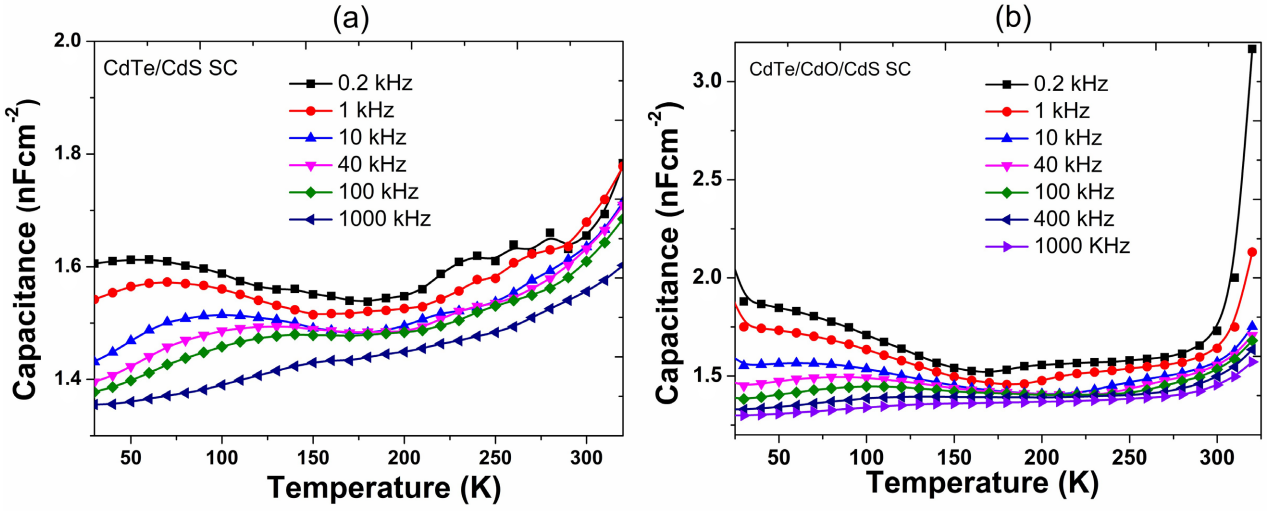

Figure 10. C-T-f curves of CdTe/CdS thin film solar cell, without (a) and with a CdO layer (b) at the interface between CdTe and CdS.

where e_t is the emission rate, $N_{C,V}$ is the effective density of states in the conduction and valence band, v_{th} is the thermal velocity of the minority carriers at the interface, $\sigma_{n,p}$ is the capture cross-section for electrons and holes, $E_A = E_t - E$ is the activation energy of the defect level E_t with respect to the band edge E, k is the Boltzmann constant, and ξ_0 covers all the temperature independent parameters [38]. The activation energy of a defect level E_A was obtained from the temperature frequency dependence of the capacitance spectra *i.e.*, from the Arrhenius plot of the quantity $\ln(\omega_o/T^2)$ versus $10^3/T$. From the Arrhenius plot of the $\ln(\omega_o/T^2)$ versus $10^3/T$ presented in **Figure 11** were estimated the activation energy of the defect levels. According to the TAS theory [38], the majority carrier to the frequency of the AC signal is limited by the modified dielectric relaxation frequency ($\omega_o = W/d \cdot \varepsilon_r \cdot \rho$), where ρ and ε_r are the material resistivity and relative permittivity, respectively, W is the depletion width, and d is the absorber thickness. For $\omega < \omega_o$, the CdTe in the quasineutral region behaves as a conductor with a bulk conductance, while for $\omega > \omega_o$, it behaves like a capacitor with a bulk capacitance. The extracted activation energies for CdS/CdTe are 0.43 eV and 0.20 eV.

Also, using admittance spectroscopy technique, authors of [39] [40] [41] [42] found a thermal ionization energy of 0.23(3) eV in CdTe attributed to the V_{Cd} defects, which is in good agreement with first principles investigations. In CdTe, Cd vacancies act as acceptors with two ionization energy levels, the first ionization state $V_{Cd}^{(0/-1)}$ and the second ionization state $V_{Cd}^{(-1/-2)}$ have been reported [43] [44]. The activation energy of 0.20 eV defect level could be located above the valence band maximum for both heterojunction devices. According to the theory, wide-band gap semiconductors show self-compensation, that is the spontaneous formation of acceptor-type intrinsic defects to compensate or passivate donor-type.

The $CdCl_2$ activation step is standard and vital process in fabricating high

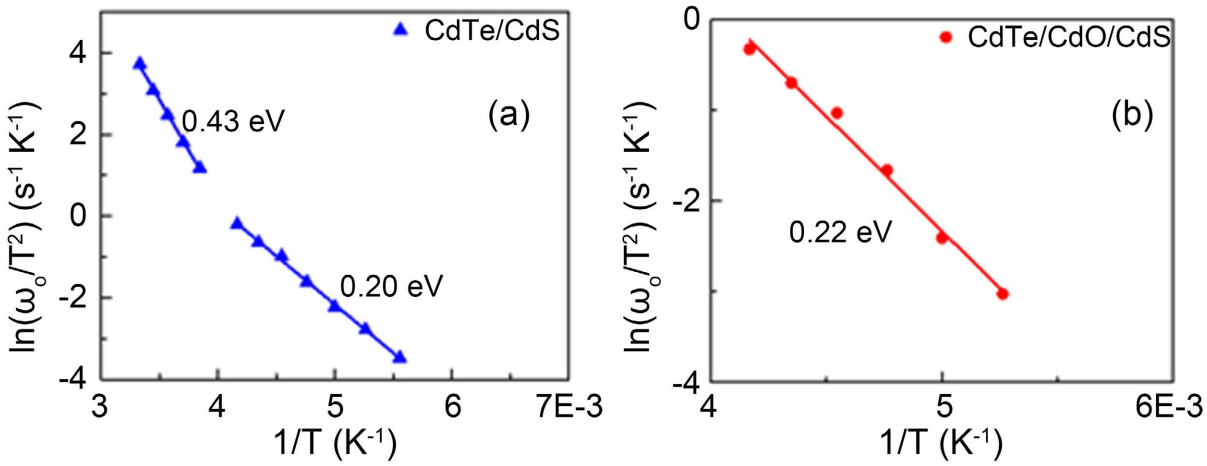

Figure 11. The Arrhenius plot of the $\ln(\omega_o/T^2)$ versus $1000/T$ of CdS/CdTe thin film solar cells, without (a) and with a CdO layer (b) at the interface.

efficiency PV devices. From a theoretical point of view, chlorine is predicted to promote further p-type doping of CdTe via a shallow donor Cl_{Te} defect with an ionization energy below the conduction band.

So, defect energies extracted from the admittance spectroscopy for CdS/CdTe devices (0.43 eV and 0.20 eV), CdS/CdO/CdTe (0.22 eV) and J-V-T (0.45 eV and 0.24 eV), (0.25 eV) measurements, respectively are in good agreement. The experimentally measured activation energies values from plot of capacitance transients and J-V-T techniques are in good agreement and therefore, we assume that the activation energy of 0.43 eV occurs due to the formation of cadmium vacancies V_{Cd} and acceptor complexes $V_{Cd} - Cl$, which continuously shift Fermi level towards valence band and decrease resistivity. Several publications [45] [46] [47] have been reported a deep trap in the range 0.43 - 0.54 eV above the valence band maximum [48] [49] [50] [51]. These experimental values are in good agreement with our value highlighted by TAS measurements in CdS/CdTe device without interface engineering and belonging to the complex $(Cl_{Te} - V_{Cd})^{-1}$ that consists of a Cl_{Te}^{+1} impurity and a V_{Cd}^{-2} defect that are below to acceptor $(Cl_{Te} - V_{Cd})^{-1}$ complex (AX-center).

Taking into account the activation energy values of 0.43 eV and 0.20 eV presented in **Figure 11** and assuming the energy diagram of CdTe for the CdS/CdTe device presented in **Figure 12**, the energetic position of these two defects 0.43 eV (AX-center) and 0.22 eV (acceptor-like defect) are situated in the space charge region. The analysis of the current-voltage characteristics in the higher and lower temperature regions of CdS/CdTe device indicates the presence of the traps with activation energy of 0.45 eV and 0.24 eV, respectively and is assigned to the recombination process as a dominant current flow mechanism. For the device with CdO insulating layer at the interface, the only a trap with activation energy of 0.25 eV was revealed. The identified traps act as a recombination centers for electrons. The TAS investigation revealed the same deep levels in CdS/ CdTe and CdS/CdO/CdTe photovoltaic devices, among which the most dominant

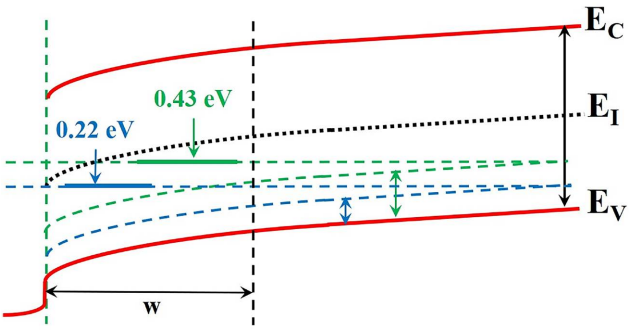

Figure 12. Schematic of the assumed energy diagram of CdTe layer in the CdS/CdTe heterojunction device.

was a trap with an activation energy of 0.20 eV and 0.22 eV. This defect has about the same value as energy states determined by J-V-T analysis. Based on the literature review and TAS system database, we assigned it to the formation of cadmium vacancies V_{Cd}. This obviously confirms that V_{Cd} defects act as a recombination center and, therefore, have a significant impact on the current flow mechanism in the low temperature region.

The engineering of interface of the CdS/CdTe heterostructure with CdO thicknesses about 8 - 11 nm "kills" the deep $(Cl_{Te} - V_{Cd})^{-1}$ AX-center and improve both J_{sc} and V_{oc} parameters, but keeps the defect with the activation energy values of 0.20 eV and 0.22 eV in both CdS/CdTe and CdS/CdO/CdTe devices.

In summary, we can assume that the concentration of free charge carriers is determined by the vacancies of cadmium V_{Cd} defects with activation energies of 0.20 eV (CdS/CdTe) and 0.22 eV (CdS/CdO/CdTe) devices that agree well with values of the publications [51] [52] [53]. The typical dopant concentrations are ~10^{14} to 10^{15} cm^{-3} for polycrystalline CdTe which is limited by the number of V_{Cd} present in CdTe [54]. The CdS/CdTe interface is one of the critical device regions in CdTe photovoltaic devices and its properties are not clearly understood at this time, and influence on device stability still unknown.

4. Conclusions

In this paper, we demonstrate that engineered nanometer CdO thin films grown by DC magnetron sputtering is an effective interface-passivation strategy for improving CdTe photovoltaic device performance. The CdO film deposition rate was 5 Å/s. The TCO/CdS/CdTe/Ni and TCO/CdS/CdO/CdTe/Ni photovoltaic devices were fabricated by CSS method under optimized fabrication conditions.

The photovoltaic parameters, such as fill factor, the short circuit current density, the open circuit voltage and the energy conversion efficiency estimated from J-V dependencies under illuminations of 100 mW/cm^2 for the n-CdS/p-CdTe heterostructure are 0.44, 24.9 mA/cm^2, 0.69 V and 7.5%. A CdS/CdTe photovoltaic device with insulating CdO interfacial layer showed power conversion efficiency of 11.6% with J_{SC}, V_{OC}, and FF of 26.8 mA/cm^2 0.80 V and 0.55, respectively. The enhancement of both J_{sc} and V_{oc} by 5% and 25%, respectively is observed.

Analysis of the C-V-T measurements shows an observable increase in the N_{CV} density profile inside the CdS/CdO/CdTe device, a difference between the built-in voltages from 0.83 V to 1.02 V and a decrease of a value of the width from 5.6 μm to 4.7 μm compared to device with non-engineered interface. In addition, after interface engineering via sputtering of CdO nanolayer the removal of the fast recombination deep $(Cl_{Te} - V_{Cd})^{-1}$ AX-center forming during $CdCl_2$ thermal treatment had place.

Further improvement of the efficiency in CdS/CdO/CdTe devices requires the elimination of the defect with the activation energy around 0.20 eV. For further improvement of CdS/CdTe solar cells efficiency we propose at the back contact to use the material with the high work function, such as graphene, that can also reduce interface carrier recombination. Band alignment measurements using photoelectron spectroscopy and synchrotron techniques will be included in the investigation of CdS/CdO/CdTe devices with contact of graphene to CdTe layer.

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Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

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