Journal of Power and Energy Engineering, 2021, 9, 93-103
https://www.scirp.org/journal/jpee
ISSN Online: 2327-5901
ISSN Print: 2327-588X

Design of Traffic Light Based on Field Programmable Gate Array

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How to cite this paper: Zhao, L. (2021) Design of Traffic Light Based on Field Programmable Gate Array. *Journal of Power and Energy Engineering*, **9**, 93-103.
https://doi.org/10.4236/jpee.2021.95006

Received: April 6, 2021
Accepted: May 24, 2021
Published: May 27, 2021

Abstract

The use of fixed-time traffic lights for road traffic control has the disadvantage of low traffic efficiency. In order to optimize the vehicle traffic at the intersection, this paper proposes a design scheme of a real-time control system for road intelligent traffic lights based on FPGA. The system adopts the polling control model, the vehicle detector detects the arrival rate of vehicles, and obtains the corresponding traffic light green time length according to the traffic rules and polling model theory. Using Altera's Cyclone IV series EP4CE15E22C8 chip as the development platform, a specific design plan is given. The circuit mainly includes program-controlled amplifier module, AD acquisition module, cross-correlation calculation module, serial port transmission and Lab-VIEW module. The system can realize the intelligent adjustment of traffic lights. Different vehicle arrival rates are detected at different times, so that the corresponding traffic light configuration time length changes accordingly. This intelligent adjustment controls road traffic and makes the main and branch roads coordinate and cooperate, thereby improving the traffic efficiency of the intersection.

Keywords

FPGA, Intelligent Traffic Lights, Clock Division, Polling Model

1. Introduction

With the rapid development of my country's economy, the number of vehicles owned has also increased sharply. Coupled with the expansion of the population, the problem of urban traffic congestion has become increasingly prominent [1]. How to make the control of traffic lights more reasonable and maximize the effectiveness of existing traffic resources has become a common concern for city managers and scientific and technological workers [2]. Therefore, a circuit de-

sign with higher flexibility, reliability and scalability can better alleviate traffic pressure, and can realize emergency treatment of emergencies [3]. At this stage, there are still many cities in China that use the second-generation timed traffic signal control technology, relying on historical data and experience to determine the signal cycle and green signal ratio of a single signal, and automatic control by computer technology [4] [5] [6]. This technology takes into account the dynamic change characteristics of traffic flow to a certain extent, but the setting data needs to rely on the results of long-term observation, and because the setting mode is fixed, its service level is not high, and it is quite effective in dealing with traffic accidents or cross-peak hours [7] [8].

In order to solve this problem, the intelligence transportation system (ITS) came into being. The intelligent transportation system comprehensively applies various advanced science and technology to the transportation system, which can greatly alleviate the traffic pressure in real life, reduce traffic accidents, and increase the traffic rate of vehicles [9]. Traffic lights are an indispensable and important tool in modern traffic control [10]. At present, the technology for realizing traffic light control is relatively mature, and there are many design research schemes [11] [12]. This article is aimed at students who are beginning to learn digital circuits and uses FPGA technology to design traffic lights [13]. Compared with traditional digital electronic design technology, FPGA technology has obvious advantages, mainly in the aspects of flexible design, high reliability, and fast working speed [14].

This manuscript introduces the design of a traffic light controller based on FPGA, which is written in Verilog HDL language and combined with Quartus II software for system design and debugging [15] [16] [17]. This design includes the main control module, power supply module, clock module, and LED display module, which realizes the design function and has a good acceptance effect [7]. Quartus II is Altera's comprehensive CPLD/FPGA development software, schematic diagram, VHDL, Veriloghdl and AHDL (Description Language supported by Altera Hardware) and other design input forms. Built-in own synthesizer and emulator. By combining with DSP Builder and MATLAB/Simulink, Quartus II can easily realize various DSP application systems. Support Altera Programmable System on Chip (SOPC) development, set system level design, embedded software development, programmable logic design in one, is a comprehensive development platform. Quartus II can realize timing/timing analysis and critical path delay analysis. Use Signal Tap II logic analysis tool for embedded logic analysis; Support the addition and creation of software source files, and link them to generate programming files [7] [18].

The vehicle detector detects the arrival rate of vehicles passing through the intersection [18]. According to the changing traffic flow information, the polling model is used to calculate the average waiting time of the corresponding vehicles. According to the traffic rules and polling theory, the average waiting time obtained is the traffic the length of the light's green time [19]. The programming

result is applied in the Quartus II software platform to adjust the traffic light duration in real time according to the detected different arrival rates, and finally realize the intelligent control of the traffic light. The purpose of this design is to detect the arrival rate of vehicles at different moments, so that the length of the corresponding traffic light configuration time changes accordingly, so as to intelligently regulate and control the road traffic, lead to the main and branch roads coordinate, thus improving the efficiency of the intersection.

2. Experimental Principle

The traffic light control circuit is an application circuit used at road intersections to control the red, yellow, and green traffic signal lights to turn on and off alternately in a prescribed time sequence. According to the requirements of the traffic rules: the red light is on and no traffic is allowed, the green light is on to allow traffic, and the yellow light is on to give the moving vehicles time to park outside the forbidden line. The traffic light control circuit designed in this article should make the red, yellow, and green lights turn on for 24 s, 4 s, and 20 s in a cycle. The output signal is displayed on LEDs and seven-segment digital tubes, of which 6 LEDs are used to indicate the red, yellow, and green lights on the north-south and east-west roads respectively, and the seven-segment digital tube is used to display the countdown before changing the lights. The block diagram of the traffic light control circuit is shown in Figure 1.

2.1. Traffic Light Control Rules

The traffic light control circuit integrates a combination circuit and a sequential circuit, and is mainly used to simulate the red, yellow, and green light changes and the countdown process at traffic intersections. The design includes three modules: clock frequency division, red-yellow-green state conversion, countdown display and decoding. The initial clock signal of this design is generated by the crystal oscillator in the experiment box. The crystal oscillator frequency is 1 Hz, that is, the timer period is 1 s, which is consistent with real life. The timer counts the time (seconds) of the traffic light. The timing module adopts a countdown mode. When the red light is on (take the north-south direction as an example), the timer starts counting down from 24, and decreases by 1 every time a clock signal comes. When the timer decreases to 1, the red light is off and the green light is on. The clock cycle required by the red-yellow-green state transition circuit is 4 s, so the external clock signal must be frequency-divided (Figure 2).

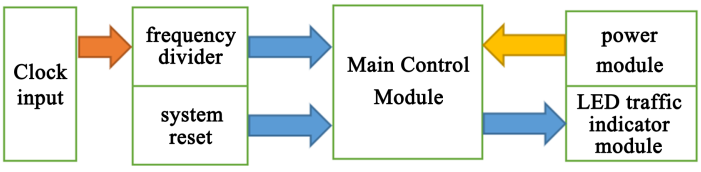

Figure 1. Block diagram of traffic light control circuit.

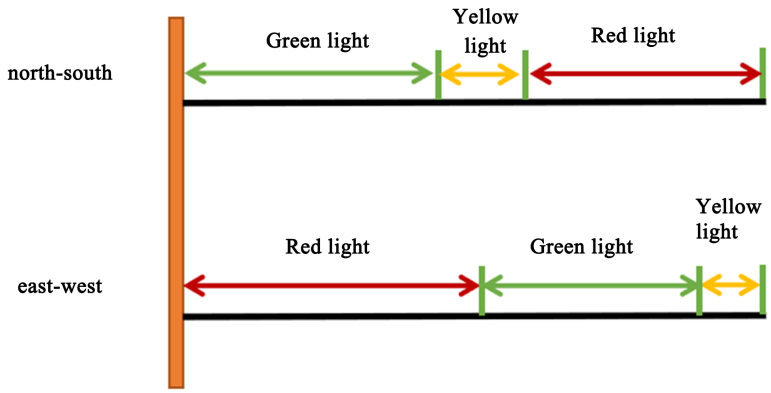

Figure 2. Traffic light system control rules.

2.2. Design Method and Realization

The system consists of three modules: clock frequency division, red-yellow-green state conversion, countdown display and decoding. The clock module is designed by VHDL language, and the other two modules are realized by means of schematic diagrams. After each module is completed, component symbols must be generated, and finally the overall circuit diagram can complete the design by calling three component symbols. This can make the final design drawing more concise.

2.3. Design and Implementation of Clock Divider Module

The clock module is realized by frequency division. The frequency divider is a basic unit with very high frequency used in FPGA design. According to the principle of the traffic light designed in this article, the yellow light is on for 4 s in a cycle. Therefore, the frequency divider divides the 1 Hz clock signal generated by the experiment box into a 1/4 Hz clock, which is realized by VHDL language. The clk_gen clock divider module is used to divide the high frequency of the system clock into the low frequency required by the counter. For example, for a 50 MHz development board system, and the working frequency of the counter is 1 MHz, then the 1 s crystal oscillator will oscillate 50 million times and send out 50 million pulses. We need a counter with a modulo 50. After receiving 50 million pulses, it will output 1 million pulses to the Timer module. The system flow chart is shown in Figure 3.

2.4. Design and Realization of Countdown Display Module

The countdown module is realized by a counter. The counter is a commonly used logic circuit in sequential logic circuits, and its function is mainly to count the number of pulses. The circuit designed in this article counts down the red light time. First, the count output signal is set to 24, and each clock pulse is decremented by 1. When it is reduced to 1, the red light is off and the green light is on. It can be realized by 74LS190 or 74LS191, and the generated component symbols are shown in Figure 4.

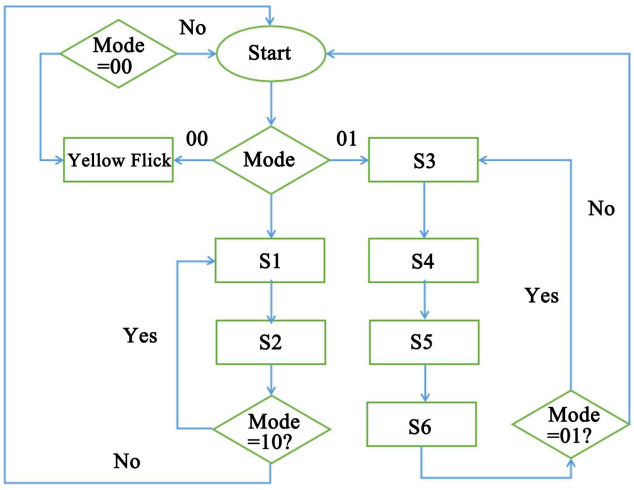

Figure 3. Traffic light system flow chart.

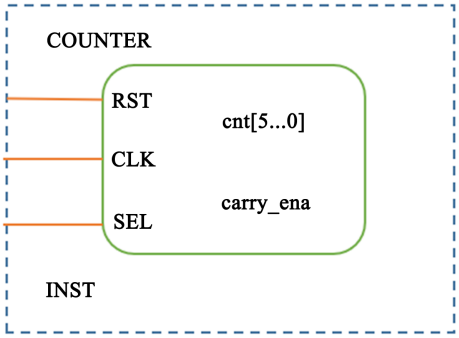

Figure 4. Symbol of traffic light module.

2.5. Design and Implementation of Red-Yellow-Green State Transition Module

By analyzing the working process of traffic lights, it can be divided into north-south and east-west directions. Make the red, yellow, and green lights turn on for 24 s, 4 s, and 20 s in a cycle. The traffic light state conversion table is shown in Table 1. The clock input of the state conversion module is the 1/4 Hz clock signal generated by the aforementioned frequency dividing module, and the twisted ring counter of modulus 12 is designed as a timing controller to control the change of the lamp.

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Table 1. Timetable for east-west and north-south traffic light intervals.

Number	East-west direction	North-south direction	Time (s)
1	Green light on, go	The red light is on. No traffic	20
2	Yellow light on, stop	The red light is on. No traffic	3
3	The red light is on. No traffic	Green light on, go	20
4	The red light is on. No traffic	Yellow light on, stop	3

2.7. UART Serial Communication Module

The UART module is basically divided into three parts, including the baud rate generating module, the receiving module and the sending module. Basic UART communication only needs two signal lines (RX, TX) to complete the mutual data communication, and the reception and transmission are in full duplex mode. TX is the UART transmitting terminal, which is output; RX is the UART receiving terminal, which is input. After UART overall RTL synthesis, as shown in the figure, CLKDIV module generates 9600 baud rate clock for TX and RX; TX module wsig is the transmit enable signal, tx terminal converts the parallel data of data_in into UART protocol serial transmission, RX receives TX Send the content, and re-convert the data into parallel data and read it out at the dataout end.

2.8. Scan_Seg1 Digital Tube Scanning Module

Module function: Because the segment of each digital tube on the DE2-70 development board is in the constant strobe state, there is no chip select signal, and the digital tube is driven by static scanning. Module operation process: scan_seg1. The digital tube scanning module will receive the data that needs to be displayed on the digital tube in each mode sent by the Controller module, such as the delay time of different color lights, and will dynamically scan according to the value on the Timer module Way to light up the corresponding digital tube.

3. Results and Analysis

The traffic light controller designed in this article is finally implemented on the EP4CE15E22C8 chip platform of Altera's Cyclone IV series. Before hardware implementation, complete the timing simulation of the three modules, and then complete the timing simulation of the top-level module, and then assign the pins on the target chip. After connecting the corresponding pins, you can download the program, and finally through the correct connection, Connect the corresponding output to the 6 light-emitting diodes of different colors on the experiment box, and you can observe the conversion of three-color traffic lights in two directions. Connect the countdown count output terminal to the corresponding pin of the 7-segment digital tube to observe the countdown of the red light.

3.1. Simulate Actual Traffic Analysis

In order to be more in line with the actual traffic situation, the clock needs to be

divided in frequency to achieve units of seconds. The system working clock clk1 has a period of 60 μs; rst is a reset signal, which works normally at high level; clk_out is a clock working signal source with a period of 1 s after frequency division. It can be seen from the traffic light sequence simulation diagram that green is the vehicle arrival rate obtained through detection, and the green light time in the north-south direction calculated by the polling model. When the arrival rate λ = 0.9, the corresponding waiting time is 20 s, That is, the green light in the north-south direction has 20 s to allow vehicles to pass. Since the system conversion time γ = 3, the waiting time of the red light in the east-west direction is 25 s; when the vehicle arrival rate λ = 0.92, it corresponds The green light time in the north-south direction is reduced to 18 s, and the waiting time for the red light in the east-west direction is correspondingly changed to 18 s, and vehicles at the intersection continue to be intelligently adjusted; when the arrival rate λ = 0.95, the passage time of vehicles in the north-south direction is increased to 16 s, The corresponding red light time in the east-west direction increases to 32 s. The data of the vehicle arrival rate is stored in the ROM storage module of the green light, and is read out to the FPGA control module through the FIFO module control, and enters the traffic light countdown and signal display. ctcn is the counting time of the green light, red is the waiting time of the red light in the east-west direction.

ctcn1 is the counting time of the red light. "Lamp-a" and "Lamp-b" are the status display of the red, green and yellow lights of the north-south and east-west traffic lights respectively. Status 1 represents the green light, status 2 represents the yellow light, status 4 represents the red light, and the east-west direction is the same. "Count-a" and "Count-b" are the countdown of the time of the three lights in the north-south and east-west directions respectively, which are consistent with the above-mentioned green and red lights. When the north-south direction "Lamp-a" = 1, that is, the north-south direction is a green light, and the corresponding arrival rate λ = 0.92, the green light duration for vehicles passing through the north-south direction is 18 s, and the yellow light for the intermediate transition time is 3 s. At this time, "Lamp-a" = 2, corresponding to the red light in the east-west direction counts down to 32 s, "Lamp-b" = 4. The total duration of the green and yellow lights in the north-south direction is equal to the red light in the east-west direction, which is consistent with the previous theory. The display status of the traffic light is consistent with the working status of the countdown counter, which conforms to the traffic law. It can be seen that there is a delay in the circuit in the obtained simulation diagram, but it does not affect the realization of the design and the analysis of the results. The intelligent adjustment performance of the intelligent traffic light system to be realized by this design is verified.

3.2. Static Timing Analysis and Comprehensive Analysis

Static Timing Analysis: Static Timing Analysis is a verification method. It uses exhaustive analysis methods, extracts the circuit timing path and calculates the

delay, and checks whether the setup time and hold time of the signal are satisfied. Through the analysis of the maximum path and the minimum path delay, errors that violate timing constraints are found. The commonly used software for static analysis is "Prime Time" software from Synopsys Ltd.

Physical synthesis: After completing the logic synthesis, we completed the front-end design and generated a gate-level netlist with logic functions. But what we have done so far is design based on logic and code, and does not involve design at the physical level. At this time, the analysis of chip performance is only based on the results of algorithms and computer simulations, and has no actual physical meaning. Therefore, in order to produce a design file that truly meets the process requirements and can be taped out, we need to perform back-end verification. The first step is to use the physical synthesis tool, according to the gate-level network standard files and constraints, and use the physical library provided by foundry to perform layout, clock tree synthesis and routing, complete the layout design, and generate a "gds" file containing physical information, providing Tape out the foundry factory. The integrated physical and physical tool used in this design is the IC Compiler tool of synopsys.

3.3. Design Rule Checking

Only chips that meet the design rules can ensure that the layout meets the manufacturer's tape-out requirements. The design rule is the specification of the size of each figure in the layout. The general design rule is based on the feature size of the device, and based on the manufacturing process level and other considerations, a set of allowable ranges for the graphic size of each layer of the mask are worked out. In the design, the DRC inspection tool Hercules in ICC is used for inspection.

4. Summary and Conclusion

This experiment completes the design of the traffic light circuit through modularization, and uses the Quartus II software to complete the design and simulation of the program. After hardware verification, the FPGA-based traffic light color conversion function and timing are correct, and the experimental results meet the expected goals. This design mainly realizes the intelligent adjustment design of traffic lights at intersections. Based on the dual-queue single-server threshold polling service model, the detected traffic flow is statistically analyzed to obtain the vehicle arrival rate, and the traffic lights are displayed according to the threshold service rules. The time is allocated to realize the real-time control state of the green light period being extended when the traffic volume is high at the intersection, and the green light period being shortened when the traffic volume is low. Finally, the programming control design of the system function is completed on the QUARTUS II software platform. Experiments have proved that on the FPGA system platform, using the threshold polling service model, traffic lights can realize intelligent adjustment of the display time of traffic lights and improve the efficiency of vehicle traffic at intersections.

This FPGA-based traffic light smart chip design project is only an introductory project in the design of traffic light chips. I think there is still a lot of room for improvement in such traffic light chips, and I still need to do a lot. In terms of function, the function of the chip designed this time is relatively single. Although the UART module gives the chip a way to remotely control the control mode, many parameters have been set in advance in order to simplify the project, and it has not been completely customized. Realizing true intelligence and integration is the future goal of modern traffic lights, and such traffic lights will be able to collect real-time road condition information through some accessible data collection equipment, and conduct automatic analysis to make judgments and processing. On top of this, all the traffic lights in each area will form a complete traffic control system. The real-time data collected by each traffic light will be summarized on the control system, and the system can regulate and control the traffic lights in the entire area. The traffic in the entire area reaches the optimal situation. The larger the area, the greater the flow of this data, and the more difficult it is to synchronize analysis. However, once the regional traffic control system is implemented, the efficiency of traffic services can be greatly improved. Minimize the degree of congestion and save a lot of time for the traffic police.

Funding

This work was funded by Collaboration between industry and school Project of Ministry of Education: "Innovative teaching and training of PAEE system in electronic information major" (No. 201901103032).

Conflicts of Interest

The author declares no conflicts of interest regarding the publication of this paper.

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