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Loop-Shaping Based Control for Switch Mode DC-DC Power Converters

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Abstract

Renewable energy sources require switching regulators as an interface to a load with high efficiency, small size, proper output regulation, and fast transient response. Moreover, due to the nonlinear behavior and switching nature of DC-DC power electronic converters, there is a need for high-performance control strategies. This work summarized the dynamic behavior for the three basic switch-mode DC-DC power converters operating in continuous conduction mode, *i.e.* buck, boost, and buck-boost. A controller was designed using loop-shaping based on current-mode control that consists of two feedback loops. A high-gain compensator with wide bandwidth was used in the inner current loop for fast transient response. A proportional-integral controller was used in the outer voltage loop for regulation purposes. A procedure was proposed for the parameters of the controller that ensures closed-loop stability and output voltage regulation. The design-oriented analysis was applied to the three basic switch-mode DC-DC power converters. Experimental results were obtained for a switching regulator with a boost converter of 150 W, which exhibits non-minimum phase behavior. The performance of the controller was tested for voltage regulation by applying large load changes.

Keywords

Renewable Energy Sources, Loop-Shaping Control, Power Electronic Converters, Current-Mode Control

1. Introduction

Switch-Mode Power Supplies (SMPS) were first developed for aerospace applications in the 60's. The interest in DC-DC switched power converters has in-

creased due to the many DC electrical energy applications from renewable energy sources like fuel-cell stacks, photovoltaic arrays, or wind power [1] [2]. These sources require an interface to condition and regulate their output voltage before being connected to the grid. Many of non-isolated topologies have been proposed using the three basic DC-DC converters, namely buck, boost, and buck-boost. In recent years, interesting topologies have been proposed to obtain high step-up or step-down voltage conversions [3].

The dynamical study of these converters is crucial for control purposes [4] [5]. Furthermore, the design of a suitable control strategy for SMPS output voltage regulation represents a major challenge due to the existence of undesirable effects such as large unpredictable loads, parameter variations, nonlinearities, disturbances, and measurement noise. Moreover, the loop stability and performance are affected by the converter parameters; therefore, they should be considered into the analysis and controller design. In this sense, several control methods have been proposed to operate SMPS properly. For instance, linearized models around an operating point have been proposed to describe the dynamic behavior of switching regulators [6] [7]. About the schemes to control these converters, the most widely used are *voltage-mode* control and *current-mode* control. To develop a suitable controller, several techniques based on numerical state-space modeling, sliding-modes, H_∞, linear-quadratic-regulator, fuzzy, optimal, and nonlinear control have been proposed in the open literature [8]-[15]. However, the physical implementation of some of the above techniques may increase the complexity, since microcontrollers are required. For this reason, there is more advisable use of linear techniques that allow finding general expressions that can be used to implement the controllers in a simple way, which can be built by using low-cost operational amplifiers.

In this paper, a discussion of the steady state and dynamic behavior is given for the three basic converters, *i.e.* buck, boost and buck-boost. Additionally, a current-mode controller design is given with the corresponding parameter selection criteria to ensure stability and performance for these converters. A physical implementation is shown based on low-cost operational amplifiers. To show the performance of the controller, an experimental 150 W boost prototype was built to validate the results given within, where step changes are applied to the output load.

This work is organized as follows. In Section 2, analysis, description and dynamic behavior of the three basic switch-mode PWM converters are discussed. Section 3, details the design of a current-mode controller with the corresponding parameter selection process. Experimental results validating the controller performance are shown in Section 4, and finally some concluding remarks are addressed in Section 5.

2. The Basic Topologies of Power Converters

The demand for high-performance PWM power converters has increased due to the use of DC electric renewable sources. The primary role of power conversion

equipment is to facilitate the transfer of power from the source to a specified load by adjusting the voltages and currents from one form to another. This equipment must be energy-efficient and reliable with a high power density; thus, reducing their size, weight, and cost. To fulfill the above requirements, it is essential to understand the converter topology's steady state and transient behavior. In this sense, the operation modes widely used are continuous conduction mode (CCM) and discontinuous conduction mode (DCM), associated with high and low power density applications. In CCM, the inductor current should never cross zero during one switching cycle. In DCM, the inductor current ripple is large enough to cause the inductor current falls to zero. Now, the description and dynamic operation of the three basic power DC-DC converters in CCM are highlighted.

2.1. Buck Converter

The growth of renewable energy sources integration has brought new applications for buck converter topology, *i.e.* battery chargers in photovoltaic and wind energy systems [16] [17] [18].

The basic topology of this converter is show in **Figure 1(a)**, where a power MOSFET M is used as an active switch, E the input voltage source, $D1$ the diode, L the filter inductor, C the filter capacitor and R the load resistance. The duty cycle D is computed by $D = t_{ON}/T$ where t_{ON} is the period, which M is conducting and T the switching period; therefore, D may take values between 0 and 1. Subsequently, i_S, i_L, i_C and i_O are the source, inductor, capacitor and output currents, respectively. Finally the output (capacitor) voltage is v_O.

In this case, the resulting average output voltage V_O in steady state is smaller than the input voltage E. Moreover, the average output current I_O is greater than the average source current I_S. In the conventional buck converter, shown in **Figure 1(a)**, there are losses due to the diode $D1$. To improve the power converter efficiency, a synchronous rectifier [19] can be used as depicted in **Figure 1(b)**, where the diode $D1$ is replaced by a power MOSFET M_2.

In steady state CCM operation, the voltage and current ripples due to the switching are

$$\Delta V_C = \frac{D(1-D)E}{8 f_S LC}, \quad \Delta I_L = \frac{D(1-D)E}{f_S L} \tag{1}$$

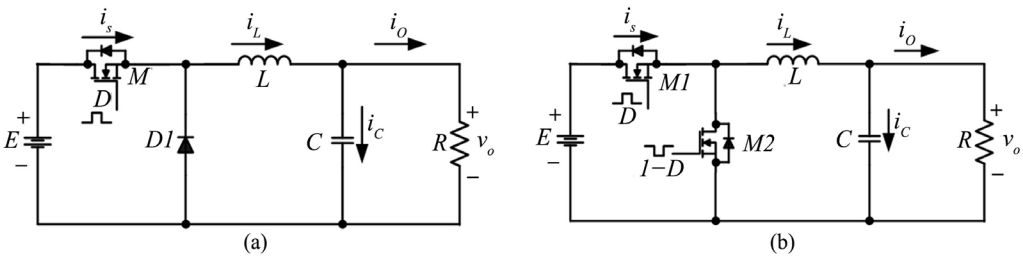

Figure 1. (a) Conventional buck converter, and (b) Synchronous buck converter.

where f_S is the switching frequency. Additionally, the inductor value must be selected such as $L > (1-D)R/2f_S$ to ensure CCM.

In this work, state-space averaging is used, which is a modeling technique widely used to "approximate" the behavior of switching converters [7] [20] [21]. This technique requires that the LC output filter corner frequency f_C be smaller than the switching frequency, such that $f_C/f_S < 1$. For the buck converter, the average dynamical model is represented by

$$\dot{i}_L = \frac{1}{L}(-v_O + Ed) \tag{2a}$$

$$\dot{v}_O = \frac{1}{C}\left(i_L - \frac{v_O}{R}\right) \tag{2b}$$

where the state variables are i_L and v_O, and the control input is the duty cycle *d*. Assuming that each state variable and the control signal are the sum of DC and AC components, they can be decomposed as

$$\begin{aligned} i_L &= I_L + \tilde{i}_L \\ v_O &= V_O + \tilde{v}_O \\ d &= D + \tilde{d} \end{aligned} \tag{3}$$

where (˜) stands for AC variables. Note that the AC terms are equal to zero in steady state. The steady state values for the average output voltage and average inductor current are

$$V_O = ED, \quad I_L = \frac{ED}{R} \tag{4}$$

Consequently, taking into account the AC terms, the linear average small-signal model for the buck converter is given by

$$\begin{bmatrix} \dot{\tilde{i}}_L \\ \dot{\tilde{v}}_O \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} \tilde{i}_L \\ \tilde{v}_O \end{bmatrix} + \begin{bmatrix} \frac{E}{L} \\ 0 \end{bmatrix} \tilde{d} \tag{5}$$

The model shown in (5) describes the behavior for frequencies up to $f_S/2$; thus, the corresponding transfer functions results as

$$\frac{\tilde{i}_L(s)}{\tilde{d}(s)} = \frac{V_O}{DR} \times \frac{RCs+1}{LCs^2 + \frac{L}{R}s + 1} \tag{6a}$$

$$\frac{\tilde{v}_O(s)}{\tilde{d}(s)} = \frac{V_O}{D} \times \frac{1}{LCs^2 + \frac{L}{R}s + 1} \tag{6b}$$

where both transfer functions have a minimum phase behavior, *i.e.* there is no right-half plane (RHP) zeros; therefore, control design is easy to carry out.

2.2. Boost Converter

The step-up power converter, commonly known as a boost converter, is shown in **Figure 2**. It has an input power source *E*, connected in series with a filter

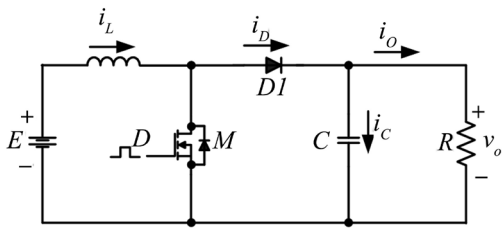

Figure 2. Conventional boost converter.

inductor L, an active switch M, a diode $D1$, an output capacitor C and the load R. The main characteristic of this converter is that, in steady state, the average output voltage V_O is greater than the input E; henceforth, the name boost.

Due to its nature, this type of converter is used in applications where the source voltage needs to step up to higher levels, *i.e.* front-end stage for photovoltaic. If a higher power is required, an interleaved converter with two paths can be used.

In steady state CCM operation, the voltage and current ripples for the boost converter due to the switching action are computed by

$$\Delta V_C = \frac{DI_O}{f_S C} \quad \text{and} \quad \Delta I_L = \frac{DE}{f_S L} \tag{7}$$

additionally, to ensure CCM, the inductor value must be selected as $L > D(1-D)^2 R/2 f_S$. Notice that the inductor current is equal to the source current. In contrast to the buck converter, this topology needs a larger filter capacitor C to limit the output voltage ripple.

In the boost converter, it is possible to average the dynamical behavior of this converter by neglecting the ripple phenomena. Thus, applying Kirchhoff laws when M is ON/OFF, the average continuous nonlinear model is obtained as

$$\dot{i}_L = \frac{1}{L}\left(-(1-d)v_O + E\right) \tag{8a}$$

$$\dot{v}_O = \frac{1}{C}\left((1-d)i_L - \frac{v_O}{R}\right) \tag{8b}$$

The nonlinear differential equations in (8) are said to be bilinear, since the input signal d is multiplying the states variables v_O and i_L directly. The steady state values for the output voltage and inductor current can be easily obtained resulting in

$$V_O = \frac{E}{1-D}, \quad I_L = \frac{E}{(1-D)^2 R}. \tag{9}$$

Consequently, taking into account the AC terms defined previously in (3), yields to the linear average small-signal model for the boost converter as

$$\begin{bmatrix} \dot{\tilde{i}}_L \\ \dot{\tilde{v}}_O \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1-D}{L} \\ \frac{1-D}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} \tilde{i}_L \\ \tilde{v}_O \end{bmatrix} + \begin{bmatrix} \frac{E}{(1-D)L} \\ -\frac{I_L}{C} \end{bmatrix} \tilde{d} \tag{10}$$

where the bilinearity has been eliminated and the resulting matrix has only constant values. The resulting transfer functions of (10) can be expressed as follows

$$\frac{\tilde{i}_L(s)}{\tilde{d}(s)} = \frac{V_O}{(1-D)^2 R} \times \frac{RCs+2}{\frac{LC}{(1-D)^2}s^2 + \frac{L}{(1-D)^2 R}s + 1} \tag{11a}$$

$$\frac{\tilde{v}_O(s)}{\tilde{d}(s)} = \frac{V_O}{1-D} \times \frac{1 - \frac{L}{(1-D)^2 R}s}{\frac{LC}{(1-D)^2}s^2 + \frac{L}{(1-D)^2 R}s + 1} \tag{11b}$$

where the transfer function output voltage-to-control signal exhibits a non-minimum phase behavior since it has a RHP zero.

2.3. Buck-Boost Converter

This converter is depicted in Figure 3. In the buck-boost converter, the diode $D1$ and inductor L have been interchanged compared to the buck converter given in Figure 1(a).

The main feature here is that the average output voltage V_O is negative. Its magnitude can be either greater, equal (when $D = 0.5$), or smaller than the input voltage; hence the name buck-boost has been coined. Thus, the output voltage and inductor ripple are the same as stated in (2).

In steady state CCM operation, the voltage and current ripples for the buck-boost converter due to the switching action can be computed by

$$\Delta V_C = \frac{DI_O}{f_S C}, \quad \Delta I_L = \frac{DE}{f_S L} \tag{12}$$

additionally, to ensure CCM, the inductor value must be selected as

$$L > \frac{(1-D)^2 R}{2 f_S} \tag{13}$$

It is evident the existence of similarities between the boost and buck-boost converters, where the only remarkable difference is in the current through the capacitor. Considering the average approach, a nonlinear dynamical model for the buck-boost converter is obtained as

$$\dot{i}_L = \frac{1}{L}\left((1-d)v_O + Ed\right) \tag{14a}$$

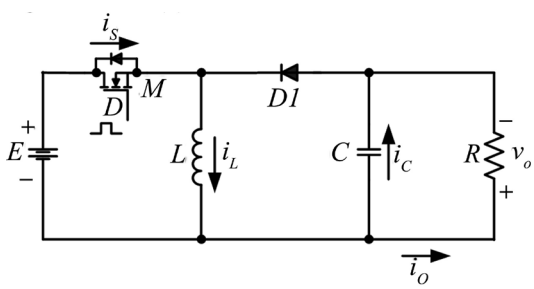

Figure 3. Conventional buck-boost converter.

$$\dot{v}_O = \frac{1}{C}\left(-(1-d)i_L - \frac{v_O}{R}\right) \tag{14b}$$

In fact, model (14) is bilinear (11), since the control input d multiplies both state variables. Again, using the decomposition of DC and AC as in (3), the DC relationships for the average output voltage and inductor current are

$$V_O = -\frac{ED}{1-D}, \quad I_L = \frac{ED}{(1-D)^2 R} \tag{15}$$

On the other hand, the small-signal linear model for the AC component is given by

$$\begin{bmatrix} \dot{\tilde{i}}_L \\ \dot{\tilde{v}}_O \end{bmatrix} = \begin{bmatrix} 0 & \frac{1-D}{L} \\ -\frac{1-D}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} \tilde{i}_L \\ \tilde{v}_O \end{bmatrix} + \begin{bmatrix} \frac{E}{(1-D)L} \\ \frac{I_L}{C} \end{bmatrix} \tilde{d} \tag{16}$$

Note that this dynamical model is no longer bilinear, because the matrix has only constant parameters. For feedback design purposes, the aim is to get the frequency domain representation of (16); thus, the transfer functions for the control signal to each state variable are

$$\frac{\tilde{i}_L(s)}{\tilde{d}(s)} = -\frac{V_O}{D(1-D)^2 R} \times \frac{RCs + 1 + D}{\frac{LC}{(1-D)^2}s^2 + \frac{L}{(1-D)^2 R}s + 1} \tag{17a}$$

$$\frac{\tilde{v}_O(s)}{\tilde{d}(s)} = \frac{V_O}{D(1-D)} \times \frac{1 - \frac{DL}{(1-D)^2 R}s}{\frac{LC}{(1-D)^2}s^2 + \frac{L}{(1-D)^2 R}s + 1} \tag{17b}$$

Similarly to the transfer function output voltage-to-control signal of the boost converter, there is a RHP zero; thus, the control task becomes difficult.

3. Loop Shaping for Current-Mode Control

Two of the most widely used control techniques are *voltage-mode* control and *current-mode* control. The *voltage-mode* control (VMC) scheme uses just one feedback loop and usually includes two elements: a voltage error amplifier and a voltage comparator [20]. The transfer functions like loop gain, closed-loop input impedance, and closed-loop audio susceptibility can be derived from the small-signal model. This control scheme is easy to design and implement due to a single control loop, but it has two major drawbacks: 1) the PI-controller used for output voltage regulation introduces a slow dynamic response, and 2) the stability is difficult to achieve for a non-minimal transfer function.

Current-mode control (CMC) contains two nested feedback loops [22]. The outer loop measures the output voltage, and the inner loop measures the current flowing through the inductor. This scheme has several advantages over *voltage-mode* control. The first one is that the active switch (MOSFET, IGBT, or

Bipolar Transistor) is turned OFF when the inductor current reaches a threshold level, and consequently, there is no current overload through the converter. The second advantage is that several switching converters can operate in parallel without a load-sharing problem. All the switching converters are provided with the same PWM signal from the control circuitry. Finally, it is well-known that the inductor current's feedback action greatly improves the dynamic performance of the overall closed-loop. In *current-mode* control, the inductor current acts as a current source. The output *LC* filters acts a voltage-controlled current source that supplies current to the output capacitor and the load; thus, the order of the system is reduced by one and the feedback compensation is considerably simplified.

There are two basic schemes reported in the open literature for *current-mode* control; one is referred to as the *peak current-mode* control (PCMC) [23] and the other as the *average current-mode* control (ACMC) [24]. In PCMC control, the inductor or active switch current is directly fed back without a low-pass filter; then, a wide bandwidth current is obtained. A major drawback in PCMC is its instability, since oscillations may occur when the duty cycle exceeds 50%. However, this instability can be eliminated by the addition of an artificial ramp. On the other hand, ACMC is an effective control method that improves current regulation accuracy and fast dynamic response. In this technique, the inductor current is measured and averaged by a compensation network to obtain its DC component. ACMC has the following advantages over PCMC: 1) there is no need for an external compensation ramp, 2) it has a high gain at DC and low frequencies, 3) noise immunity of the measured current signal, and 4) over-current protection for each cycle of PWM. It has been shown that a modified version of ACMC can also be applied to high-gain converters, *i.e.* quadratic and cascade [25] [26] [27].

Current-mode control has been widely adopted as a useful technique for easing the design and improving regulators' dynamic performance with switch-mode converters. Early references have discussed the basic principles and advantages of this technique [22]. A methodology is now given to select the controller gains for the boost converter properly. When the inductor current is used for output voltage regulation, a faster response is obtained when step changes are applied to the load. Sensing the inductor current can also be used for preventing overload current through the converter. To derive the controller expressions, a proposed configuration for this technique is shown in **Figure 4**. Notice that this scheme applies in general for the buck, boost, and buck-boost converters. As can be seen, this scheme has current and voltage loops. For the current loop, N is the current sensor gain, $G(s)$ a high-gain compensator, $F(s)$ a low-pass filter, and finally V_P the peak magnitude of the ramp used to generate the control pulses. For the voltage loop, H stands for the voltage sensor gain, V_R the desired output voltage, and $K(s)$ the transfer function of the PI controller.

The overall controller design procedure for this scheme is a twofold problem: 1) shaping gain for the current loop $L_1(s)$, *i.e.* the product of transfer functions of

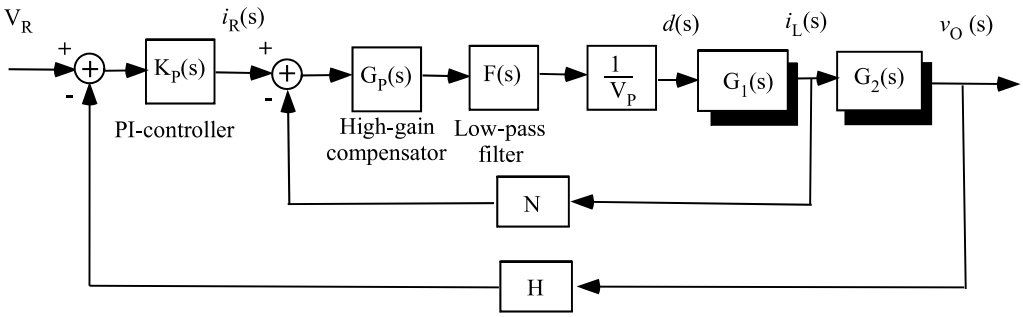

Figure 4. Switching regulator scheme to be used to control the power converters.

inner loop, and 2) shaping gain for the voltage loop $L_V(s)$, *i.e.* the product of transfer functions in the outer loop. For robust stability of each loop the following requirements have to be satisfied: 1) for relative stability, the slope at or near cross-over frequency must be not more than −20 dB/dec; 2) to improve steady-state accuracy, the gain at low frequencies should be high; and 3) for robust stability, appropriate gain and phase margins are required [28]. In the following, an easy-to-use procedure is given to ensure good loop gain characteristics of the closed-loops. The poles and zeros for the current-mode controller are set mainly from the converter's operating switching frequency.

3.1. Current Loop Control

As can be seen, the transfer function inductor current-to-control signal has two complex poles and a left-hand zero. When damping is added through the gain N, the behavior looks like a gain and a single pole. Then, the high-gain compensator and low-pass filter are added, which have the following transfer functions

$$G(s) = G_P \frac{s+\omega_Z}{s} \quad \text{and} \quad F(s) = \frac{1}{s/\omega_p + 1} \tag{18}$$

respectively, where G_P is the compensator gain, ω_Z stands for the location of the compensator zero and ω_P for the location of the filter pole. Notice that both transfer functions can be implemented using a single operational amplifier as shown in **Figure 5**. Then, the corresponding control law $\tilde{d}$ is defined by

$$\tilde{d} = \frac{1}{V_p}\left(\frac{1}{s/\omega_p + 1}\right)\left(\frac{G_p(s+\omega_Z)}{s}\right)\left(\tilde{i}_R - N\tilde{i}_L\right). \tag{19}$$

The design procedure is given now. The high-gain compensator zero ω_Z should be placed at least a decade below of half of the PWM switching frequency f_S. Practically, the zero is determine by the relationship $\omega_Z = 1/R_a C_a$ where R_a and C_a are the resistance and capacitance corresponding to the current loop control circuit. The low-pass filter pole f_P, on the other hand, should be placed either at half of f_S or above. Using the circuitry in **Figure 5**, the pole is computed by

$$\omega_p = \frac{C_a + C_b}{R_a C_a C_b} \tag{20}$$

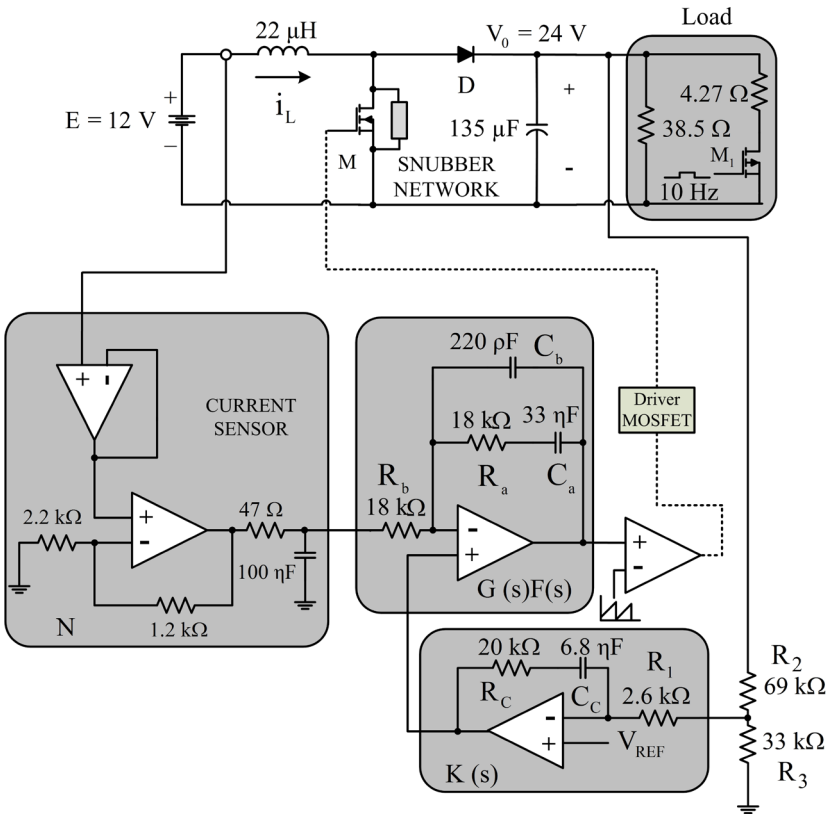

Figure 5. Switching regulator using a boost converter of 150 W.

Here C_b is the capacitor of the current loop circuit.

The compensator gain is computed by

$$G_P = \frac{R_a}{R_b} \tag{21}$$

where the resistance values must be carefully selected such that

$$G_P < \frac{5V_P (1-D)^2 R}{2NV_O} \tag{22}$$

3.2. Voltage Loop Control

Once the current loop has been tuned, the voltage loop gain has to be designed. The outer loop is designed to provide a suitable steady state correction of the output voltage using a PI controller. The transfer function for the PI controller is given by

$$K(s) = K_P \left(1 + \frac{1}{T_i s}\right) \tag{23}$$

where $K_P = R_C / R_1$ is the proportional gain and T_i the integral time. The resulting reference current for this loop is

$$\tilde{i}_R(s) = K_P \left(1 + \frac{1}{T_i s}\right)(\tilde{v}_R - H\tilde{v}_O) \tag{24}$$

The design procedure is as follows. The proportional gain is selected such that

$$K_P < \frac{10N}{(1-D)HR} \tag{25}$$

where $H = (R_1 \parallel R_3)/(R_1 \parallel R_3 + R_2)$.

Finally, the integral time is computed by $T_i = R_C C_C$ where R_C and C_C are the resistance and capacitance values of the PI controller, which must be selected such that $1/T_i$ should be placed at least one decade below f_S.

In this sequel, for the sake of clear and straightforward exposition, the attention has been focused on a boost converter since its transfer function (14) has a non-minimum behavior; thus, a controller is more difficult to design. However, without loss of generality, the proposed control scheme can be extended to both buck and buck-boost converters. The resulting expressions are shown in Table 1. As the buck converter has a minimum phase behavior, voltage-mode control can be used where the output voltage is the only feedback variable.

4. Experimental Results

A boost converter with the corresponding current-mode controller is shown in Figure 5, where the procedure outlined in Section 3 has been used. The converter parameters are shown in Table 2. The inductor current is measured using by a LA50-P transducer from LEM manufacturer with a current gain of $N = 0.07$. An input source of $E = 12$ V is provided and a nominal duty cycle of $D = 0.5$ is selected, which accordingly to (10) provides an average output voltage of $V_O = 24$ V and an average inductor current of $I_L = 12.6$ A to a nominal resistive load of $R = 3.8\ \Omega$, which results in an output power of about 150 W.

Table 1. Summary for controller tuning.

Converter	f_Z	f_P	G_P	T_i	K_P
Buck	———	———	———	$10/f_S < T_i$	$K_P < \frac{5V_P D}{HV_O}$
Boost	$f_Z < \frac{f_S/2}{10}$	$f_S/2 < f_P$	$G_P < \frac{5V_P(1-D)^2 R}{2NV_O}$	$10/f_S < T_i$	$K_P < \frac{10N}{(1-D)HR}$
Buck-boost	$f_Z < \frac{f_S/2}{10}$	$f_S/2 < f_P$	$G_P < \frac{5V_P D(1-D)R}{NV_O}$	$10/f_S < T_i$	$K_P < \frac{5N}{HR}$

Table 2. Boost converter parameters.

Capacitor C	135 μF
Inductor L	22 μH
Nominal load R	3.8 Ω
Diode D	Schotky SBL3045PT
MOSFET M	IRFP4468
MOSFET M_1	IRF150
Modulator	LM311

Finally, the switching frequency is selected to be $f_S = 75$ kHz, the peak magnitude of the ramp is $V_P = 5$ V, and the voltage sensor gain is $H = 0.033$. According to (7), the capacitor voltage and inductor current ripples are $\Delta V_C = 0.308$ V and $\Delta I_L = 3.6$ A, respectively. To ensure CCM, the inductor L has been selected such that (8) is fulfilled. The controller parameters are $f_Z = \omega_Z / 2\pi = 267.93$ Hz, $G_P = 1$, $f_P = \omega_P / 2\pi = 40.4$ kHz, $K_P = 7.7$ and $T_i = 0.0136$ ms.

Open and closed-loop experimental tests were performed considering nominal and step changes in the load resistance through the switch M_L. These variations range from 3.8 Ω to 38.5 Ω; that is from full to 10% of load at a frequency of 10 Hz, which evidently modifies the load current profile.

4.1. Open Loop Test

Frequency responses of the theoretical transfer functions and the corresponding experimental from the prototype are shown in Figure 6 and Figure 7. Indeed, this graphical comparison validates the mathematical representation concerning the experimental since the responses are qualitative close. The difference between the theoretical and experimental frequency responses at frequencies between 1 kHz to 1.1 kHz is mainly due to the equivalent series resistance (ESR) of the filter capacitor. The frequency response plots were obtained at the nominal load and open loop using the Frequency Response Analyzer 300 from AP Instruments. Note that the gain of the modulator $1/V_P$ is included in (12) for a coherent comparison.

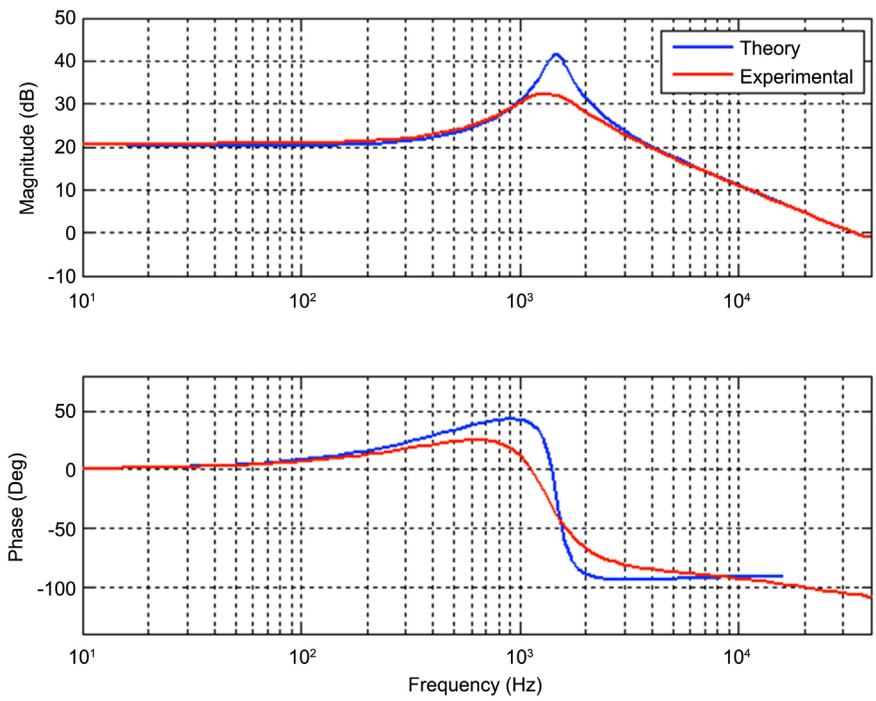

Figure 6. Comparison between theoretical and experimental frequency responses of transfer function inductor current-to-control signal: (top) magnitude (y-axis: 10 dB/div), (bottom) phase (y-axis: 50 deg/div).

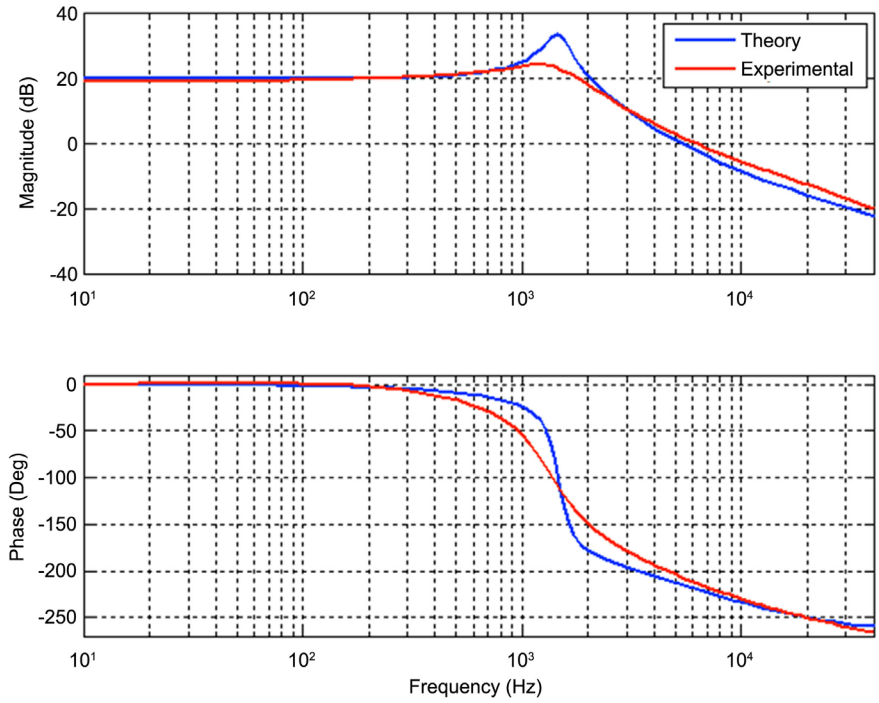

Figure 7. Comparison between theoretical and experimental frequency responses of transfer function output voltage-to-control signal: (top) magnitude (*y*-axis: 20 dB/div), (bottom) phase (*y*-axis: 50 deg/div).

The experimental time response of the boost converter behavior in open loop is shown in **Figure 8**, where the duty cycle is set to approximately to 24 V. The inductor current exhibits a triangular waveform. Now, step changes are applied to the load, the resulting output voltage changes from 24 V in nominal load to 28 V as M_1 is turned OFF. It is clear that the output voltage is unregulated since, for every change in the load, the output voltage changes as well, as can be seen in **Figure 9**.

4.2. Closed-Loop Test

The experimental frequency responses in closed-loop for the current and voltage loop gains are shown in **Figure 10** and **Figure 11** at the nominal load. In the first case, the current loop gain has a −20 dB/dec slope and 70 degree phase margin when the magnitude reaches 0 db; therefore, internal stability is ensured. The PI controller dominates the experimental frequency response for the voltage loop gain. At the crossing of 0 db, the slope has a −20 dB/dec slope with a 88 degrees phase margin, which ensures robust stability. Furthermore, both loop gain responses show high gains at low frequencies and a 4 kHz bandwidth.

The output voltage regulation is shown in **Figure 12**, when load changes are applied at a frequency of 10 Hz. It is noticeable that the output voltage remains constant despite changes from full to 10% load. The resulting control signal v_{CON} to be compared with the ramp signal is shown in **Figure 13**, where it is clear that a change in the load modify the duty cycle.

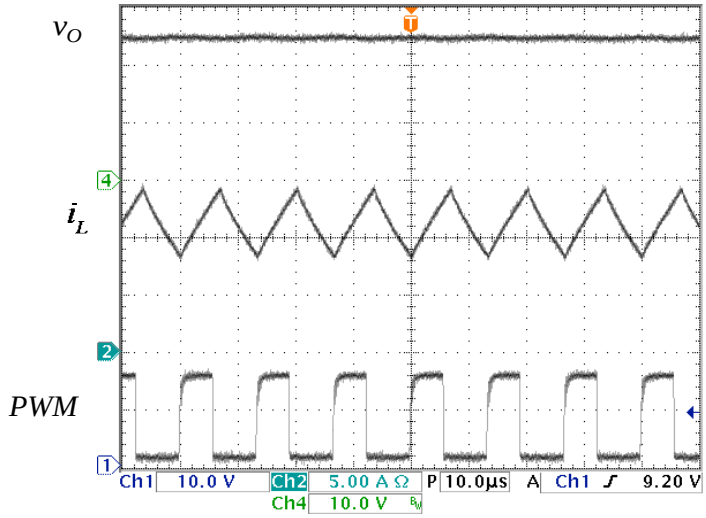

Figure 8. Open loop nominal response (*x*-axis: 40 ms/div): (from top to bottom) output voltage v_O (*y*-axis: 10 V/div), inductor current i_L (*y*-axis: 5 A/div), and PWM (*y*-axis: 10 V/div).

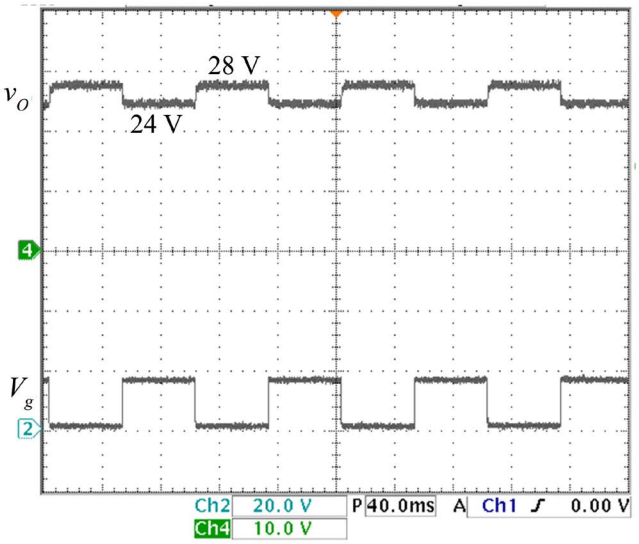

Figure 9. Open loop time response (*x*-axis: 40 ms/div): (top) output voltage v_O (*y*-axis: 10 V/div), and (bottom) trigger voltage V_g of load MOSFET M_1 (*y*-axis: 20 V/div).

5. Conclusion

This paper deals with a practical methodology for output voltage regulation for the three basic switch-mode converters. The scheme feds back the inductor current to implement an inner control loop using a high-gain compensator and a low-pass filter. The sensed current can also be used for over-current load protection. Afterward, the voltage loop is designed by implementing a PI controller for steady-state error regulation. Furthermore, a well-defined and straightforward procedure for the selection of the controller parameters is given, which ensures system stability and output voltage regulation. The resulting voltage loop gain is shaped into $L_V(s) \approx \omega_C / s$, which provides good gain and phase margins. The

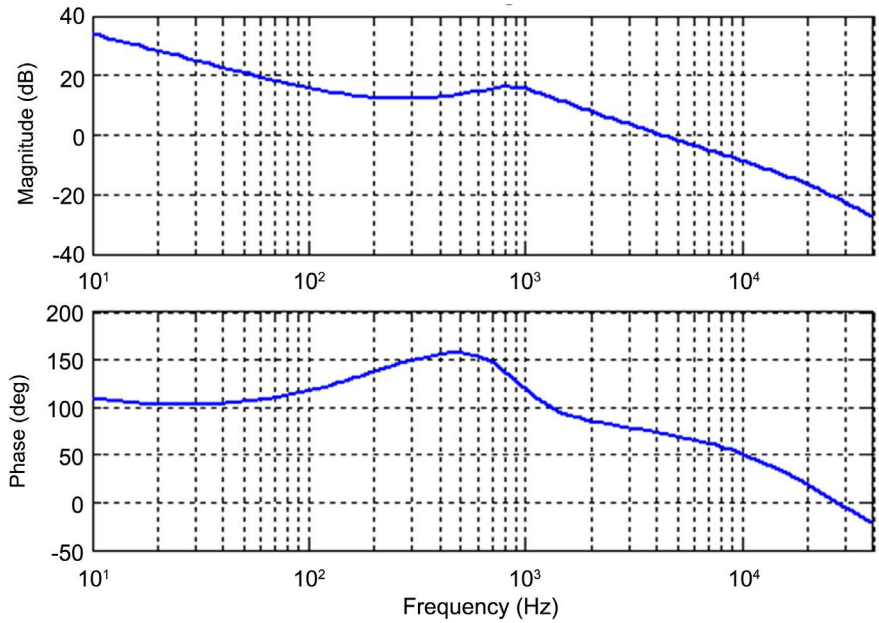

Figure 10. Experimental frequency response at nominal load for the current loop gain $L_I(s)$: (top) magnitude (*y*-axis: 20 dB/div), (bottom) phase margin (*y*-axis: 50 deg/div).

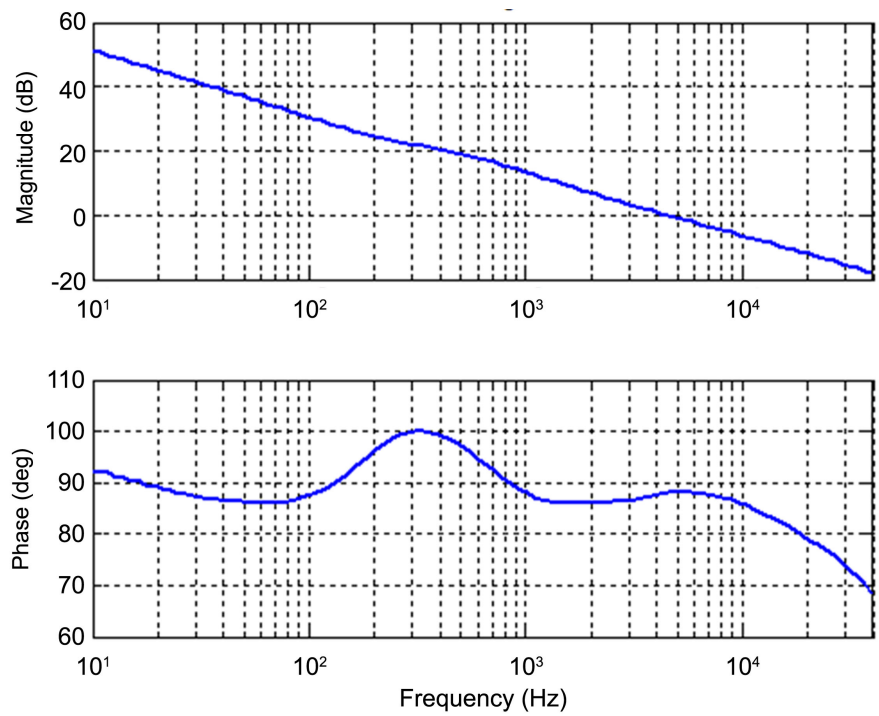

Figure 11. Experimental frequency response at nominal load for the voltage loop gain $L_V(s)$: (top) magnitude (*y*-axis: 20 dB/div), (bottom) phase margin (*y*-axis: 10 deg/div).

simplicity of the approach is of significant value in which the analytic results can be used to make design choices and tradeoffs between the inner and outer loops. This methodology was explicitly implemented in a current-mode controller for a boost converter, but it could be easily extended to the buck and buck-boost

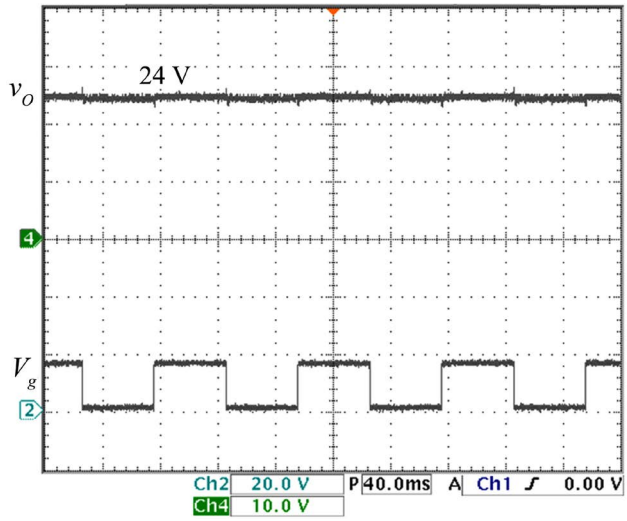

Figure 12. Closed-loop time response for the output voltage (*x*-axis: 40 ms/div): (top) output voltage v_O (*y*-axis: 10 V/div), and (bottom) trigger voltage V_g for MOSFET M_1 (*y*-axis: 20 V/div).

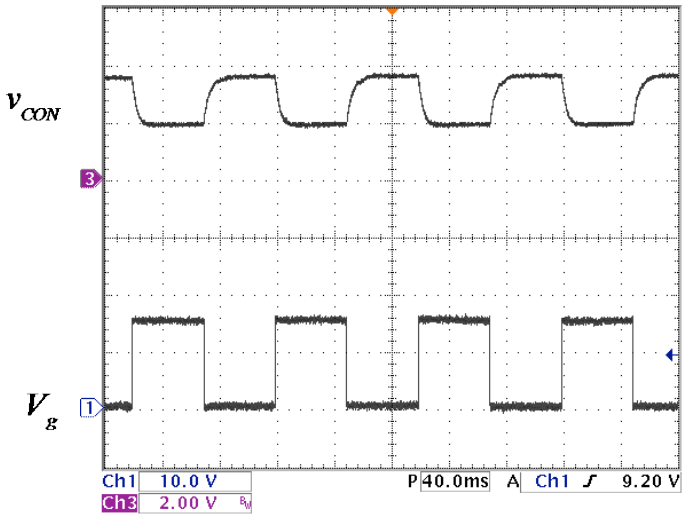

Figure 13. Control signal for step changes to the load (*x*-axis: 40 ms/div): (top) Control signal v_{CON} (*y*-axis: 2 V/div), and (bottom) trigger voltage V_g for MOSFET M_1 (*y*-axis: 10 V/div).

converters. This procedure can also be extended to other kinds of converters like the quadratic or cascaded buck or boost converters widely used to step-up or step-down voltages from renewable energy sources.

Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

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