

# Challenges in Processing Diamond Wire Cut and Black Silicon Wafers in Large-Scale Manufacturing of High Efficiency Solar Cells

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Abstract

Texturing of diamond wire cut wafers using a standard wafer etch process chemistry has always been a challenge in solar cell manufacturing industry. This is due to the change in surface morphology of diamond wire cut wafers and the abundant presence of amorphous silicon content, which are introduced from wafer manufacturing industry during sawing of multi-crystalline wafers using ultra-thin diamond wires. The industry standard texturing process for multi-crystalline wafers cannot deliver a homogeneous etched silicon surface, thereby requiring an additive compound, which acts like a surfactant in the acidic etch bath to enhance the texturing quality on diamond wire cut wafers. Black silicon wafers on the other hand require completely a different process chemistry and are normally textured using a metal catalyst assisted etching technique or by plasma reactive ion etching technique. In this paper, various challenges associated with cell processing steps using diamond wire cut and black silicon wafers along with cell electrical results using each of these wafer types are discussed.

## **Keywords**

Diamond Wire Cut, Black Silicon, Slurry Wafers, Amorphous Silicon, Additives, Etching and Texturization

## **1. Introduction**

Solar industry in the last several years had been driven by cost and competition to produce increased cell efficiency at the lowest production cost [1] [2] [3]. In order to address this ever-rising need of global demand to produce cheaper solar cells, it was essential to reduce the overall cost of cell manufacturing by mini-

mizing the cost of wafer manufacturing [4]. In wafer manufacturing, the crystallization process has a strong impact on the cost and potential performance of the cells [5]. In the last few years, the wafer manufacturing industry moved from regular slurry wire cut (SWC) to diamond wire cut wafers (DWC) considering the potential savings in silicon material wastage and significant improvement in sawing process throughput [6] [7] [8]. This created a cost pressure on solar cell manufacturers to quickly adapt to the changes in surface morphology of incoming diamond wire cut wafers as compared to slurry cut wafers and re-optimize the acidic etchant bath to deliver same quality of texturing process [9]. Establishment of a standard texturing process plays a key role in producing a wafer surface of diamond wire cut wafers that is equal or better to slurry cut wafers in terms of kerf loss, total thickness variation, reflectivity, mechanical strength and wafer performance for solar cells [10].

Literature studies did not address the various factors associated with operational issues with DWC wafers in a large-scale manufacturing environment. In this paper, the technical challenges in processing of DWC wafers into solar cells are discussed. From additive assisted texturing process to following a specific orientation of saw mark of wafers at each process station, all the techniques are discussed in detail. Various design of experiments (DOE's) to improve the texturing quality on DWC wafers using different sources of wafers, chemical compositions and silicon etch rates are discussed. Comparison of electrical results between regular SWC and DWC cells by overcoming processing challenges to achieve comparable efficiencies between these two wafer types is discussed.

In the second part of this work, the processing details of black silicon (B-Si) wafers into solar cells are discussed. Since the processing techniques of metal catalyst assisted etching (MCCE) using silver nitrate solution or plasma etching using reactive ion etching (RIE) were not available at cells fabrication facility, pre-processed wafers after MCCE and acidic texturing process were bought directly from wafer suppliers. After a quick surface cleaning process using Potassium Hydroxide (KOH), Hydrofluoric Acid (HF) and Hydrochloric Acid (HCl), the wafers were processed from POCl<sub>3</sub> diffusion to rest of the processing steps to complete as solar cells.

Results comparison between solar cells processed using SWC, DWC and B-Si wafers in terms of reflectivity, wafer appearance, surface morphology and cell electricals is discussed in this work. Significant process development work by using DOE's from texturing to screen printing process was carried out for DWC wafers to improve the average cell efficiency from barely 18.0% during preliminary process trials to over 18.75% using optimized process in continuous mass production. A similar set of process optimization was carried out for B-Si wafers to improve the average cell efficiency from 18.60% during preliminary trials to 18.96% using optimized process in continuous mass production.

## 2. Experimental Work

The standard process flow that was followed for Group-A (SWC), Group-B & C

(DWC) and Group-D (Black-Si) are as shown below in Figure 1.

Figure 1 shows the process flow for SWC (group A) and DWC wafers (group B) that were procured from a same wafer supplier and processed for solar cells. Texturing was carried out in an industrial inline wet chemistry equipment in acid etch bath filled with HF, HNO3 and a type of additives whose primary composition consisted of Phosphoric Acid (PA) and Acetic Acid (AC). These additives were added directly to the acid etch bath through an auto dosing system developed in-house to automatically pump certain quantity of additives into the etch bath based on frequency of time or number of wafers processed. Several experiments were conducted to find the optimum quantity of additives required in the acid etch bath to achieve a stable silicon etch loss of 1.7 µm per wafer side and uniform texturing quality. Other than the wafer types, all the processes were identical until solar cells were produced. Recipe optimization at diffusion and Plasma Enhanced Chemical Vapor Deposition (PECVD) process steps were required for DWC wafers due to in the increased wafer surface area as compared to SWC wafers. A double printing process was applied for the screen-printing of wafers from both groups and after contact firing process to form the front and rear electrical contacts, the cells from both groups were measured using a sun simulator at Standard Test Conditions (STC) with a 1-sun irradiance of 1000 W/m<sup>2</sup> at 25°C. Figure 1 also shows the process flow for DWC (group C) and Black-Si (B-Si) (group D) wafers that were procured from a same wafer supplier. DWC wafers from groups B and C were subjected to same processing conditions and B-Si wafers were subjected to a cleaning step using HF, HCl and KOH and continued for same processing as rest of the groups.



Figure 1. Process flow for fabrication of solar cells from SWC, DWC and Black-Si wafer groups.

Wafers from all four groups were analyzed under an optical microscope to visualize the surface morphology of wafers prior to and after texturing process with and without additives. As observed from Figures 2(a)-(d) images, the SWC wafers exhibits an evenly rough saw tooth structure, whereas DWC wafers from Figures 2(e)-(i) shows a series of smooth grooves and striped structures that are visible even to naked eye. These striped structures are known as pilgrim waves [11] that is usually formed during the wafer slicing process and the pattern depends upon many factors like the sawing method, type of coolant used, size of diamond grains, diameter of steel core wire, synthetic resins used for attaching diamond grains to core wire etc. Since the DWC wafer surface consists of smooth & rough structures, the wafer surface roughness cannot be used as a mean to measure the sawing quality as compared with sawing process carried out with SWC wafers. Figure 2(j) indicates the surface morphology of B-Si wafer after the acidic (HF + HCl) and alkaline (KOH) cleaning steps.



**Figure 2.** Schematic of wafer surface morphology due to texturing and cleaning process on SWC, DWC & B-Si wafer groups respectively.

## 3. Results

Several DOE's were carried out for group B wafers to identify the optimum etch rate required to work well with the chosen additive based on the saw damage removal and surface finish observed on DWC wafers after the texturing process. Etching mechanism in DWC wafers happens mostly at rough surface (chipped and striped structures) and less or none at smooth groove structures for same etching speed as slurry wafers. From literature, it is understood that for DWC wafers, the chipped and striped regions tends to have higher crystalline silicon content, whereas the smooth grooves has higher amorphous silicon due to presence of higher oxygen content [12]. These amorphous silicon regions become masking regions during texturing process and thereby affecting the etching quality on the wafer surface. Hence, these regions in DWC wafers requires additional etching time to be completely removed in order to have a reduced WAR and improved the short circuit current (Isc) performance in solar cells [13].

Figure 3(a) shows the Weighted Average Reflectance (WAR) measurements of SWC and DWC wafers from groups A and B measured on raw wafers (before texturing), textured wafers (without additives) and textured wafers (with additives). Reflectance measurements on these sub-groups of wafers were done to understand the behavior of texturing process on different wafer surface of SWC and DWC wafers. Reflectance values were measured from the wavelength of 300 nm to 1300 nm to cover the entire spectrum of light using a Bentham spectrophotometer. From these measurements, it can be observed that with respect to reflectance of raw wafers, the reflectance of DWC wafers increases after texturing process with additives (PA + AC group) as compared to the reflectance, which is the lowest for SWC wafers textured using same additives. This change in wafer surface behavior indicates that the additives that may work well with SWC wafers need not necessarily work in same manner with DWC wafers. As suggested from literature, it will be further interesting to understand this difference of surface behavior between these two wafer types and correlate it to the respective chemical treatment wafers undergo during texturing process [11].

**Figure 3(b)** shows the WAR measurements of DWC and Black-Si wafers from groups C and D measured on raw wafers (before texturing), textured wafers (with additives) and MCCE wafers (after cleaning) respectively. Since the texturing (MCCE) process was already done from the wafer supplier end, it was not possible to study the texturing process behavior on B-Si wafers by comparing to DWC wafers. From the results, it can be observed that the reflectivity of B-Si raw wafers is significantly lower than DWC wafers and which further reduces after a wafer surface cleaning process using chemicals such as 5% KOH, 10% HF and 10% HCl by concentration respectively for group D wafers.

**Figure 4** shows the DWC wafers having two types of saw marks, "straight" and "curved" in **Figure 4(a)** and **Figure 4(b)** indicating the variation in wire sawing process on incoming wafers, which is also zoomed and shown in the "inset". This type of variation has a direct influence on the surface roughness and morphology during texturing process resulting in non-uniform reflectivity across the wafers [14]. Processes like Saw Damage Etch (SDE) and texturing will cause preferential etching in such regions; however, studies have indicated that such periodic pattern of saw marks will remain throughout the cell fabrication process [9] [11]. **Figure 4(c)** and **Figure 4(d)** indicates the presence of such variation in saw marks after texturing and PECVD SiN deposition processes.

**Figure 5** shows the WAR (%) measurements for different silicon etch rates measured after SDE and texturing process. It was observed that for DWC wafers,



**Figure 3.** (a) Reflectance of wafers measured from SWC (group A) and DWC wafer (group B) groups; (b) Reflectance of wafers measured from DWC (group C) and Black-Si wafer (group D) groups.

depending on the surface roughness, the saw mark orientation and incident angle of light beam from the spectrophotometer has an influence on the WAR measurement, similar to what was suggested in literature [10] [12]. Preferential etching during SDE and texturing processes in DWC wafers due to the predominant presence of amorphous silicon in shimmer and smooth groove regions presents a greater challenge in achieving lower WAR and improved Isc on DWC wafers [12] [13]. SWC wafers on the other hand do not have this influence in WAR measurement due to a more regular rough surface morphology. From these results, it was evident that reflectivity was lowest for 1.7  $\mu$ m (with additives) group.

**Figure 6** shows the comparison of cell efficiencies with respect to different silicon etch rates from SDE and texturing process. The average efficiencies reported here are preliminary results using a small group of 1000 cells in each etch rate group after the manufacturing line was converted from SWC to DWC wafers and without any process specific optimization done for DWC wafers. This experiment was primarily done to identify the optimum etch rate for DWC wafers which gives improved Isc and Voc performance. From **Figure 7**, it was observed that higher the etch rate, better was the Voc performance, but Isc was low



(a) DWC raw wafer with straight saw mark lines



(c) DWCwafer after texturing process



(d) DWCwafer after PECVD SiN deposition process

**Figure 4.** Schematic of DWC wafer surface showing straight and curved saw mark lines at different stages of processing.



**Figure 5.** WAR (%) measurements for different silicon etch rates after SDE and texturing process.

and for lower etch rate groups, Voc was low but Isc was observed to be high. Following this observation, it was decided to keep silicon etch rate of 1.7  $\mu$ m in SDE and texturing process in which a comparative gain in Isc and Voc was



Figure 6. DWC cell efficiency at different etch rates of texturing process.



Figure 7. Isc and Voc performance of DWC cells at different etch rates of texturing process.

observed. Reported efficiencies in **Figure 6** are low as the initial DWC wafer trials were conducted in a semi-automated cell fabrication line that involved manual handling of wafers at few processing stations.

In order to improve the overall cell efficiency using DWC wafers, a complete set of process at each stage and material trials were carried out which includes trials using wafers, additives and front contact pastes from different suppliers. Each of these process and material trials were conducted separately to realize the individual process or material contribution towards the cell efficiency gain. Figure 8 shows the cell efficiency trend towards using the DWC wafers from different suppliers indicated as A, B and C and wafer grades indicated as A-0, A-1 and B-1 respectively. Along with wafers with respective grade from different suppliers, processes from diffusion until co-firing were optimized focusing on cell efficiency improvement. Average sheet resistance (R-sheet) from diffusion process was increased from 90  $\Omega$ /sq to 105  $\Omega$ /sq with excellent process uniformity using low-pressure POCl<sub>3</sub> deposition process. Silicon nitride deposition using PECVD process was also optimized from a 2-layer deposition to a 3-layer deposition process to improve Isc and Voc. Finally, the front screen design for screen-printing was optimized from 40 µm finger opening and 95 fingers single print process to 32 µm finger opening and 111 fingers double print process,



Figure 8. Cell efficiencies of SWC and DWC wafer groups.

resulting in a significant gain in overall electrical performance of solar cells. Reported efficiencies in **Figure 8** for DWC wafers were conducted in a fully automated cell fabrication line that did not involve any manual handling of wafers at any process station.

DWC wafers saw mark orientation (pilgrim waves) plays a very significant role in determining the electrical performance of solar cells [12]. While for processes like diffusion, wet edge isolation and SiN deposition using PECVD, the orientation of DWC wafers with respect to pilgrim waves have no impact on electrical performance, however it seems to influence processes like texturing and and screen printing process. It was observed that perpendicular orientation of pilgrim waves to the flow of texturing acid bath resulted in non-uniform etching on wafers. Also at screen printing process, the perpendicular orientation of pilgrim waves to the screen printed fingers resulted in poor fill factor due to distorted finger pattern printed over the smooth groove regions present on DWC wafer surface. **Figure 9** shows the DWC wafers orientation that needs to be followed at each process station in a completely automated cell fabrication line in order to get a "parallel" orientation between the wafers saw marks and screen printed fingers.

An experiment was conducted in the semi-automatic cell fabrication line using "parallel" and "perpendicular" orientation of DWC wafer saw marks with respect to screen-printed grid lines. From the results shown in **Table 1**, it can be observed that fill factor (FF) for perpendicular orientation group was severely affected due to poor ohmic contacting which is also indicative from the series resistance of this group cells. Several trials were conducted to validate this observation of wafer saw mark orientation influence on cell electrical results and all yielded similar results.

B-Si wafers from group D were processed into solar cells and electrical performance was compared with DWC wafers from group C. Since the MCCE process was carried out at the wafer supplier end and wafers were procured as textured, it was difficult to maintain a consistent texturing quality on incoming wafers. Poor texturing quality on B-Si wafers will result in non-uniform diffusion and SiN deposition process [15]. **Figure 10** shows the poor texturing quality on B-Si wafers resulting in non-uniformity of SiN color after PECVD process.



**Figure 9.** DWC wafers saw mark orientation at each processing stage in solar cell fabrication line.



(a) B-Si wafer with poor texturing quality (b) Poorly textured B-Si wafers resulting in non-uniform SiN deposition

**Figure 10.** Schematic of B-Si wafers showing poor textured regions and subsequently resulting in non-uniform SiN layers.

**Table 1.** Electrical results of DWC cells produced in parallel and perpendicular orientation of saw marks with respect to screen-printed grid lines.

Parameters	Parallel orientation	Perpendicular orientation				
Voc (mV)	631.16	630.0				
Isc (A)	8.71	8.67				
FF (%)	79.77	69.73				
Rsh (Ω)	306	550				
Rs (mΩ)	4.63	6.5				
Vmp (mV)	534.4	508.9				
Imp (A)	8.21	7.49				
IRev1 (A)	0.190	0.790				
IRev2 (A)	0.300	1.110				

**Figure 11** shows the comparative reflectivity for SWC, DWC and B-Si wafers after SiN deposition using PECVD process.

From these results, it can be observed that the reflectivity of B-Si wafer is lower in shorter wavelength region as compared to SWC or DWC wafer, thereby



**Figure 11.** WAR (%) measurements for SWC, DWC and B-Si wafers after SiN deposition using PECVD process.

helping with maximum absorption of light and boosting the Isc performance of solar cells [16]. In the longer wavelength region, the reflectivity of B-Si wafer shows a similar trend as SWC as compared to DWC wafers.

The electrical results of cells produced using DWC wafers from group 3 and B-Si wafers from group 4 are summarized in Figure 12. Several trials were conducted for B-Si wafers to identify the best recipe for cleaning process by trying different chemical ratios of KOH, HF and HCl and ozone treatment from wet edge isolation process on as-textured B-Si wafers from the supplier, which are indicated as T-1 to T-10 in Figure 12(a). Diffusion, PECVD and Screen-printing processes were also optimized to improve the overall electrical performance of the device, which are indicated as trials from T11 to T15 in Figure 12(a). Diffusion process was optimized to improve the R-sheet uniformity across the wafers and increase the average R-sheet from 90  $\Omega/sq$  to 105 $\Omega/sq$  by using low-pressure POCl<sub>3</sub> deposition process. PECVD process was also optimized from a two-layer SiN deposition to a three-layer deposition process. All these process improvements were applied to both group-3 and group-4 wafers, results of which for B-Si wafers are shown in Figure 12(b). The cumulative effort of process optimization at each step lead to achieve a consistent average efficiency of 18.96% in mass scale production, showing an efficiency gain of 0.3% to 0.4% over DWC cells. Electrical results of pilot production using DWC and B-Si cells group are summarized as shown in Table 2.

## 4. Conclusion

In this work, the challenges of processing diamond wire cut and black silicon wafers in a large-scale manufacturing environment were discussed. A detailed experiment to process wafers for solar cells using both these wafer types was discussed. Study on surface morphology and reflectivity measurements shows the texturing quality and optical behavior of these wafer surfaces when compared to conventional slurry wafers. The importance of saw mark orientation dominant in DWC wafers with respect to the wafer orientation followed at each processing step and its influence on electrical results was discussed. A summary of process optimization carried out at every processing station and a trial to test the wafer quality from multiple suppliers were discussed leading to an overall





(a) a Average efficiency of B-Si trial group cells

(b) b Average efficiency of B-Si with respect to process trials in mass production



Cells	Avg. Eff (%)	Voc (mV)	Isc (A)	FF (%)	Rsh (Ω)	Rs (m $\Omega$ )	Vmp (mV)	Imp (A)	IRev1 (A)	IRev2 (A)	Qty (no's)
DWC	18.59	636.5	8.96	80.10	341	2.12	539.8	8.46	0.116	0.218	23398
B-Si	18.96	635.4	9.10	80.56	516	1.25	541.2	8.61	0.104	0.180	25595

Table 2. Electrical results summary of DWC (group 3) and B-Si (group 4) cells.

efficiency improvement of up to 18.75% using DWC wafers and up to 18.96% using B-Si wafers. An efficiency improvement of 0.37% was realized in this work for B-Si cells as compared to DWC wafers with more than 100 mA improvement observed in Isc. The quality of wafers plays a crucial role in determining the cell efficiency and with a correct set of processes in place; it is possible to achieve an average efficiency of over 19% for standard Al-BSF multi-crystalline solar cells in a solar cell manufacturing industry. The reported work can be an interesting read for any PV large-scale manufacturing company, which deals with DWC and B-Si wafers, overcoming the challenges associated with these wafers to produce high efficiency multi-crystalline cells.

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## **Conflicts of Interest**

The authors declare no conflicts of interest regarding the publication of this paper.

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