Scientific Research Publishing

Journal of Power and Energy Engineering, 2025, 13(9), 95-116
https://www.scirp.org/journal/jpee
ISSN Online: 2327-5901
ISSN Print: 2327-588X

Comparative Study of Sinusoidal PWM Strategies in Cascaded Multilevel Inverters

Muhammad Syazreen Samsudin[1], Azrita Alias[1*], Nurul Ain Mohd Said[1], Fazlli Patkar[1], Jurifa Mat Lazi[1], Md Hairul Nizam Bin Talib[1], Muhammad Zaid Aihsan[2]

[1]Faculty of Electrical Technology and Engineering, Universiti Teknikal Malaysia Melaka, Melaka, Malaysia
[2]Faculty of Electrical Engineering Technology, University Malaysia Perlis (UniMAP), Perlis, Malaysia
Email: *azrita@utem.edu.my

How to cite this paper: Samsudin, M.S., Alias, A., Said, N.A.M., Patkar, F., Lazi, J.M., Talib, M.H.N. and Aihsan, M.Z. (2025) Comparative Study of Sinusoidal PWM Strategies in Cascaded Multilevel Inverters. *Journal of Power and Energy Engineering*, **13**, 95-116.
https://doi.org/10.4236/jpee.2025.139007

Received: August 9, 2025
Accepted: September 6, 2025
Published: September 9, 2025

Abstract

This paper presents a comparative study of four Sinusoidal Pulse Width Modulation (SPWM) strategies Phase Disposition (PD-PWM), Phase Opposition Disposition (POD-PWM), Alternate Phase Opposition Disposition (APOD-PWM), and a Modified SPWM applied to Cascaded H-Bridge Multilevel Inverter (CHMI) systems. MATLAB/Simulink is used to simulate both 5-level and 11-level CHMI configurations, focusing on output voltage quality and total harmonic distortion (THD) as performance metrics. The analysis is conducted by varying two key control parameters: modulation index (0.5 to 1.0) and switching frequency (5 kHz, 10 kHz, 20 kHz). The results show that increasing voltage levels is the most effective way to improve waveform quality, while modulation strategy plays a minor role. POD and APOD offer slight THD advantages, and Modified SPWM performs almost identically to PD-PWM, making it a simpler alternative for practical CHMI applications. The findings provide a practical guideline for selecting appropriate SPWM strategies in high-performance inverter applications such as electric vehicles, industrial drives, and renewable energy systems.

Keywords

Cascaded H-Bridge Multilevel Inverter (CHMI), Sinusoidal Pulse Width Modulation (SPWM), PD-PWM, POD-PWM, APOD-PWM, Modified SPWM, Total Harmonic Distortion (THD), Modulation Index, Switching Frequency, MATLAB/Simulink

1. Introduction

Rapid technological advancements and global population growth are placing increasing pressure on energy sustainability, making it one of the world's most press-

ing challenges. The continued reliance on fossil fuels for power generation poses significant risks due to limited resource availability and the environmental consequences of greenhouse gas (GHG) emissions [1]. These concerns underscore the urgent need for innovative energy solutions that balance environmental, economic, and societal priorities [2].

In this context, multilevel inverters have emerged as a critical enabling technology in modern power electronic systems. They are widely employed in industrial motor drives, electric vehicles (EVs), and renewable energy systems due to their ability to enhance energy efficiency and system performance through precise voltage control and reduced power losses [3] [4]. Notably, multilevel inverters offer the advantage of producing high-quality output voltage with lower total harmonic distortion (THD), which is essential for maintaining power quality in sensitive applications [5]-[7].

Among the various topologies, the Cascaded H-Bridge Multilevel Inverter (CHMI) is particularly favored for its modular design, scalability, and ability to synthesize near-sinusoidal waveforms using multiple H-bridge cells, each fed by an independent DC source [8] [9]. This makes CHMI suitable for applications requiring high voltage and low harmonic distortion without relying heavily on output filters.

To achieve optimal voltage regulation and minimize harmonic content, Pulse Width Modulation (PWM) techniques are commonly employed. Among them, Sinusoidal PWM (SPWM) stands out for its simplicity and effectiveness in generating high-quality waveforms. Several SPWM variants such as Phase Disposition (PD-PWM), Phase Opposition Disposition (POD-PWM), and Alternate Phase Opposition Disposition (APOD-PWM) have been developed, each characterized by different arrangements of carrier and reference signals. These variations influence the inverter's switching behavior and overall harmonic performance.

More recently, Modified SPWM techniques, which use a single triangular carrier and multiple sinusoidal reference signals, have gained attention for offering reduced implementation complexity while still maintaining acceptable output waveform quality. However, comprehensive performance comparisons of traditional and modified SPWM strategies under varying operating conditions remain limited in the literature.

The project addresses that gap by presenting a simulation-based comparison of four SPWM strategies, PD, POD, APOD, and Modified SPWM applied to 5-level and 11-level CHMI systems using MATLAB/Simulink. The performance is evaluated in terms of Total Harmonic Distortion (THD) and output voltage stability across a range of modulation index (MI) and switching frequencies (Fs). The goal is to provide practical insights into the selection of optimal modulation strategies for high-performance inverter applications in renewable energy systems, electric vehicle drives, and industrial automation.

2. Methodology

The performance of four Sinusoidal Pulse Width Modulation (SPWM) techniques

applied to Cascaded H-Bridge Multilevel Inverter (CHMI) systems is analyzed through a structured methodology involving system modeling, control strategy implementation, and simulation-based evaluation. The methodology includes the development of two inverter configurations: a 5-level CHMI comprising two cascaded H-bridge cells, and an 11-level CHMI comprising five cascaded H-bridge cells. Both systems are simulated using MATLAB/Simulink under varying modulation indices and switching frequencies to assess their voltage output and harmonic distortion characteristics. The overall simulation workflow is illustrated in Figure 1.

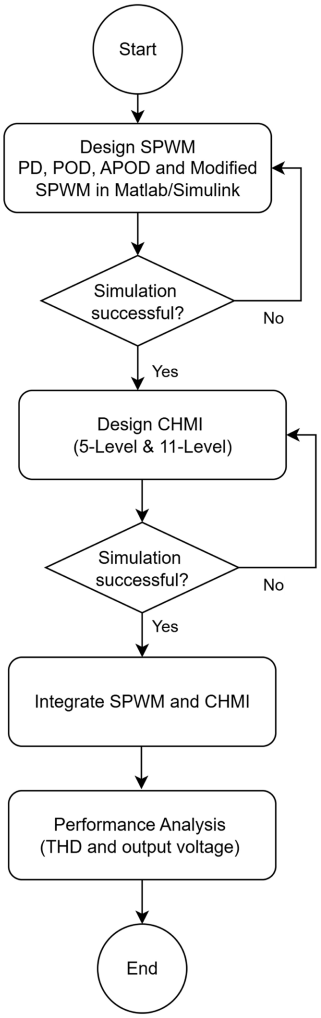


Figure 1. Simulation workflow for evaluating SPWM strategies in CHMI systems, including system modeling, implementation, and performance analysis using MATLAB/Simulink.

2.1. System Design and Configuration

Two CHMI topologies were constructed using independent DC sources for each H-bridge module to enable stepped voltage synthesis. A resistive load of 5 Ω is connected to the inverter output to simplify waveform analysis. The system is de-

signed to operate in single-phase mode, and MOSFETs are used as switching elements due to their fast response and efficiency. The block diagram of the 5-level CHMI is shown in Figure 2, comprising two cascaded H-bridge cells powered by separate DC sources. The 11-level CHMI configuration, depicted in Figure 3, consists of five cascaded H-bridge cells, enabling bigger voltage level resolution for reduced harmonic distortion.

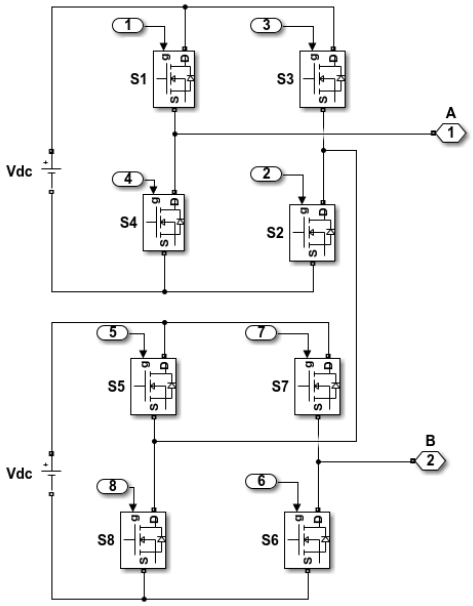


Figure 2. The block diagram of the CHMI configuration (5-level), showing the arrangement of H-bridge cells powered by independent DC source.

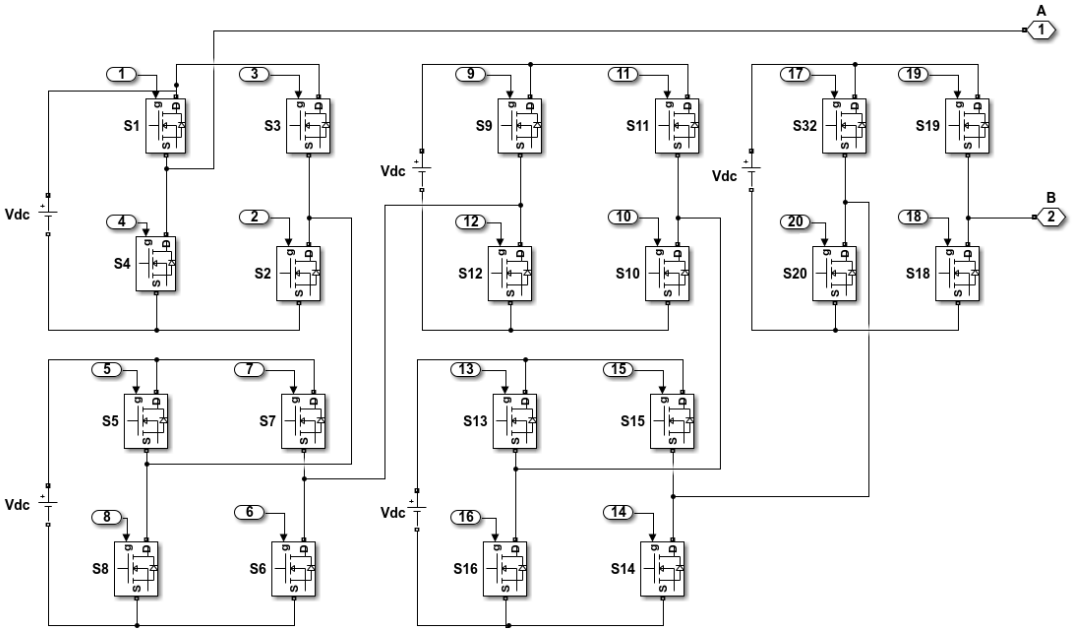


Figure 3. The block diagram of the CHMI configuration (11-level), showing the arrangement of H-bridge cells powered by independent DC sources.

2.2. System Strategies and Parameters

Four SPWM techniques were implemented for performance comparison: (1) Phase Disposition (PD-PWM): All carrier signals are in phase. (2) Phase Opposition Disposition (POD-PWM): Carrier signals above and below the zero axis are 180˚ out of phase. (3) Alternate Phase Opposition Disposition (APOD-PWM): Adjacent carriers are alternately phase-shifted by 180˚. (4) Modified SPWM: Uses a single triangular carrier with multiple sinusoidal reference signals. The switching signals for the 5-level Cascaded H-Bridge Multilevel Inverter (CHMI) were developed using a carrier-based SPWM logic. As shown in Figure 4, a sinusoidal reference signal is scaled by the modulation index to control the amplitude of the output waveform. This reference is then compared with multiple triangular carrier signals to generate the gate pulses for the inverter switches.

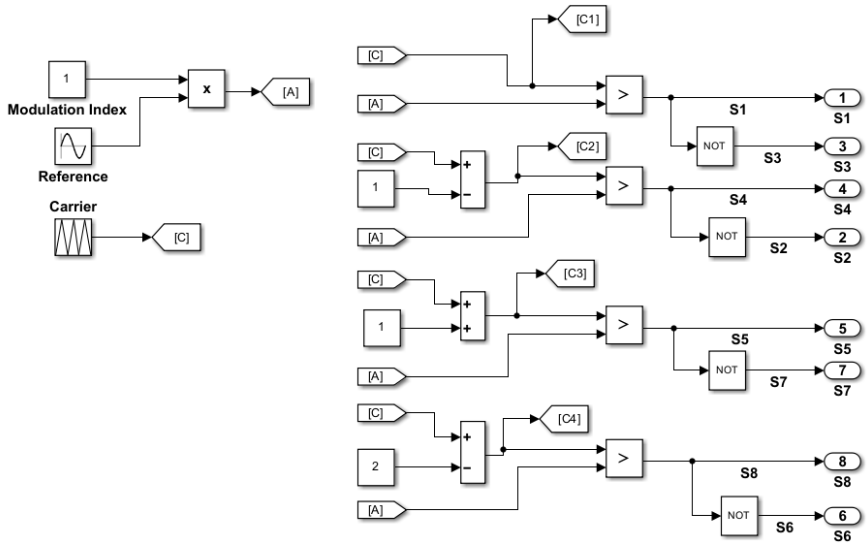


Figure 4. Simulink-based implementation of SPWM switching logic for 5 CHMI using Phase Disposition (PD-PWM).

For the Phase Disposition (PD-PWM) strategy, all carrier signals are in phase and vertically fixed. Each comparison block determines whether the reference exceeds the corresponding carrier. A logical NOT gate is used to generate the complementary gate signal for the opposing switch in each H-bridge cell, ensuring proper inverter operation and avoiding shoot-through conditions. This configuration supports up to eight switches (S1 - S8), controlling four H-bridge legs. The output from each comparator triggers a gate signal depending on the condition $A > C_n$, where A is the amplitude-modulated reference, C_n is the nth carrier signal level.

To implement POD-PWM and APOD-PWM, only the phase configuration of the triangular carrier signals needs to be adjusted. In the POD approach as shown in Figure 5, carrier signals positioned above and below the zero reference are phase-shifted by 180˚. For APOD as indicated in Figure 6, each adjacent carrier signal is alternately shifted by 180˚, resulting in a more even distribution of switch-

ing transitions and improved harmonic dispersion. This modular setup enables flexible adaptation between different SPWM strategies with minimal modifications to the Simulink model structure.

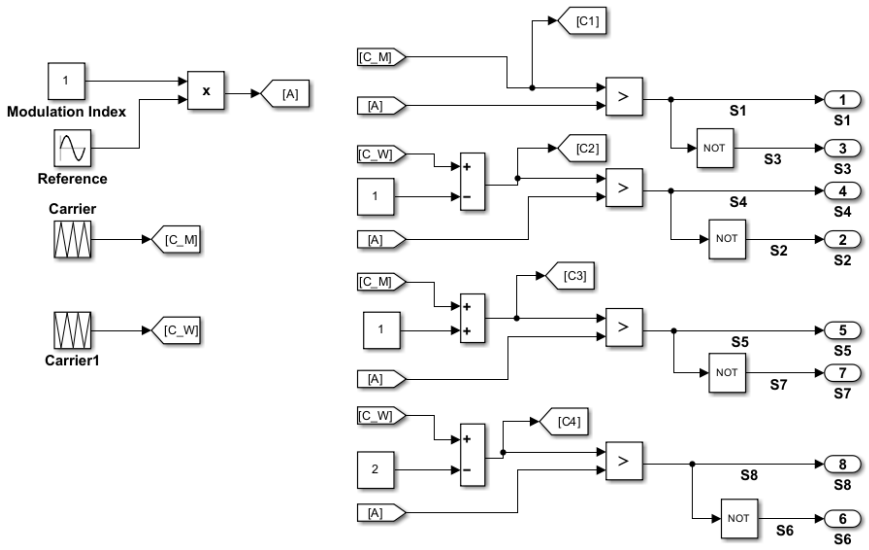


Figure 5. Simulink-based implementation of SPWM switching logic for CHMI using Phase Disposition (POD-PWM).

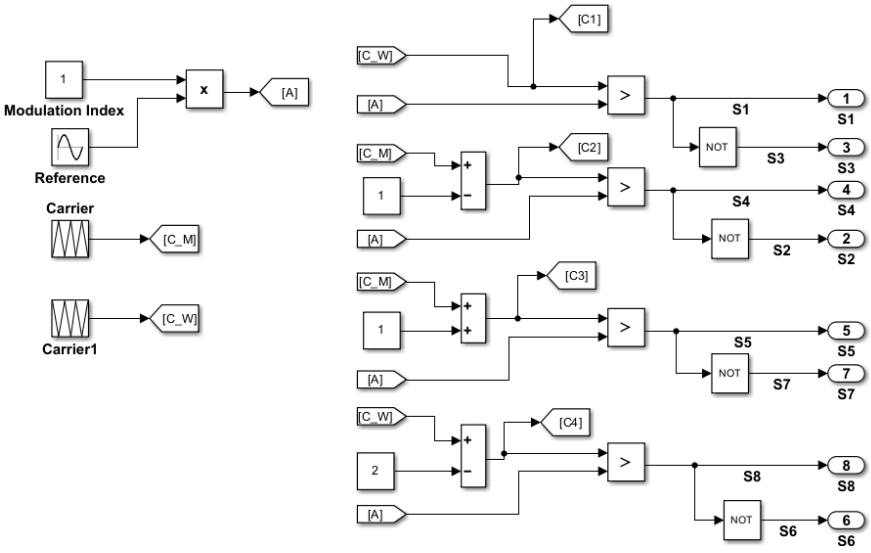


Figure 6. Simulink-based implementation of SPWM switching logic for CHMI using Phase Disposition (APOD-PWM).

The Modified Sinusoidal Pulse Width Modulation (SPWM) technique uses a single triangular carrier signal compared against multiple sinusoidal reference signals to generate gate pulses for each inverter switch, as shown in Figure 7. As shown in the diagram, the reference signal is first scaled by the modulation index to set the desired output voltage amplitude. Then, additional offsets are added to the reference to generate multiple reference waveforms (Ref1, Ref2, Ref3, and

Ref4) corresponding to each H-bridge level. Each modified reference is compared with the same carrier signal. The result of each comparison produces a switching pulse (e.g., S1, S2, S3, ..., S8) that controls a pair of power switches in the CHMI circuit. A logical NOT gate is used to generate the complementary signal for the lower switch in each H-bridge leg. This method simplifies the control structure by using only one carrier signal instead of multiple, as required in conventional multi-carrier SPWM techniques (like PD, POD, or APOD). Despite its simplicity, it still produces acceptable output voltage levels and switching behavior for multilevel inverter operation.

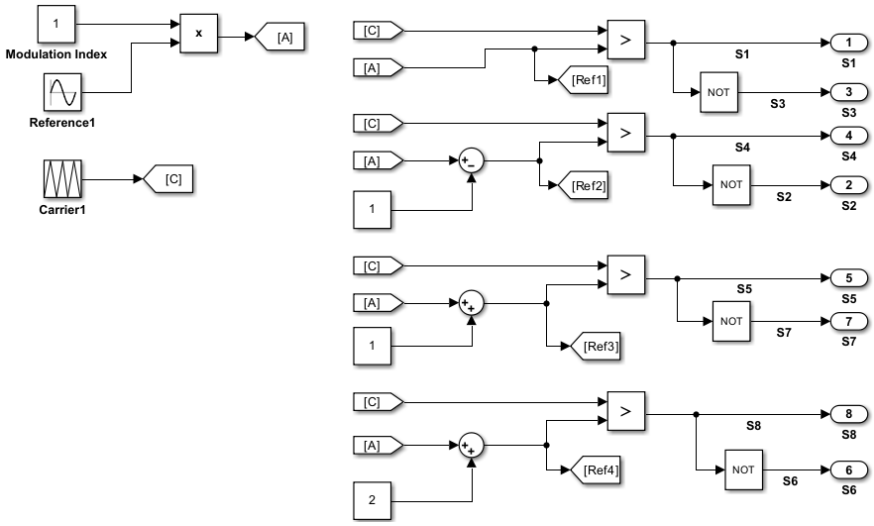


Figure 7. Modified SPWM using one carrier and several reference signals to generate switching pulses.

The simulation results in Figures 8(a)-8(d) display the carrier and reference waveforms used to generate switching signals for four different SPWM techniques, based on a 50 Hz sinusoidal reference signal. The sampling frequency and carrier frequency were both set to 1 kHz, ensuring sufficient resolution for accurate pulse generation and waveform analysis. In PD-PWM, all triangular carriers are aligned in phase, resulting in symmetrical and uniform switching. POD-PWM introduces a 180˚ phase shift between carriers above and below the zero axis, which helps cancel certain harmonics and balances switching across the positive and negative half cycles. In APOD-PWM, each adjacent carrier is phase-shifted by 180˚, leading to more evenly distributed switching events and smoother voltage transitions.

Modified SPWM shows a different structure, where a single triangular carrier is compared against multiple phase-shifted sine references. This approach reduces control complexity while maintaining acceptable switching performance. Overall, these waveforms demonstrate the impact of carrier arrangement on switching behavior, which directly affects the output voltage quality and harmonic distortion of the inverter.

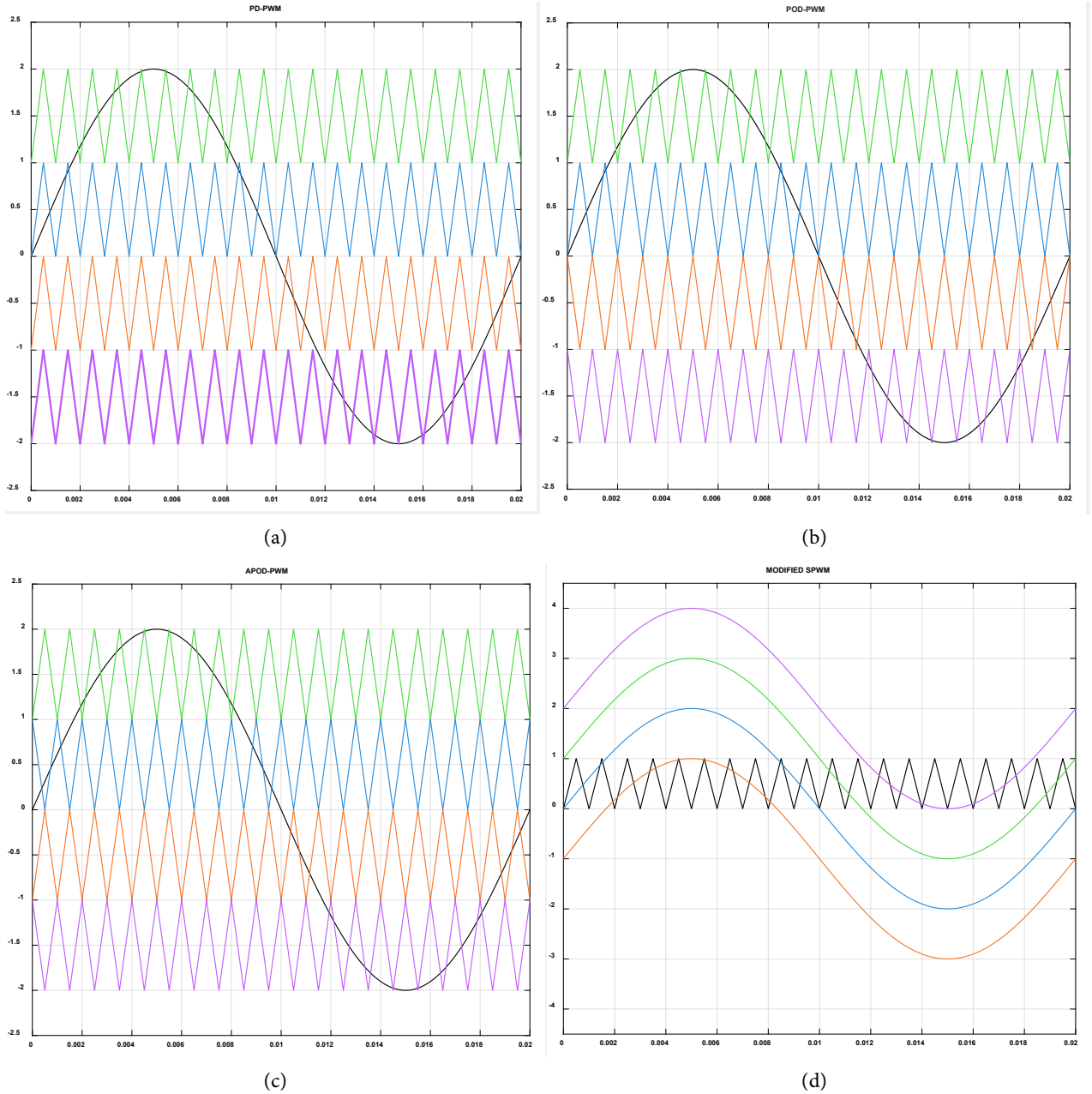


Figure 8. Simulation results showing reference and carrier waveforms for different SPWM techniques: (a) PD-PWM (b) POD-PWM (c) APOD-PWM (d) Modified SPWM.

2.3. Performance Evaluation Metrics

The performance of each SPWM strategy was assessed based on two critical output parameters which is Total Harmonic Distortion (THD) and Root Mean Square Output Voltage (V_{rms}). These metrics provide a quantitative measure of the power quality, waveform integrity, and efficiency of the multilevel inverter under different control conditions.

2.3.1. Total Harmonic Distortion (THD)

THD is a widely accepted parameter for evaluating the waveform quality of in-

verter outputs. It measures the deviation of the output voltage from a pure sinusoidal waveform due to the presence of harmonic components. A lower THD indicates better power quality and reduced stress on connected loads, especially in sensitive applications such as motor drives and grid-tied renewable systems [10] [11]. THD is calculated using the following formula:

$$\text{THD} = \sqrt{\frac{\sum_{n=2}^{\infty} V_n^2}{V_1^2}} \times 100\% \tag{1}$$

where, V_1 is the RMS (Root Mean Square) value of the fundamental frequency component, V_n is the RMS value of the *n*th harmonic component (for $n = 2,3,4,\cdots$). In MATLAB/Simulink, THD values were computed using the Powergui FFT Analysis Tool and voltage scope output signals.

2.3.2. RMS Output Voltage (THD)

The output voltage of a multilevel inverter is a critical parameter in determining its suitability for various applications. A higher RMS value typically indicates more efficient use of the DC link voltage and better voltage transfer to the load. The RMS voltage of the inverter output is calculated using:

$$V_{rms} = V_p \sqrt{\frac{M_a}{2}} \tag{2}$$

where, V_p is the peak amplitude of the output voltage waveform, M_a is the modulation index and defined by,

$$M_a = \frac{A_{ref}}{A_c} \tag{3}$$

A_{ref} is the peak amplitude of the sinusoidal reference signal, and A_c is the peak of the triangular carrier signal [12].

Modulation index values influence the output waveform linearity, with values below 1.0 operating in the linear region. Overmodulation (*i.e.* $M_a > 1$) introduces distortion and is avoided in this study. Maintaining an optimal modulation index is essential to balance output voltage and waveform quality.

2.3.3. Switching Frequency Impact

Switching frequency (f_s) refers to the frequency of the triangular carrier signal used in Sinusoidal Pulse Width Modulation (SPWM). It is a key parameter in determining the resolution of the output waveform and the inverter's dynamic response. A higher switching frequency increases the number of switching events per cycle, resulting in a waveform that more closely resembles a pure sinusoidal output and typically yields lower Total Harmonic Distortion (THD). Despite these advantages, increasing the switching frequency introduces trade-offs. Higher leads to greater switching losses, increased electromagnetic interference (EMI), and elevated thermal stress on power electronic devices. These effects can reduce system efficiency and require additional cooling or thermal management solutions [13] [14].

2.4. Motor-Equivalent RL Load

A purely resistive load is used as a baseline for fair comparison of modulation strategies. To verify practical relevance, a motor-equivalent series RL load is introduced with a target lagging power factor representative of drive applications [15]. Parameter selection. For a desired power factor, $pf = \cos\varphi$ at fundamental frequency f, the RL parameters satisfy:

$$\cos\varphi = \frac{R}{\sqrt{R^2 + (2\pi fL)^2}}; \quad L = \frac{R\tan\varphi}{2\pi f} \tag{8}$$

In this study the R identical to the resistive baseline and set $pf = 0.8$ (lagging) at $f = 50$ Hz, yielding $L \cong 50$ mH.

3. Result and Discussion

This section presents the simulation results for four SPWM strategies: PD-PWM, POD-PWM, APOD-PWM, and Modified SPWM. Each SPWM technique was applied to both 5-level and 11-level CHMI configurations. The number of output voltage levels (n) is calculated using the standard multilevel inverter formula:

$$n = 2l + 1 \tag{4}$$

where l represents the number of cascaded H-bridge cells per phase. Based on this, the 5-level inverter uses 2 H-bridge modules, and the 11-level inverter uses 5 H-bridge modules connected in cascaded, each powered by a separate DC source (15). The analysis focuses on output voltage waveform characteristics, total harmonic distortion (THD), and the effects of varying modulation index and switching frequency.

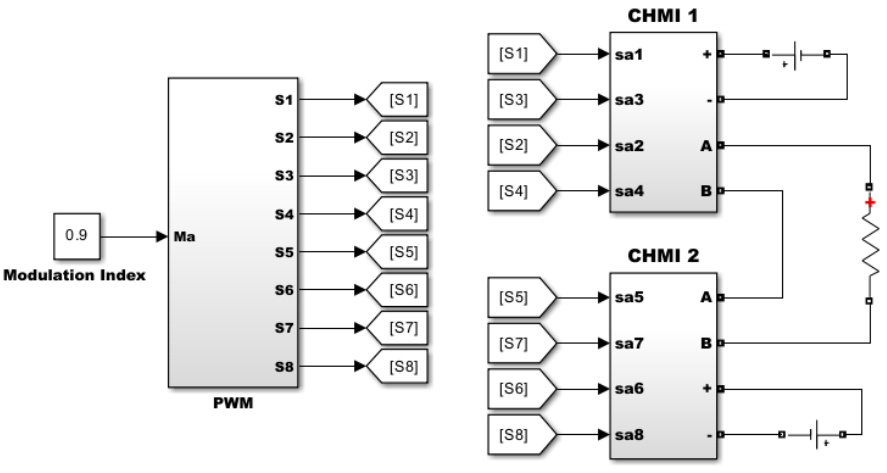


Figure 9. MATLAB/Simulink implementation of a 5-level Cascaded H-Bridge Multilevel Inverter (CHMI).

Figure 9 and Figure 10 The 5-level inverter is constructed using two cascaded H-bridge cells per phase, resulting in five output voltage levels. Each H-bridge is supplied by an isolated DC source. The system includes eight switching devices

(Sa1 - Sa8), with PWM signals generated from a modulation block based on the selected SPWM strategy and modulation index. The output voltage (V_o) and load current (I_o) are measured across a purely resistive load.

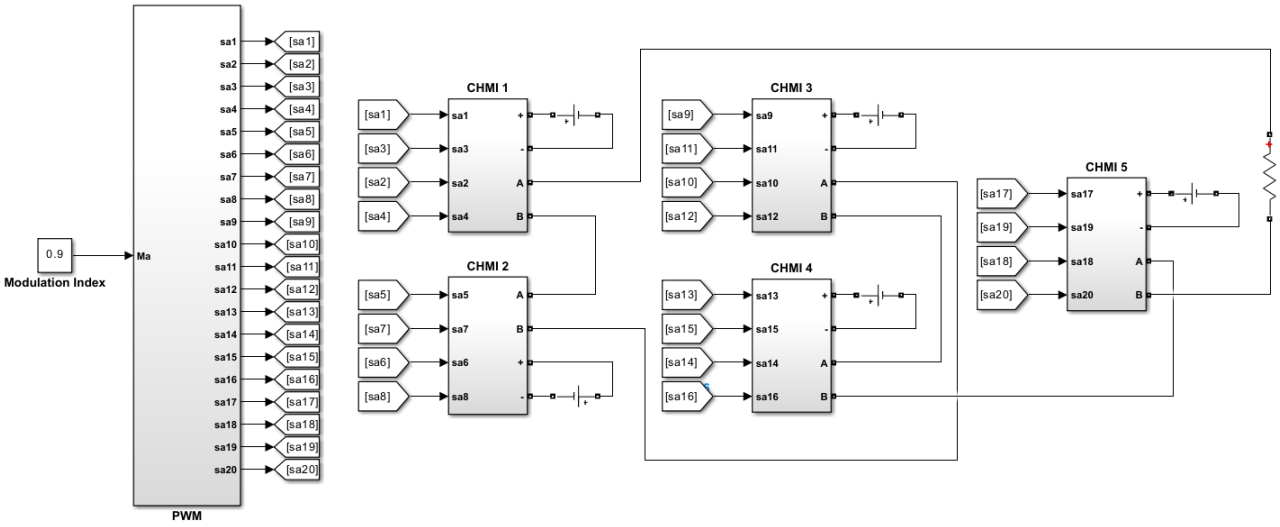


Figure 10. MATLAB/Simulink implementation of a 11-level Cascaded H-Bridge Multilevel Inverter (CHMI).

For the 11-level inverter, the model includes five cascaded H-bridge cells per phase, producing eleven distinct voltage levels. A total of 20 switching devices are used (four per H-bridge cell), each controlled by dedicated gate signals. As in the 5-level setup, each cell is powered by an independent DC source, and switching signals are generated based on the selected SPWM technique. Voltage and current measurement blocks are included for waveform analysis and harmonic distortion evaluation.

3.1. Output Voltage Waveform Analysis

The performance of four SPWM techniques, PD-PWM, POD-PWM, APOD-PWM, and Modified SPWM was evaluated in terms of output voltage waveform and switching behavior. Simulations were conducted using both 5-level and 11-level CHMI configurations under fixed conditions: a modulation index of 0.9, a switching frequency of 10 kHz, and a 50 Hz sinusoidal reference. Each H-bridge cell was supplied with a 100 V DC source, and the inverter output was connected to a 10 Ω resistive load. A 100 V DC source was chosen for numerical stability and per-unit comparability; the cascaded H-bridge scales to typical EV buses (≈400 - 800 V) and grid-level DC (≈600 - 1000 V) by increasing series DC sources with the same per-unit control and THD/loss trends.

Figure 11 presents the stepped output voltage waveforms for PD-PWM, POD-PWM, APOD-PWM, and Modified SPWM techniques using a 5-level CHMI. All four methods generate consistent five-level output with similar voltage steps and switching characteristics. The waveform shapes are nearly identical, indicating comparable performance in generating multi-level outputs at this configuration.

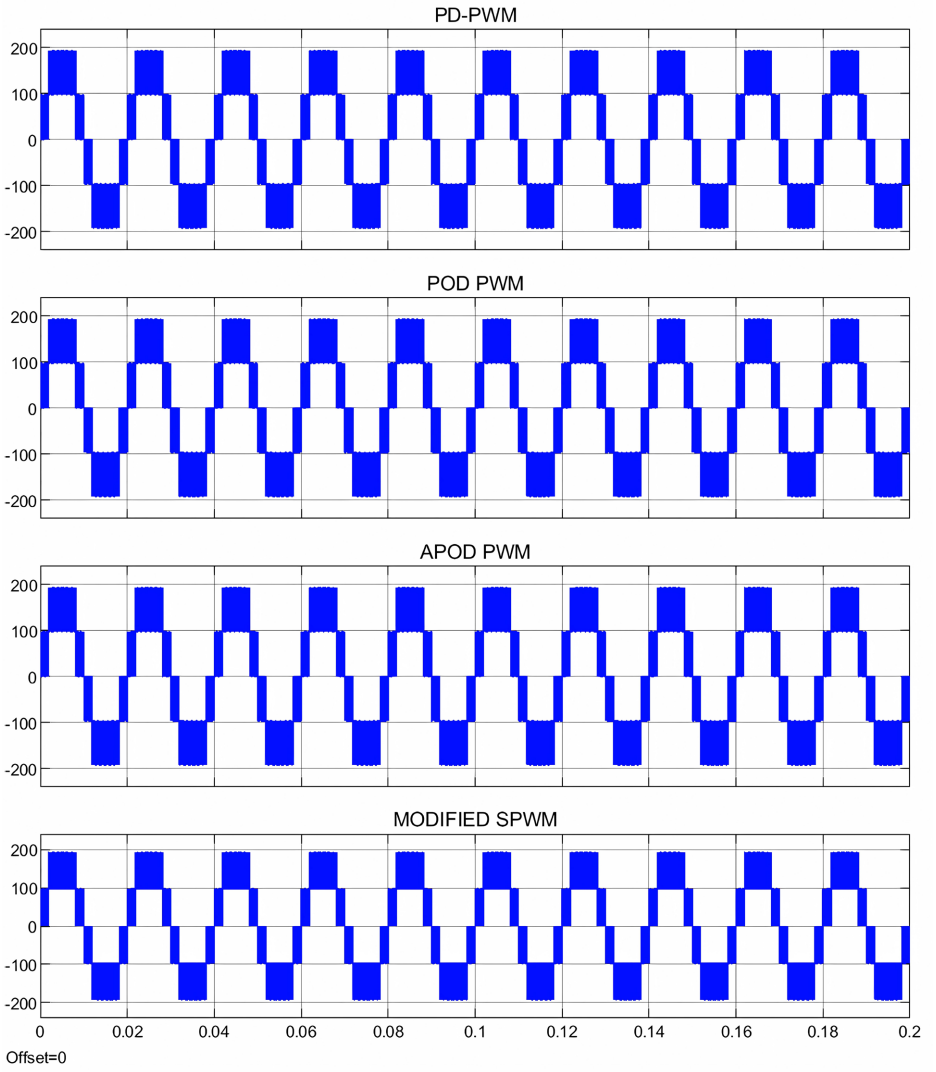
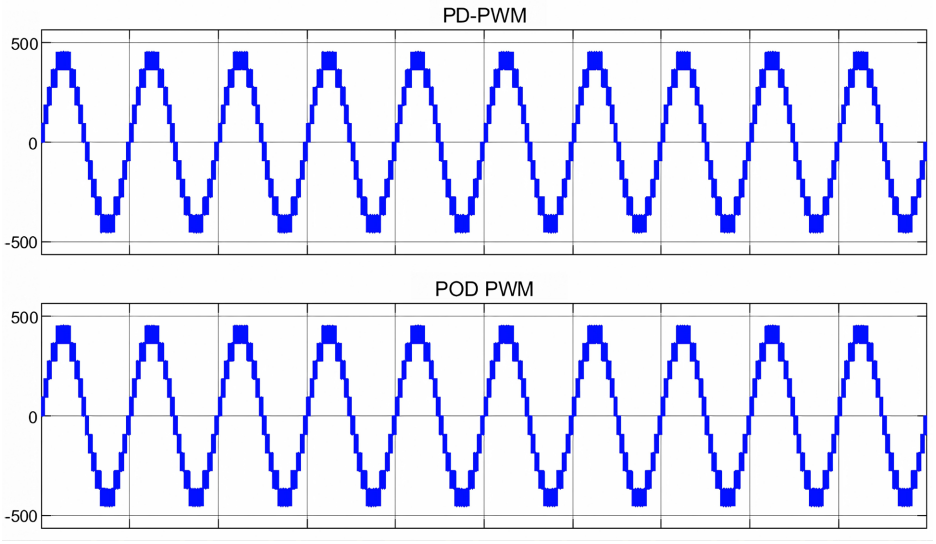


Figure 11. Simulation results showing the output voltage waveforms using PD-PWM, POD-PWM, APOD-PWM, and Modified SPWM for 5-level.



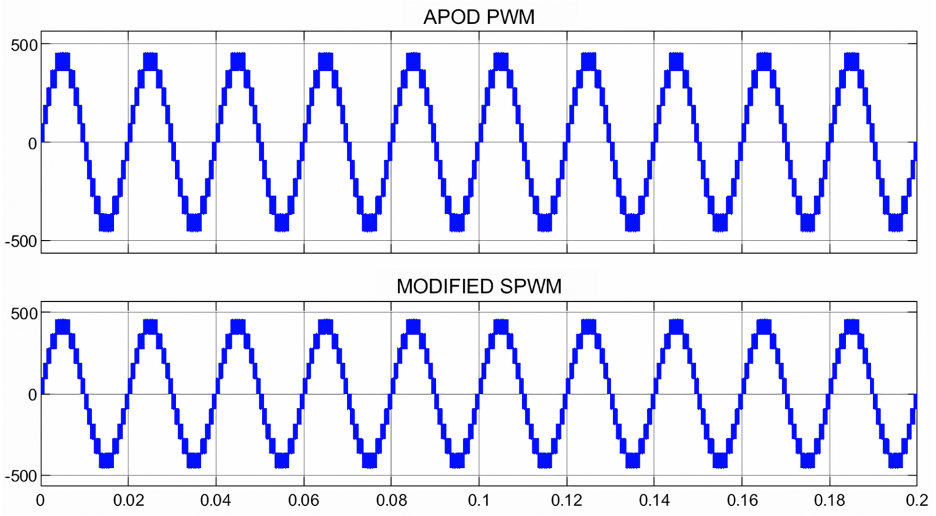


Figure 12. Simulation results showing the output voltage waveforms using PD-PWM, POD-PWM, APOD-PWM, and Modified SPWM for 11 level.

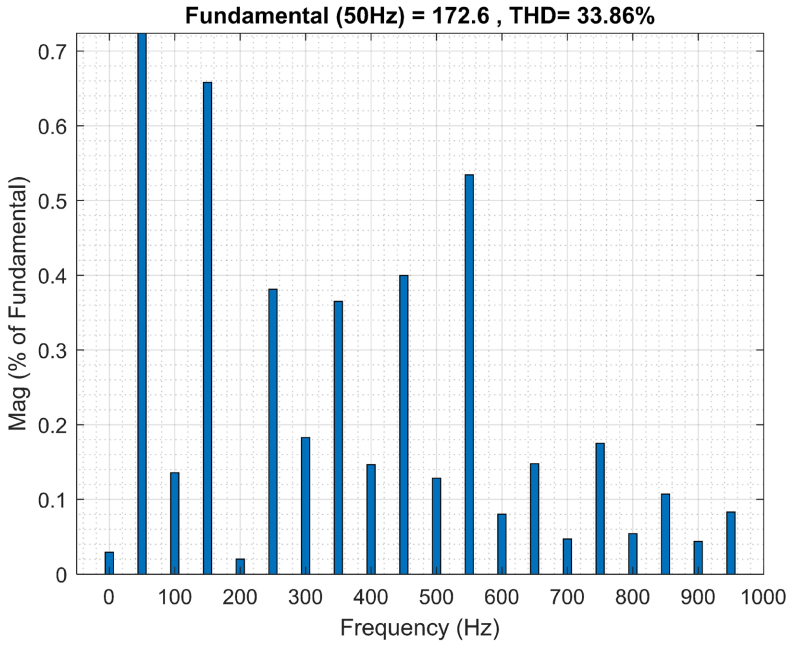
Figure 12 shows the output voltage waveforms for the same PWM techniques using an 11-level CHMI. With increased voltage levels, the output becomes more sinusoidal, and the stair-step effect is significantly reduced. Again, the waveforms from all four techniques appear visually similar, producing smooth and symmetrical outputs. This suggests that, for both 5-level and 11-level inverter configurations, the different modulation strategies result in comparable output quality, and further analysis such as FFT or THD is needed to highlight any performance difference.

3.2. Harmonic Distortion Performance

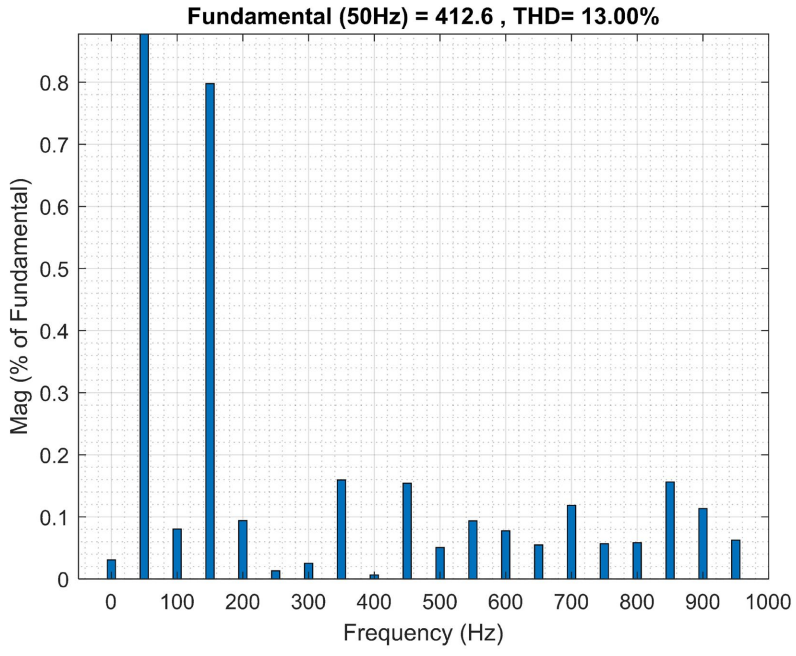
Figure 13(a) and Figure 13(b) show the harmonic spectrum of the output voltage for PD-PWM applied to both 5-level and 11-level CHMI configurations, respectively. In the 5-level CHMI, the output contains significant harmonic components, especially at lower and mid-order frequencies. The fundamental amplitude at 50 Hz is 172.6, and the THD is 33.86%, indicating considerable waveform distortion. This level of distortion is expected due to the limited number of voltage steps, which results in larger jumps between levels and more harmonic content in the output. In contrast, the 11-level CHMI shows a much cleaner output waveform. The fundamental component is 412.6, and the THD drops to 13.00%. With more voltage levels, the inverter can more closely approximate a sinusoidal waveform, reducing the magnitude of harmonic components significantly. The switching frequency of 10 kHz contributes to the high resolution of the PWM signal, while the modulation index of 0.9 ensures full utilization of the DC supply range.

Table 1 summarizes the Total Harmonic Distortion (THD) for four SPWM strategies applied to both 5-level and 11-level CHMI systems. Across all methods, the 11-level inverter shows significantly lower THD values compared to the 5-level configuration. The lowest THD was observed in POD-PWM and APOD-

PWM for the 11-level CHMI at 12.94%, indicating improved harmonic performance due to finer voltage steps. In contrast, all techniques resulted in THD values around 33% - 34% for the 5-level inverter, confirming that increasing the number of levels is more impactful than the modulation strategy itself when it comes to reducing harmonic distortion.



(a)



(b)

Figure 13. Harmonic spectrum of output voltage using PD-PWM with M_a = 0.9, f_s = 10 kHz, and 100 V DC per cell (a) 11-level CHMI (b) 5-level CHMI.

Table 1. Comparison of total harmonic distortion (THD) for different SPWM techniques in 5-level and 11-level CHMI inverters.

Switching techniques	Total harmonic distortion (THD)	
	5-level	11-level
PD-PWM	33.86%	13.00%
POD-PWM	34.01%	12.94%
APOD-PWM	33.70%	12.94%
MODIFIED SPWM	33.86%	13.00%

3.3. Comparative Summary

This section provides a comparative evaluation of THD and fundamental voltage performance for four SPWM techniques—PD-PWM, POD-PWM, APOD-PWM, and Modified SPWM—applied to both 5-level and 11-level CHMI configurations. The analysis considers variations in modulation index and switching frequency to assess the impact of modulation strategy and inverter level count on output waveform quality and voltage stability. Results are presented in tables and figures to highlight performance trends and key differences between configurations.

3.3.1. Total Harmonic Distortion (THD) and Fundamental Voltage Analysis

Table 2 and Table 3 present the THD and fundamental voltage results for PD-PWM, POD-PWM, APOD-PWM, and Modified SPWM applied to 5-level and 11-level CHMI, respectively with modulation indices from 0.5 to 1.0. The DC source voltage for each H-bridge cell was set to 100 V, with a switching frequency of 10 kHz and a 50 Hz reference.

Table 2. THD (%) and fundamental voltage (V_o peak) for different modulation indices using four PWM techniques in 5-level and 5-level CHMI.

M_a	PD-PWM		POD-PWM		POD-PWM		MODIFIED SPWM	
	THD (%)	V_o (peak)	THD (%)	V_o (peak)	THD (%)	V_o (peak)	THD (%)	V_o (peak)
0.5	54.14	95.88	54.29	95.75	53.92	96.07	54.14	95.88
0.6	44.53	115.4	44.48	115.4	44.59	115.4	44.53	115.4
0.7	41.95	134.5	41.79	134.6	42.14	134.5	41.95	134.95
0.8	38.54	153.6	38.49	153.4	38.5	153.4	38.54	153.6
0.9	33.86	172.6	34.01	172.6	33.7	173	33.86	172.6
1.0	27.33	192	27.5	191.2	27.31	192	27.33	192

Table 3. THD (%) and fundamental voltage (V_o peak) for different modulation indices using four PWM techniques in 5-level and 11-level CHMI.

M_a	PD-PWM		POD-PWM		POD-PWM		MODIFIED SPWM	
	THD (%)	V_o (peak)	THD (%)	V_o (peak)	THD (%)	V_o (peak)	THD (%)	V_o (peak)
0.5	23.85	231.8	23.87	231.7	23.91	231.7	23.85	231.8
0.6	18.35	277.6	18.34	277.6	18.37	277.7	18.35	277.6

Continued

0.7	16.88	322.8	16.81	323.1	16.81	323	16.88	322.8
0.8	13.79	368.1	13.95	367.7	13.97	367.7	13.79	368.1
0.9	13	412.6	12.94	412.3	12.94	412.2	13	412.6
1.0	11.06	456.7	11.05	456.5	11.06	456.5	11.06	456.7

The 11-level CHMI achieved much lower THD values (23.85% - 11.05%) than the 5-level CHMI (54.29% - 27.53%), confirming that higher voltage levels significantly improve waveform quality. Fundamental voltage increased proportionally with modulation index, ranging from approximately 233 V to 455.9 V for the 11-level and from 95.9 V to 192 V for the 5-level system. Across all modulation indices, POD-PWM and APOD-PWM showed slightly better THD performance than PD-PWM and Modified SPWM, although differences were minimal. Modified SPWM matched the conventional methods in both THD and fundamental voltage while offering simpler implementation.

Overall, the results indicate that increasing the number of voltage levels has a greater effect on THD reduction than changing the modulation strategy, with POD and APOD providing only marginal improvements.

3.3.2. Effect of Switching Frequency on THD and Fundamental Voltage

Figure 14 illustrate the effect of switching frequency on the Total Harmonic Distortion (THD) and fundamental voltage for PD-PWM, POD-PWM, APOD-PWM, and Modified SPWM, in both 11-level and 5-level CHMI configurations. Switching frequency variation results show that the 11-level CHMI maintained low and stable THD (~13%) and nearly constant fundamental voltage (~412 V) across all SPWM methods, indicating minimal benefit from increasing frequency. In contrast, the 5-level CHMI exhibited higher THD (~33% - 35%) and lower fundamental voltage (~173 V), with only slight harmonic improvement at higher frequencies and a voltage drop for PD-PWM at 20 kHz. Overall, the number of voltage levels has a much greater influence on waveform quality than switching frequency or modulation method, with POD and APOD offering marginal THD advantages. Across all modulation indices, POD and APOD consistently delivered slightly lower THD values compared to PD-PWM. The Modified SPWM method closely matched the performance of PD-PWM in both THD and fundamental voltage, with differences being negligible in all tested cases. This indicates that Modified SPWM can serve as a simpler alternative to PD-PWM without compromising waveform quality.

Average performance trends show that the 11-level CHMI consistently delivers low THD (~13%) and stable fundamental voltage (~412 V) regardless of switching frequency, confirming that waveform quality is primarily determined by the number of voltage levels rather than frequency. In contrast, the 5-level CHMI exhibits significantly higher THD (~33% - 35%) and a gradual reduction in fundamental voltage as switching frequency increases, indicating a higher sensitivity to switching frequency changes. This highlights the advantage of higher-level inverter con-

figurations in achieving better harmonic performance and voltage stability with less dependence on switching frequency (Figure 15).

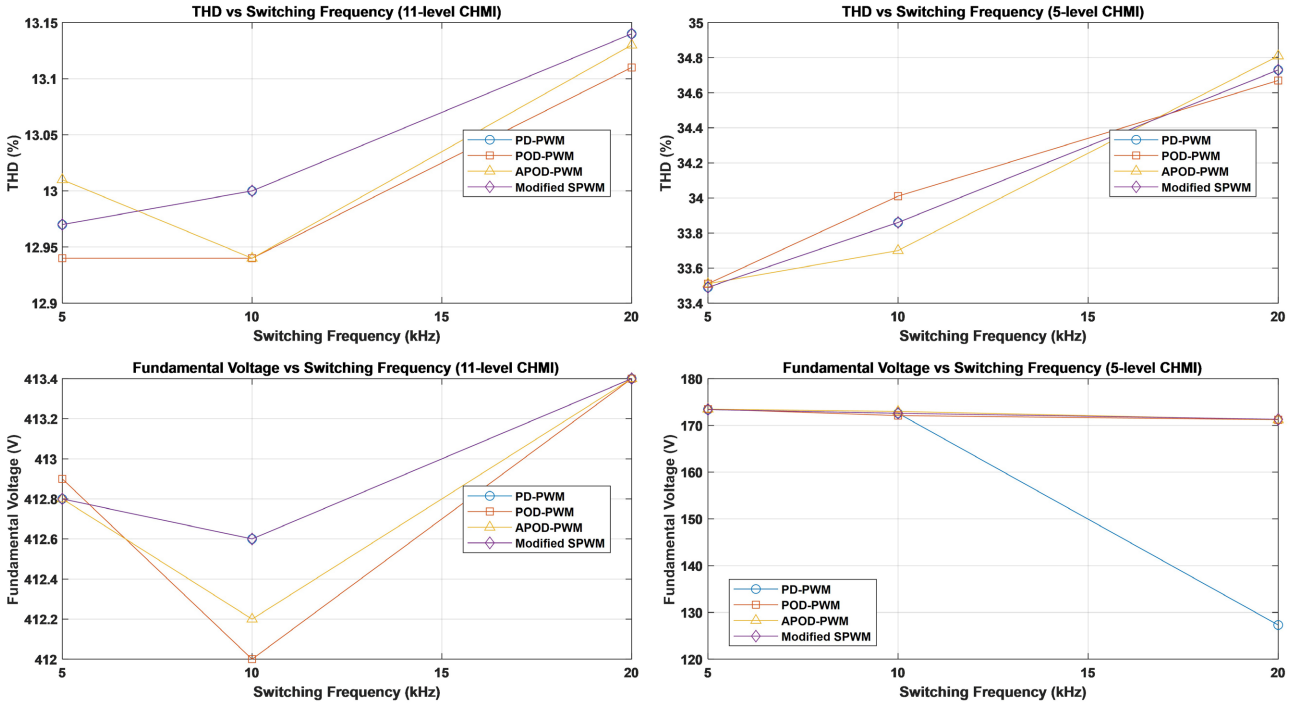


Figure 14. THD and fundamental voltage vs. switching frequency for 11-level and 5-level CHMI using various SPWM methods.

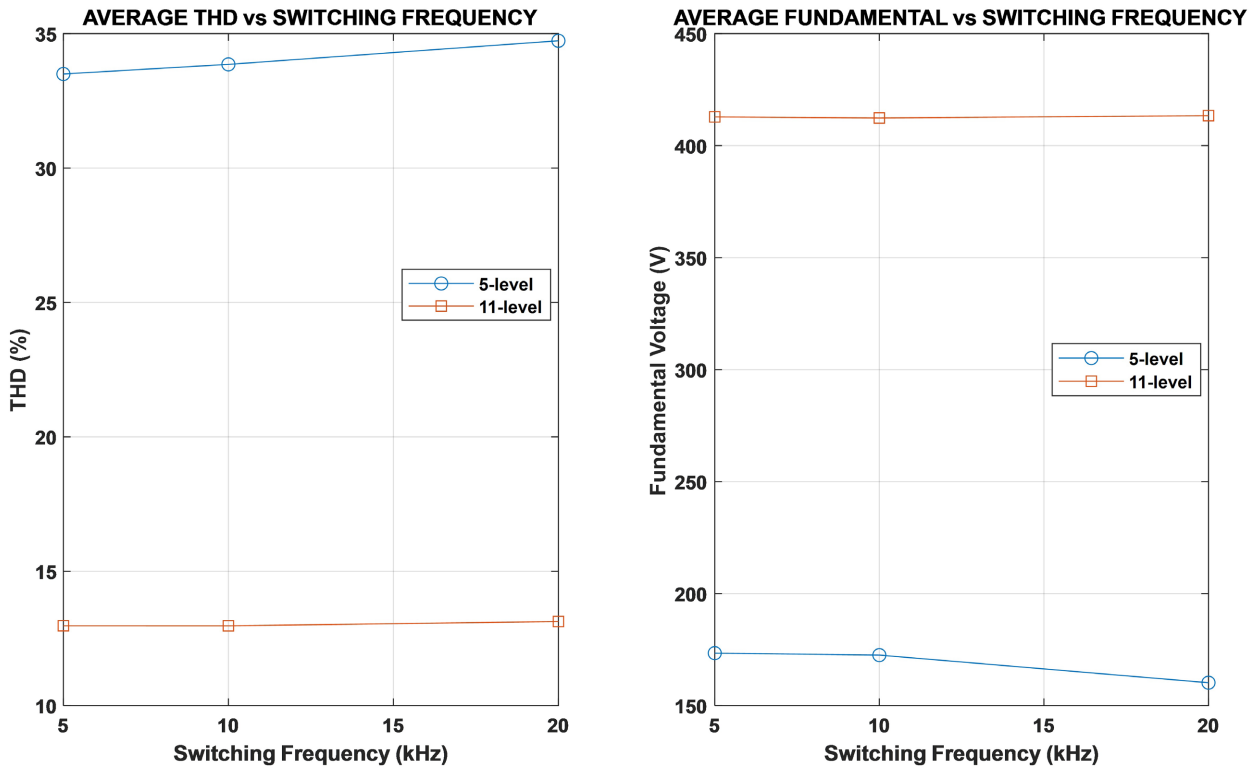


Figure 15. Average THD (left) and average fundamental voltage (right) versus switching frequency for 5-level and 11-level CHMI.

3.3.3. Switching-Loss and Efficiency Implications

To complement the THD and fundamental voltage analysis, the efficiency impact of switching losses at the tested frequencies was quantified. Switching losses per device, P_{SW} were estimated using a standard hard-switching model using formulas (4) and (5).

$$P_{SW} \approx \frac{1}{2} V_{DC} \times I\left(t_r + t_f\right) f_{SW} \tag{4}$$

$$\text{Total } P_{SW} = N \times P_{SW} \tag{5}$$

where $V_{DC} = 100$ V per H-bridge cell, t_r = rise time, t_f = fall time, assume $t_r + t_f = 100$ ns (as a representative MOSFET edge time), f_{SW} = switching frequency and N is the number of MOSFET. The inverter output power is given by:

$$P_{out} = \frac{V_{RMS}^2}{R_L} \tag{6}$$

Finally, the efficiency can be calculated using:

$$\eta(\%) = \frac{P_{out}}{P_{out} + \text{Total } P_{SW}} \times 100 \tag{7}$$

Table 4 shows that switching loss increases with frequency, which causes a small drop in efficiency. For the 5-level CHMI, efficiency falls from 99.84% at 5 kHz to 99.35% at 20 kHz, while the 11-level CHMI decreases from 99.83% to 99.32% in the same range. Although the loss is less than 1%, higher switching frequencies lead to more device heating and greater cooling demand. At the same time, increasing f_{SW} shifts EMI to higher frequencies, making filtering easier but at the cost of higher switching losses. This confirms the trade-off between efficiency, thermal stress, and EMI performance in practical design.

Table 4. Switching losses and corresponding inverter efficiencies for 5-level and 11-level CHMI at different switching frequencies.

f_{SW} (KHz)	5-Level				11-Level			
	P_{SW} (W)	Total P_{SW} (W)	P_{out} (kW)	η (%)	P_{SW} (W)	Total P_{SW} (W)	P_{out} (kW)	η (%)
5	0.305	2.44	1.49	99.84%	0.7295	14.59	8.51	99.83%
10	0.610	4.88	1.49	99.67%	1.4590	29.18	8.51	99.66%
15	0.915	7.32	1.49	99.51%	2.1885	43.77	8.51	99.49%
20	1.220	9.76	1.49	99.35%	2.9180	58.36	8.51	99.32%

In practical implementation, several challenges may affect the performance of multilevel inverters compared to ideal simulation results. Dead-time insertion, which is necessary to avoid shoot-through, can introduce waveform distortion and reduce the effective output voltage. Switching losses, as quantified in this work, further contribute to device heating and efficiency reduction, requiring careful thermal management. Moreover, device limitations such as finite switching speed, volt-

age/current ratings, and thermal constraints restrict the achievable operating range. Finally, the control implementation for multilevel inverters is more complex, as precise synchronization of multiple carriers and switching signals is required. These factors highlight that while simulation results are promising, additional considerations are necessary for reliable hardware realization.

3.4. Validation under RL/Motor-Equivalent Load

Figure 16, Figure 17 show the phase voltage under the motor-equivalent RL load for the four SPWM schemes. In all cases the phase voltage is nearly sinusoidal with small high-frequency ripple from carrier switching; moving from 5-level to 11-level visibly reduces the ripple/step granularity and yields a smoother envelope at the same modulation index. The load voltage is further smoothed by the series inductance and lags the voltage by the expected angle for power factor of 0.8, with no DC offset or low-frequency distortion observed.

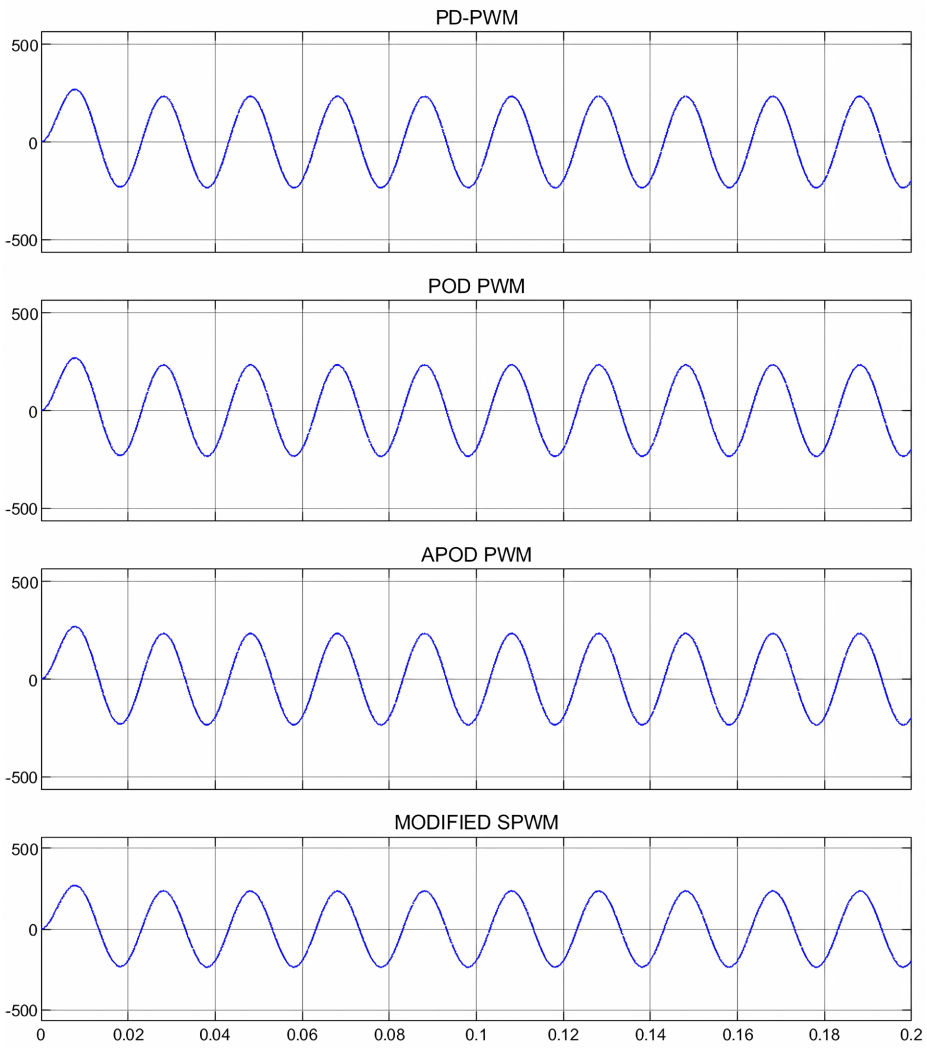


Figure 16. Simulation results showing the output voltage waveforms using PD-PWM, POD-PWM, APOD-PWM, and Modified SPWM for 5 level with RL load.

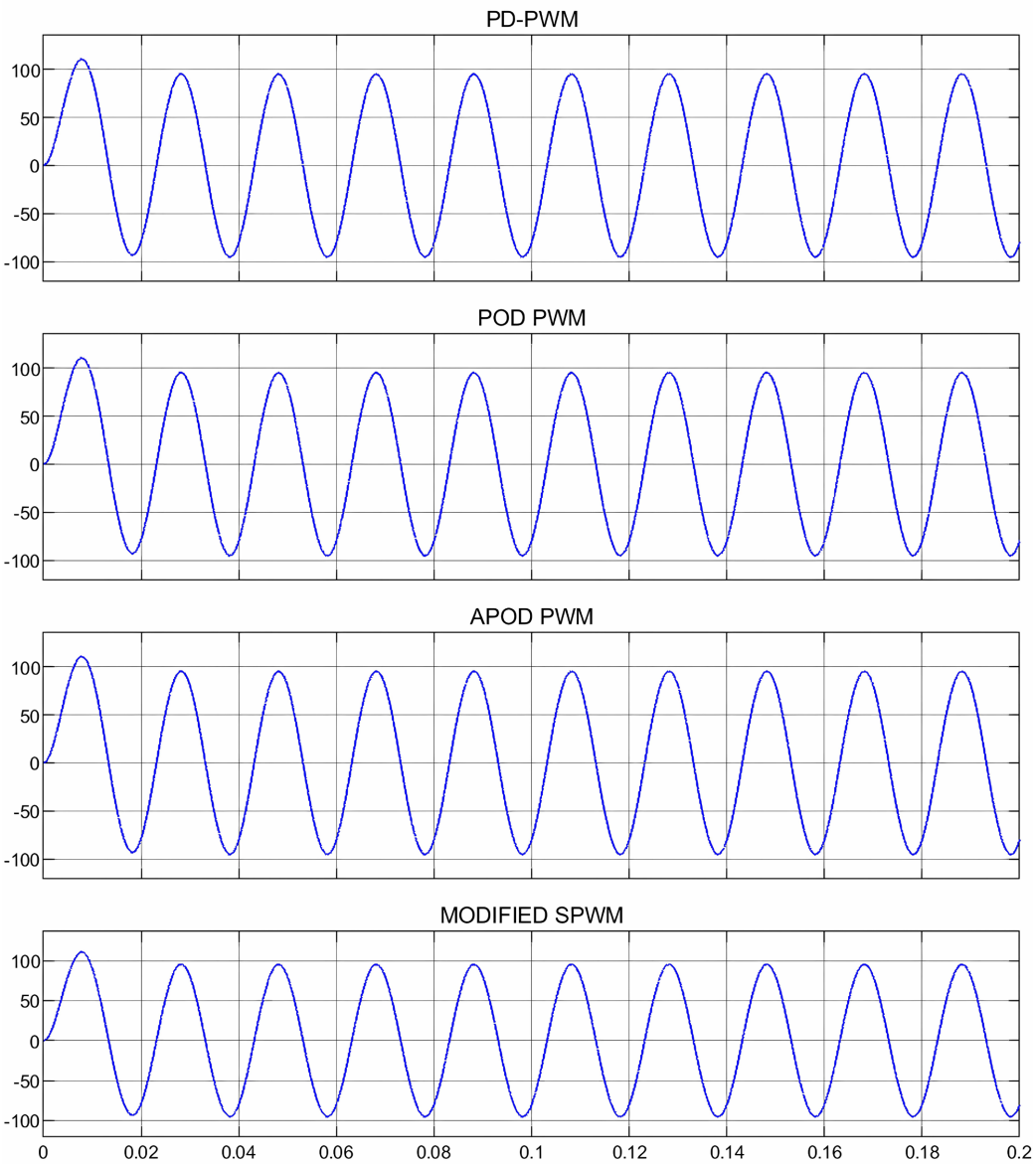


Figure 17. Simulation results showing the output voltage waveforms using PD-PWM, POD-PWM, APOD-PWM, and Modified SPWM for 11 level with RL load.

As summarized in **Table 5**, the 5-level CHMI yields voltage THD in the 0.27% - 0.34% range, with POD-PWM lowest (0.27%), PD and Modified essentially equal (0.29%), and APOD highest (0.34%). For the 11-level case, THD tightens to 0.20% - 0.22% with POD-PWM again best (0.20%), APOD at 0.21%, and PD/Modified at 0.22%. Moving from 5 to 11 levels reduces THD by roughly 24% - 38% across the four schemes, and the ranking observed with the resistive load is preserved, though differences narrow at higher levels. These results confirm that, under practical drive conditions, increasing the number of levels is an effective way to improve harmonic quality, while the RL load mainly attenuates current harmonics (beneficial for conducted EMI) without altering the fundamental conclusions about the modulation strategies.

Table 5. Comparison of total harmonic distortion (THD) for different SPWM techniques in 5-level and 11-level CHMI inverters under RL.

Switching techniques	Total harmonic distortion (THD)	
	5-level	11-level
PD-PWM	0.29%	0.22%
POD-PWM	0.27%	0.20%
APOD-PWM	0.34%	0.21%
MODIFIED SPWM	0.29%	0.22%

4. Conclusion

This paper compared four SPWM techniques in 5-level and 11-level CHMI configurations, focusing on the effects of modulation index and switching frequency. Results showed that increasing the number of voltage levels greatly improves waveform quality and voltage stability, while modulation strategy has only a minor effect. POD and APOD provided slightly better harmonic performance, whereas Modified SPWM closely matched the performance of PD-PWM in all tested cases. This indicates that Modified SPWM can be adopted as a simpler alternative to PD-PWM without compromising performance. Switching frequency had little influence on the 11-level CHMI but affected the 5-level configuration more noticeably. Overall, voltage level count was the dominant factor in achieving low THD and stable output voltage. Future work may explore hybrid SPWM techniques or adaptive modulation strategies to further optimize inverter performance. Hardware testing is recommended to validate simulation results in real world conditions. In addition, integrating renewable energy sources as DC inputs could provide deeper insight into system behaviour under variable input conditions. While the simulation results demonstrate the effectiveness of the proposed multilevel inverter schemes, several practical issues must be considered in hardware implementation. Dead-time effects, device switching limits, and the added control complexity of multilevel structures may reduce performance compared to the ideal case, and careful design is required to balance efficiency, reliability, and EMI compliance.

Acknowledgements

The authors would like to express their sincere gratitude to Universiti Teknikal Malaysia Melaka (UTeM), the Faculty of Electrical Technology and Engineering, the Centre of Robotic and Industrial Automation (CERIA), and the Centre of Research and Innovation Management (CRIM) for their support and contributions.

Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

References

[1] Kannan, R., Angamuthu, R. and Ahmed, K.Y. (2017) Photo Energy Conversion Using

Synchronous Sequential Circuit Based Diode Clamp Multilevel Inverter. 2016 6*th International Conference on Intelligent and Advanced Systems* (*ICIAS*), Kuala Lumpur, 15-17 August 2016, 1-6. https://doi.org/10.1109/icias.2016.7824068

[2] Sorrell, S. (2010) Energy, Economic Growth and Environmental Sustainability: Five Propositions. *Sustainability*, **2**, 1784-1809. https://doi.org/10.3390/su2061784

[3] Hren, A., Truntič, M. and Mihalič, F. (2023) A Survey on the State-of-the-Art and Future Trends of Multilevel Inverters in BEVs. *Electronics*, **12**, Article 2993. https://doi.org/10.3390/electronics12132993

[4] Tolbert, L.M., Peng, F.Z. and Habetler, T.G. (1998) Multilevel Inverters for Electric Vehicle Applications. *Power Electronics in Transportation* (*Cat. No.*98TH8349), Dearborn, 22-23 October 1998, 79-84. https://doi.org/10.1109/pet.1998.731062

[5] Taha, T.A., Shalaby, M., Wahab, N.I.A., Zaynal, H.I., Hassan, M.K., Al-Sowayan, S., *et al.* (2025) Recent Advancements in Multilevel Inverters: Topologies, Modulation Techniques, and Emerging Applications. *Symmetry*, **17**, Article 1010. https://doi.org/10.3390/sym17071010

[6] Ahamad, N., Hasan, M.M. and Uddin, S. (2021) Review of Multilevel Inverters for PV Energy System Applications. *Energies*, **14**, Article 1585. https://doi.org/10.3390/en14061585

[7] Ravi, R. and Karuppanan, P. (2023) Cascaded H-Bridge Multilevel Inverter for Electric Vehicles: Configuration and Performance Investigation. *Journal of Power Electronics and Electric Drives*, **11**, 134-145.

[8] Kumar, D. and Singh, B. (2023) Comparative Performance of Modular with Cascaded H-Bridge Three-Level Inverters for Industrial Motor Control Applications. *International Journal of Electrical Power & Energy Systems*, **150**, Article 109020.

[9] Alam, M.R., Das, P.C. and Bhuiyan, M.M.H. (2024) Review of Multilevel Inverter for High-Power Applications. *International Journal of Power Electronics and Drive Systems*, **15**, 104-112.

[10] Arranz-Gimon, A., Zorita-Lamadrid, A., Morinigo-Sotelo, D. and Duque-Perez, O. (2021) A Review of Total Harmonic Distortion Factors for the Measurement of Harmonic and Interharmonic Pollution in Modern Power Systems. *Energies*, **14**, Article 6467. https://doi.org/10.3390/en14206467

[11] Zhang, S., Li, H., Liu, Y., Liu, X., Lv, Q., Du, X., *et al.* (2024) An Improved SPWM Strategy for Effectively Reducing Total Harmonic Distortion. *Electronics*, **13**, Article 3326. https://doi.org/10.3390/electronics13163326

[12] Vadhiraj, S., Swamy, K.N. and Divakar, B.P. (2013) Generic SPWM Technique for Multilevel Inverter. 2013 *IEEE PES Asia-Pacific Power and Energy Engineering Conference* (*APPEEC*), Hong Kong SAR, 8-11 December 2013, 1-5. https://doi.org/10.1109/appeec.2013.6837117

[13] İnci, M. (2019) Performance Evaluation of Multi-Carrier PWM Techniques: PD, POD and APOD. *International Journal of Applied Mathematics Electronics and Computers*, **7**, 38-43. https://doi.org/10.18100/ijamec.569660

[14] Balasubramanian, M. and Geetha, B.T. (2022) Reduction of Harmonics in Multilevel Inverter Using Phase Disposition PWM Compared with Conventional PWM Based on Efficiency. 2022 5*th International Conference on Contemporary Computing and Informatics* (*IC3I*), Uttar Pradesh, 14-16 December 2022, 855-861. https://doi.org/10.1109/ic3i56241.2022.10072518

[15] Tolbert, L.M., Fang Zheng Peng, and Habetler, T.G. (1999) Multilevel Converters for Large Electric Drives. *IEEE Transactions on Industry Applications*, **35**, 36-44. https://doi.org/10.1109/28.740843