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Design of Ku Band 64 Channel Tile Type Transceiver Component

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Abstract

Based on the high integration and low profile application requirements of phased array systems, a Ku band 64-element tile type transceiver component was developed. Through the high-density integrated 3D design concept, the 64-element transceiver channels are arranged in a rectangular grid array, and the functional circuits are horizontally arranged and vertically integrated, achieving the low profile characteristics of the components. Detailed introductions were provided on the key circuit design, structural design, and thermal design of the components. Through physical testing, the single channel receiving gain of the transceiver component is ≥6 dB, and the noise figure is ≤3.5 dB; Single channel transmission gain ≥ 4 dB, transmission saturation output power ≥ 22 dBm; Each channel can independently achieve 6-bit phase shift and 4-bit attenuation functions. The phase consistency of 64 channels is better than 7˚, and the amplitude consistency is better than 0.6 dB. The component size is 100 mm × 84 mm × 13.1 mm, with a mass of less than 150 g. This transceiver component has a standardized architecture and can flexibly achieve large-scale array expansion.

Keywords

Ku Band, Tile Tyle, Sending and Receiving Components, High Density Integration

1. Introduction

Currently, AESA (Active Electronically Scanned Array) is widely used in multipurpose radar, electronic warfare, satellite communication and other fields. The highly integrated T/R (Transmit/Receive) modules of the phased array, as the "eyes" of the antenna, are the core components of the phased array system. Their volume, weight, power consumption and cost directly determine the performance of the entire phased array antenna. According to the assembly method, the AESA T/R modules can be divided into "brick" structure and "tile" structure.

The "brick" structure T/R modules are vertically integrated and horizontally assembled, with the characteristics of low integration and large longitudinal dimensions, making it difficult to miniaturize the sub-arrays. In contrast, the "tile" modules are horizontally integrated and vertically assembled based on Low Temperature Co-fired Ceramic (LTCC) and other multi-layer substrates. The "tile" structure T/R modules adopt a multi-layer structure, with vertical interconnections between layers for signal transmission, featuring low profile and high integration. By assembling several sub-arrays, the chip layout becomes more regular and can be flexibly expanded into a large-scale array.

With the development of microelectronic systems towards miniaturization and high integration, the application of phased array systems is becoming more and more widespread. Therefore, the development of miniaturized and highly integrated tile-type T/R modules is particularly urgent [1]-[7].

This paper proposes a design method for a 64-element Ku-band tile-type T/R module, and verifies the feasibility of the entire design through performance measurements of the T/R module.

2. Circuit Design

2.1. Solution Introduction

This tile-type transceiver module operates in a half-duplex mode. In the receive mode, the 64 RF signals from the antenna unit are individually subjected to low-noise amplification, programmable phase shifting, and programmable attenuation. The amplitude and phase of each signal can be independently adjusted, with a phase shift step of 5.625˚ and an attenuation step of 1 dB, up to a maximum of 15 dB attenuation. The signals are then combined through an RF power combining network and output. In the transmit mode, the RF signal from the power distribution network is first divided into 32 equal-power paths. Each path then goes through phase shifting and amplitude adjustment, and is finally amplified by power amplifiers and transmitted to the antenna. The phase shifter and attenuator are shared between the receive and transmit paths, with a phase shift step of 5.625˚ and an attenuation step of 1 dB, up to a maximum of 15 dB attenuation.

The module integrates a low-frequency control circuit, which can independently control the 64-path phase shifting and attenuation circuits through external commands. The block diagram of the transceiver module is shown in **Figure 1**.

2.2. Three-Dimensional Vertical Interconnection Technology

The transceiver module has a high-density integration of 65 RF ports, with 1 RF common port and 64 RF branch ports. The 64 branch ports are directly connected to the antenna array, so it is a critical design requirement to ensure low return loss for all 64 RF ports.

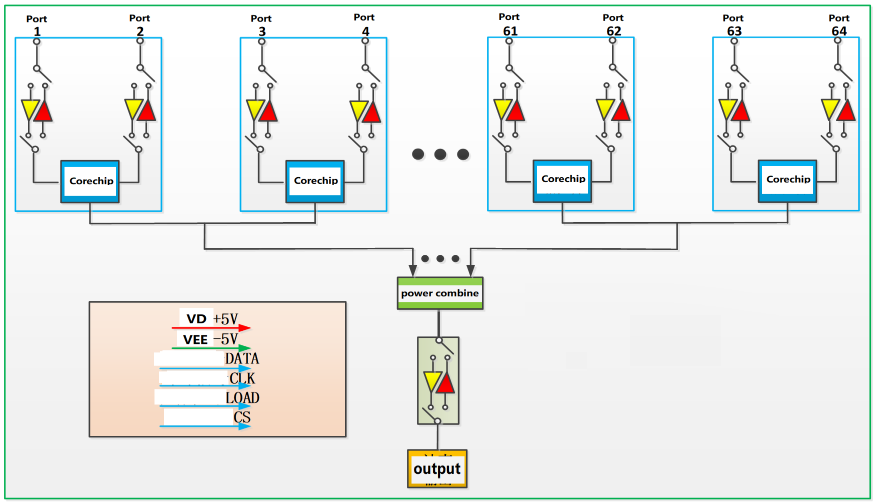

Figure 1. Block diagram of transceiver component solution.

The ports use RF micro-miniature push-in (SMP) connectors that are soldered onto the housing, with the SMP input ports vertically interconnected to the PCB. To improve the input/output port impedance matching and reduce standing waves, matching sections have been added. Through modeling and simulation optimization of the matching section length and width, as shown in **Figure 2** and **Figure 3**, the simulation results show that within the wide frequency band of 13 GHz to 18 GHz, the insertion loss is low, and the return loss of each input port is better than −20 dB, achieving good performance.

To quickly obtain the optimal coaxial structure parameters, the characteristic impedance (Z0) of the coaxial structure is used to determine the initial simulation parameters:

$$Z0 = 60 / \sqrt{\varepsilon r} * \ln\left(\mathrm{Do}/\mathrm{Di}\right) \tag{1}$$

where: εr is the relative dielectric constant of the medium; Do is the outer conductor diameter of the coaxial structure; Di is the inner conductor diameter of the coaxial structure.

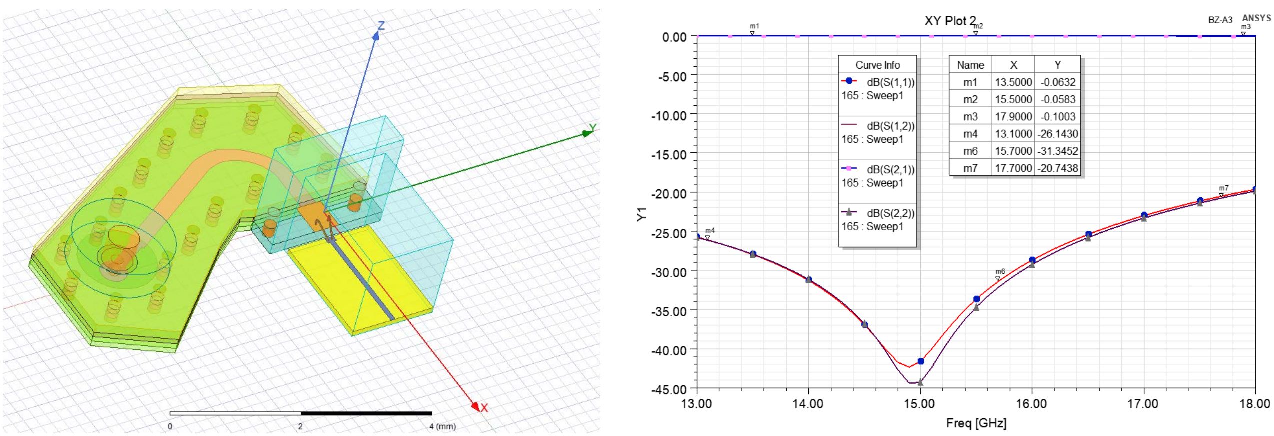

Figure 2. RF branch vertical transition three-dimensional model and simulation results.

Based on the PCB process rules, the via diameter has been fixed at 200 μm, so the inner conductor diameter of the coaxial structure is already determined. To ensure the transmission structure is well-matched to the chip, the characteristic impedance should be as close to 50 Ω as possible. Using Equation (1), the value of Do can be determined.

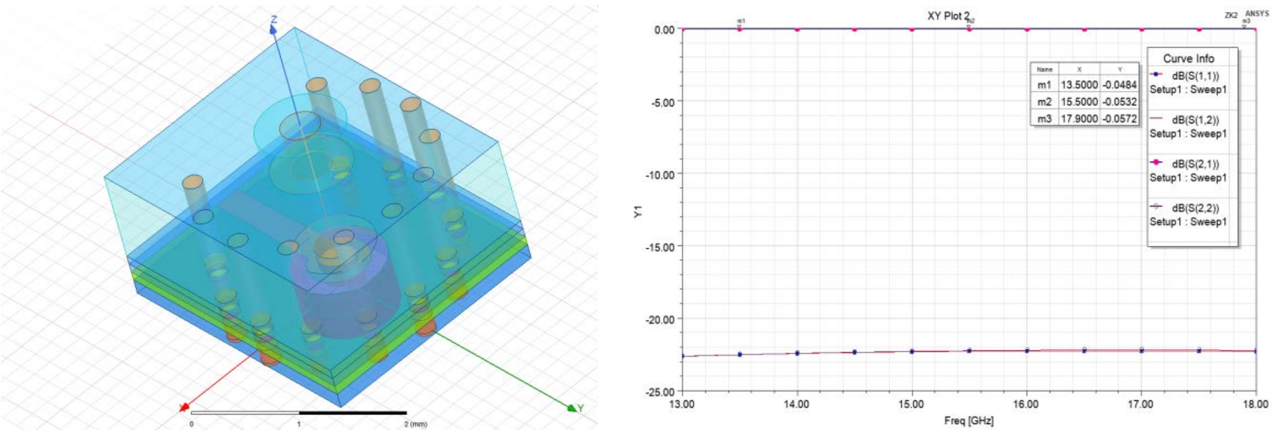

Figure 3. RF main port vertical transition three-dimensional model and simulation results.

2.3. Feed Network Design

To ensure the channel consistency of the 64-element tile-type transceiver module, a symmetric layout design was adopted. The power divider isolation can affect the phase accuracy and phase-induced amplitude modulation performance indicators [8]. To improve the inter-channel isolation, isolation resistors were added within the power divider network.

A simulation model of the RF feeding network was established, as shown in **Figure 4**. The simulation results show that the 4-way power divider network has an insertion loss ≤ 8 dB, the isolation between adjacent ports is better than −20 dB, and the isolation between non-adjacent ports is better than −25 dB, as shown in **Figure 5** and **Figure 6**. The performance meets the design requirements of the module.

2.4. Amplitude and Phase Command Control Circuit Design

Each channel of the transceiver module can independently receive and execute external control commands to adjust the phase and amplitude of the RF signals. The schematic diagram of the command control circuit is shown in **Figure 4**. CS1 to CS6 are the channel selection signals for the transceiver module. The internal decoding circuit decodes the input CS1 to CS6 signals and selects the corresponding phase shifter/attenuator of the channel. At this time, the phase shifter/attenuator can be programmed.

When CS is low, the clock CLK and data DATA can enter the chip internally; when CS is high, the clock CLK and data DATA are blocked outside the chip [9]. The command control circuit, through the decoder and inverter, realizes the chip selection function of the phase shifter/attenuator chip. By combining the configuration

DATA bits, the independent amplitude and phase control function of the 64 channels is ultimately achieved.

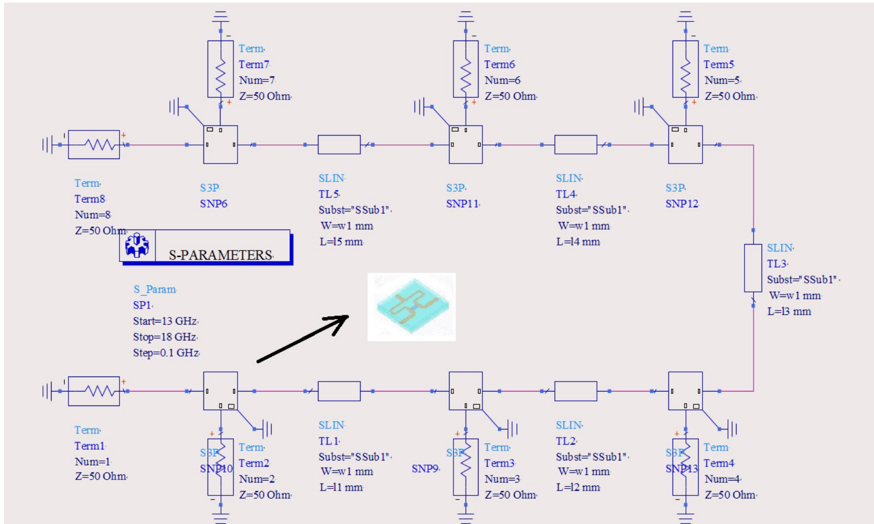

Figure 4. Feeder network link simulation.

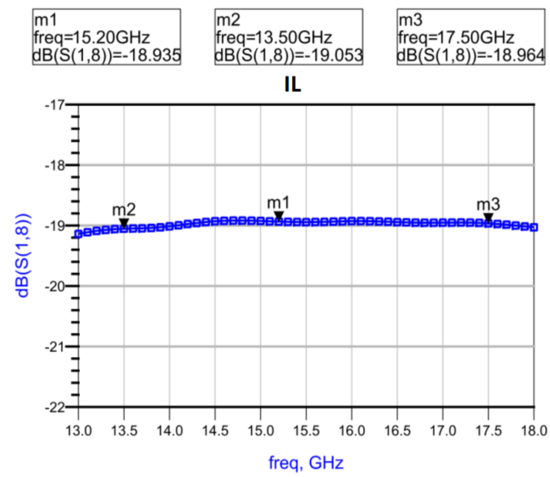

Figure 5. Feed network insertion loss simulation curve.

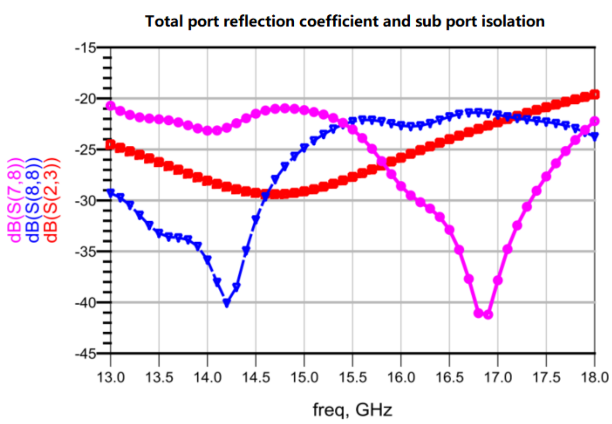

Figure 6. Feed network isolation and port reflection simulation curve.

3. Structural Design

The structural design of the transceiver module adopts a sub-unit design, and the layout can be arrayed and expanded. The 3D model is shown in **Figure 7**. For large-scale phased array transceiver systems, the entire array surface can be divided into several scalable sub-arrays, and the core component of each scalable sub-array is the 64-element tile-type transceiver module. Through the flexible combination of sub-arrays, it is easy to realize large-scale array implementation.

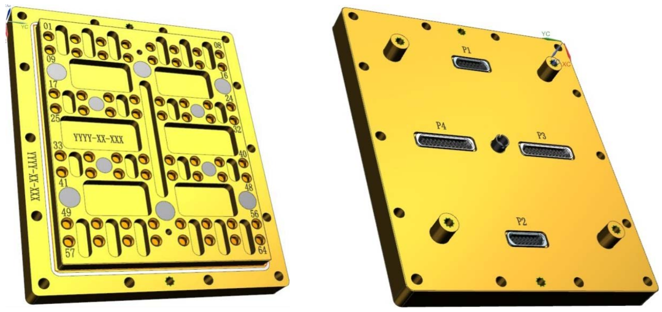

Figure 7. RF interface form of connecting TR component and antenna array.

In this phased array antenna solution, a separate power distribution module does not exist. This functional circuit has been integrated into the TR component through a multi-layer printed board process, achieving a power distribution of 1:64. The TR component consists of printed boards, structural parts, 64 SMP connectors connected to the antenna, 4 low-frequency sockets connected to the wave control, and a high-frequency socket connected to the AIU, as shown in **Figure 8**. The 8*8 scale whole-board TR multi-layer printed circuit board is installed in the metal cavity shown in the picture above by welding. The SMP connector is assembled to the cover plate by welding. The cover plate and the metal cavity are processed by laser Sealing and welding to achieve airtightness. The total outlet of the Ku frequency band of the TR circuit is located at the bottom of the metal cavity in the figure. It also appears in the form of a coaxial metal pad on the printed board, as shown in the figure below.

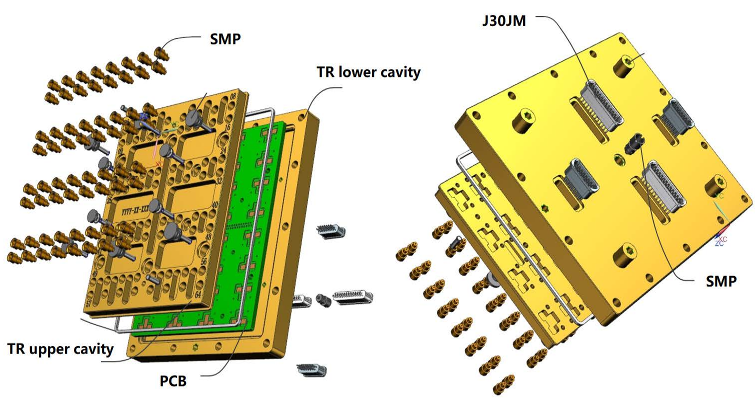

Figure 8. Exploded view of TR module.

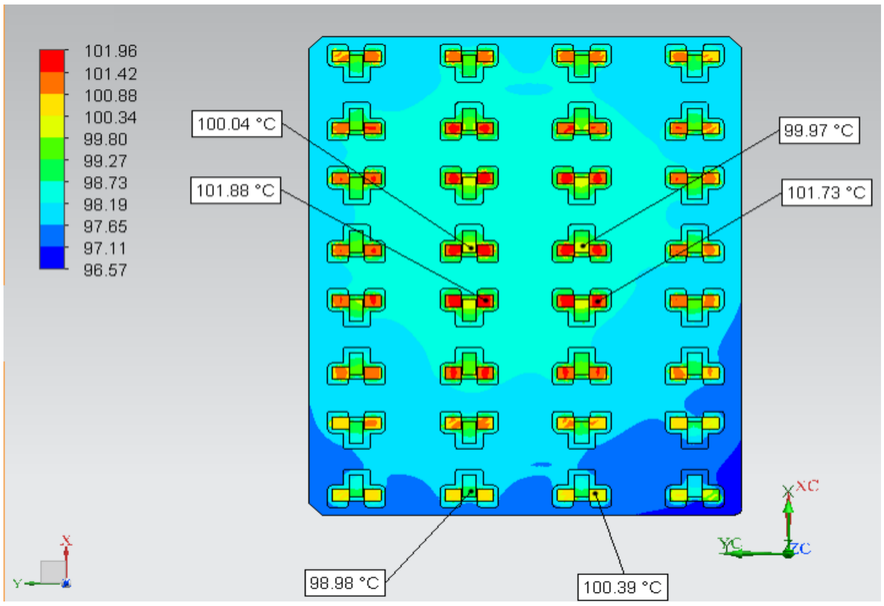

Figure 9. TR component device temperature distribution.

The transceiver component adopts high-density integration technology and integrates several active circuits in a limited space. Thermal design is one of the important focus technologies of the component. For multi-channel transceiver components, distribute active devices around dense grounding holes inside the printed board to shorten the heat dissipation path, reduce the thermal resistance between the device and the metal shell, and avoid the concentration of heat sources. According to the actual working conditions of the component, a thermal simulation analysis was carried out on the component under the condition of boundary temperature +85℃. The results are shown in **Figure 9**. Through the thermal analysis cloud diagram, the maximum temperature rise of the active device is about 20℃, and each channel The heat is evenly distributed and the components can work for a long time.

4. Physical Objects and Test Results

Analysis Based on the aforementioned scheme design and simulation analysis work, a KU-band 64-element tile transceiver component was successfully developed. The actual product is shown in **Figure 10**. The overall dimensions of the component are 100 mm × 84 mm × 13.1 mm, and the mass is less than 150 g. Compared with traditional multi-channel transceiver components, the size and weight are significantly reduced.

The test results are shown in **Figure 11** to **Figure 12**. The components work in the Ku frequency band, and the frequency band can be expanded according to needs. The single-channel receiving gain is ≥6 dB, the noise coefficient is better than 3.5 dB, the 64-channel receiving phase consistency is RMS ≤ 6˚, the 64-channel receiving attenuation consistency is RMS ≤ 0.5 dB, and all 64 channels can realize amplitude and phase control independently.

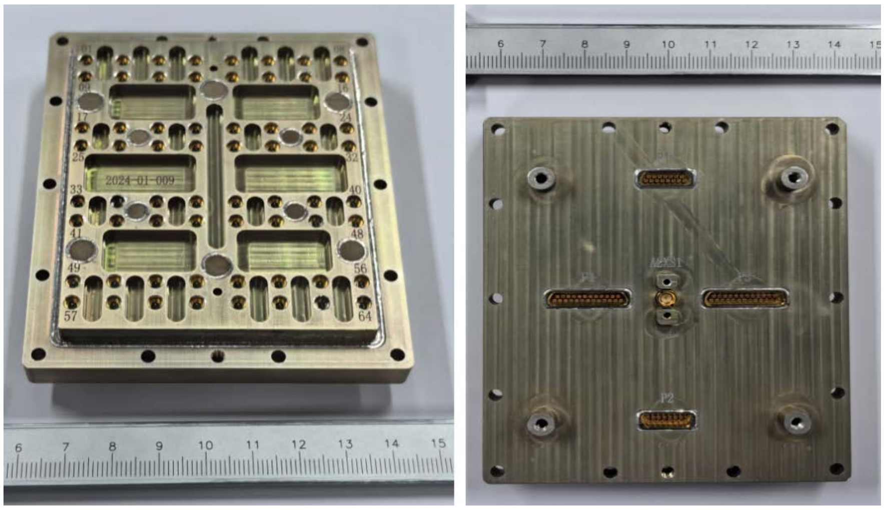

Figure 10. Physical diagram of components.

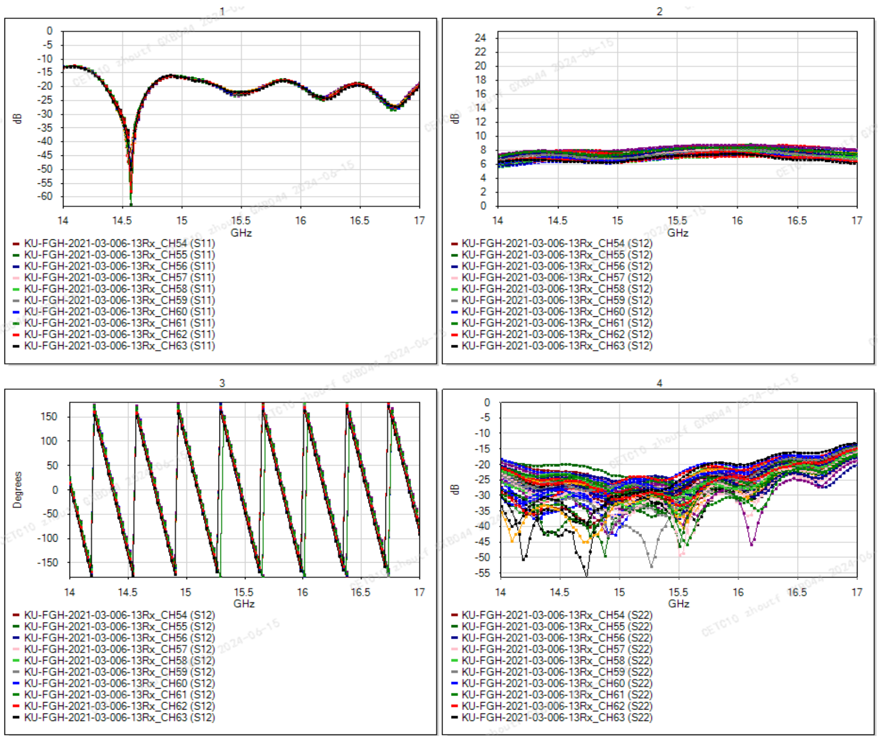

Figure 11. Test results of transmission channel.

The gain of a single transmit channel is ≥4 dB, the transmit output power is ≥22 dBm, the 64-channel transmit phase consistency is better than 7˚, the 64-channel transmit attenuation consistency is better than 0.6 dB, and each channel can independently realize amplitude and phase control.

The gain of a single receiving channel is ≥4 dB, the noise coefficient of a single channel is ≤3.5 dB, the phase consistency of 64 channels is better than 4˚, the attenuation consistency of 64 channels is better than 0.5 dB, and each channel can realize amplitude and phase control independently.

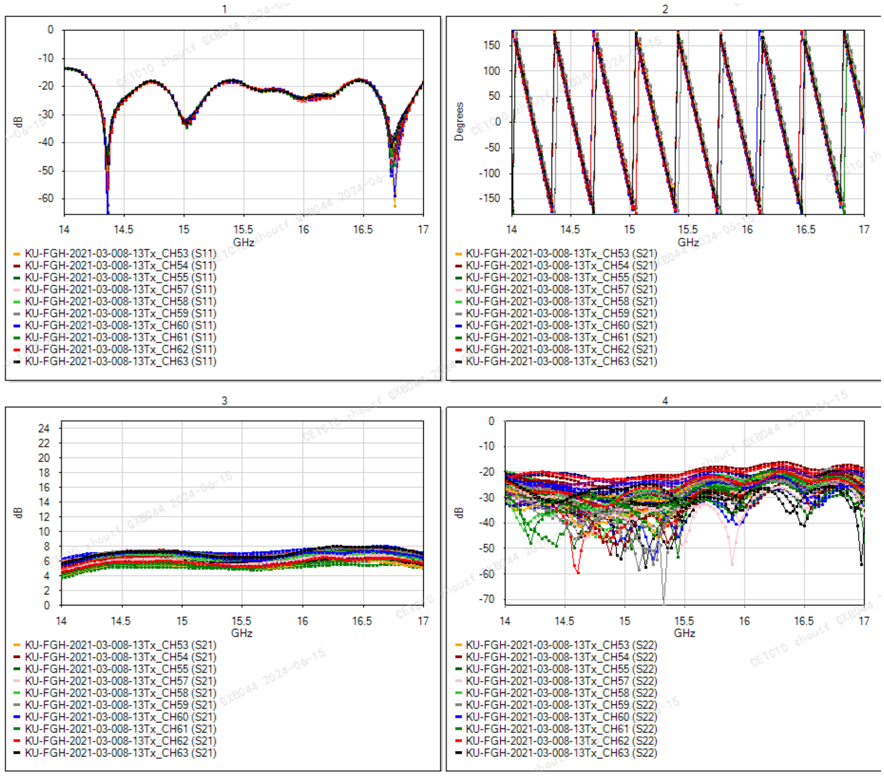

Figure 12. Test results of receiving channel.

5. Conclusion

This article proposes a design scheme for a multi-channel tile-type transceiver component and develops a Ku-band 64-element transceiver component. Through physical testing and verification, its performance indicators fully meet engineering needs. The developed transceiver components achieve high integration, low profile, and lightweight characteristics under the premise of meeting performance requirements and focus on solving the tile-type transceiver component architecture topology design, high-performance three-dimensional vertical interconnection design, and high-density integrated component thermal design. Technical issues. After subsequent full verification, the transceiver component can be directly applied to low-profile tile phased array systems.

Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

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