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Application of FPGA in Process Tomography Systems

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Abstract

This paper will provide some insights on the application of Field Programmable Gate Array (FPGA) in process tomography. The focus of this paper will be to investigate the performance of the technology with respect to various tomography systems and comparison to other similar technologies including the Application Specific Integrated Circuit (ASIC), Graphics Processing Unit (GPU) and the microcontroller. Fundamentally, the FPGA is primarily used in the Data Acquisition System (DAQ) due to its better performance and better trade-off as compared to competitor technologies. However, the drawback of using FPGA is that it is relatively more expensive.

Keywords

Data Acquisition System (DAQ), Field Programmable Gate Array (FPGA), Application Specific Integrated Circuit (ASIC), Graphics Processing Unit (GPU), Microcontroller

1. Introduction

Industrial process tomography (IPT) is generally a cross sectional imaging of parameters of industrial processes and usually a function of time [1]. In IPT, the three classifications of sensor systems are transmission mode, reflection mode and emission mode techniques [2]. The four typical tomography sections are sensor array, data acquisition system, image reconstruction and display system [3] [4] as shown in **Figure 1**.

However, one should always remember that in real industrial and research application, it is possible to implement combinations of stated sensors or known as multi-modality. For example, Deng [5] has used 1) Electrical Resistance Tomography (ERT) with electromagnetic (EM) flowmeter 2) Electrical Capacitance Tomography (ECT) with ERT and 3) ECT with electrostatic sensor for two

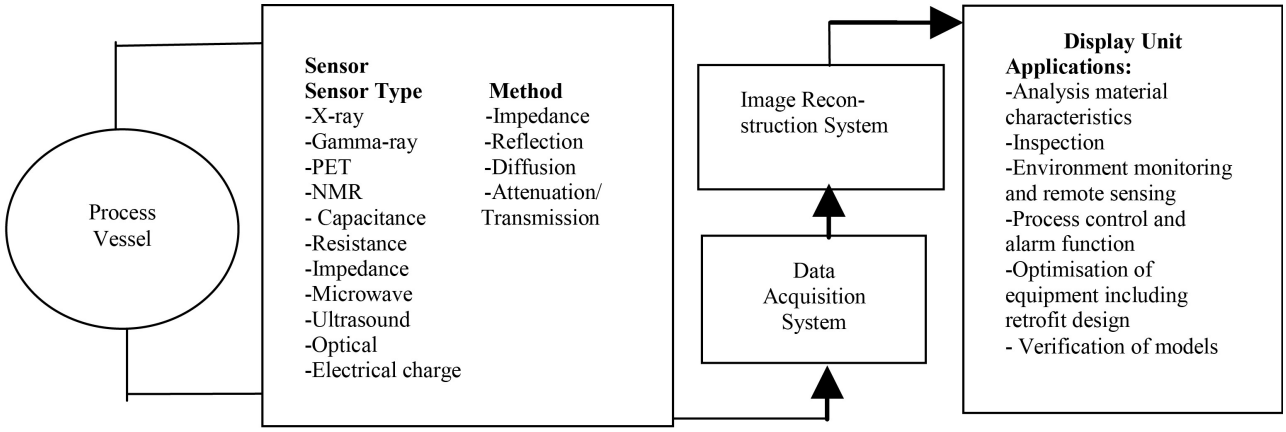

Figure 1. Block diagram of typical tomography system [3] [4].

phase flow measurement. On the other hand, an example of such industrial application is a dual-modality ECT and ERT by Industrial Tomography System [6] that is able to visualize water and sand flow as well as oil and gas flow.

In general, processors are included in all hardware design except the smallest design due to its size and cost [7]. There are various brands of Field Programmable Gate Array (FPGA) in the market. Two of the most common manufacturer of FPGA or Complex Programmable Logic Devices (CPLD) one might encountered are probably Altera and Xilinx. According to [8], the three parameters to evaluate Field Programmable Gate Array (FPGA) are speed, area, and power (energy). Meanwhile, the languages of choice for FPGA are Verilog and VHDL (Verilog Hardware Description Language). The advantages of FPGA include the ability to construct the required hardware [9]. This is better than the usual application-specific standard product (ASSP) which is applicable to other technologies as well or using the application-specific integrated circuit (ASIC) which is more cost, time consuming, and of higher risk.

In this paper, we discussed the performance of the Field Programmable Gate Array (FPGA). The sections are divided into: 1. Introduction, 2. Electrical Resistance Tomography, 3. Electrical Capacitance Tomography, 4. Electrical Impedance Tomography, 5. Ultrasonic, 6. Other Types of Tomography, 7. Comparison of FPGA with Competitor Technologies, 8. Conclusion.

2. Electrical Resistance Tomography (ERT)

Electrical Resistance Tomography (ERT) is based on concept where different medium will not have a similar conductivity [10].

Zhang [11] in his ERT system were implementing 16 rectangle stainless steel electrodes of 10 mm width and 20 mm height for each plane. **Figure 2** shows the ERT system platform. In his work, Field-Programmable Gate Array (FPGA) and measurement (MEAS) was used in the direct digital synthesizer (DDS) system, multiplexing (MUX) and power supply (PWS). Besides that, FPGA was also used to provide control signals that enhance the data acquisition system (DAQ) and communication functions. Excitation signal which are generated by FPGA are

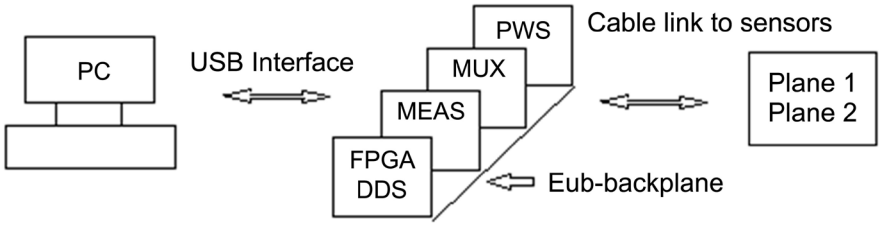

Figure 2. The ERT system platform [11].

sinusoidal current from frequency range 1Hz to 1 MHz which are sent to MEAS card to excite a pair of adjacent electrodes and the projected data is measured, *i.e.* the resulting potential difference between another pair of adjacent electrodes. The conclusions that were achieved are the reconstructed images can reflect the change of the cross-section distribution of the gas/liquid two-phase flow; the estimation of the gas holdup can be obtained and used in industry control. The presented cross correlation velocity measurement method base on gas holdup was feasible.

Another author, Zhang [12] applied CompactPCI bus and the FPGA on his novel data acquisition system (DAQ) for his Electrical Resistance Tomography system. **Figure 3** shows the architecture of the DAS based on CompactPCI bus and FPGA. The roles of FPGA which are included in the DAQ are digital filters, digital demodulations, injecting strategy change and data transportation based CompactPCI bus. By applying digital techniques such as used by FPFA instead of analogue counter parts, challenges such as noise, component mismatching, input offset and their speed is limitation could resolved. In most ERT system, FPGA chips are used to carry out the tasks of control while the DSP chips is using for data processing. Nevertheless, in comparison of FPGA with respect to traditional instruction-driven DSP processors, via parallel implementation generates much more computation power which leads to high bandwidth and good precision in ERT systems. In addition, applying FPGA in ERT helps in upgrading and debugging. By adding extra CompactPCI cards and simple configuration modifications in FPGA chips and software in host computer, the author could make the single plane Electrical Resistance Tomography system extended and upgraded easily to multi-plane. On the other hand, the FPGA plays the role of flexible control of the injecting method and strategy. The digital signal processing technique in FPGA is used to measure and process the desired signals. In terms of performance tested in laboratory, the data acquisition system (DAQ) at the 100 kHz sine wave injecting signal could achieve at least 1500 frame/s and will increase with frequency with achievable Signal-to-Noise ratio 73 dB.

3. Electrical Capacitance Tomography (ECT)

In the same manner, Electrical Capacitance Tomography (ECT) measures the difference in capacitance typically in the range of 0.01pF to 1pF [13].

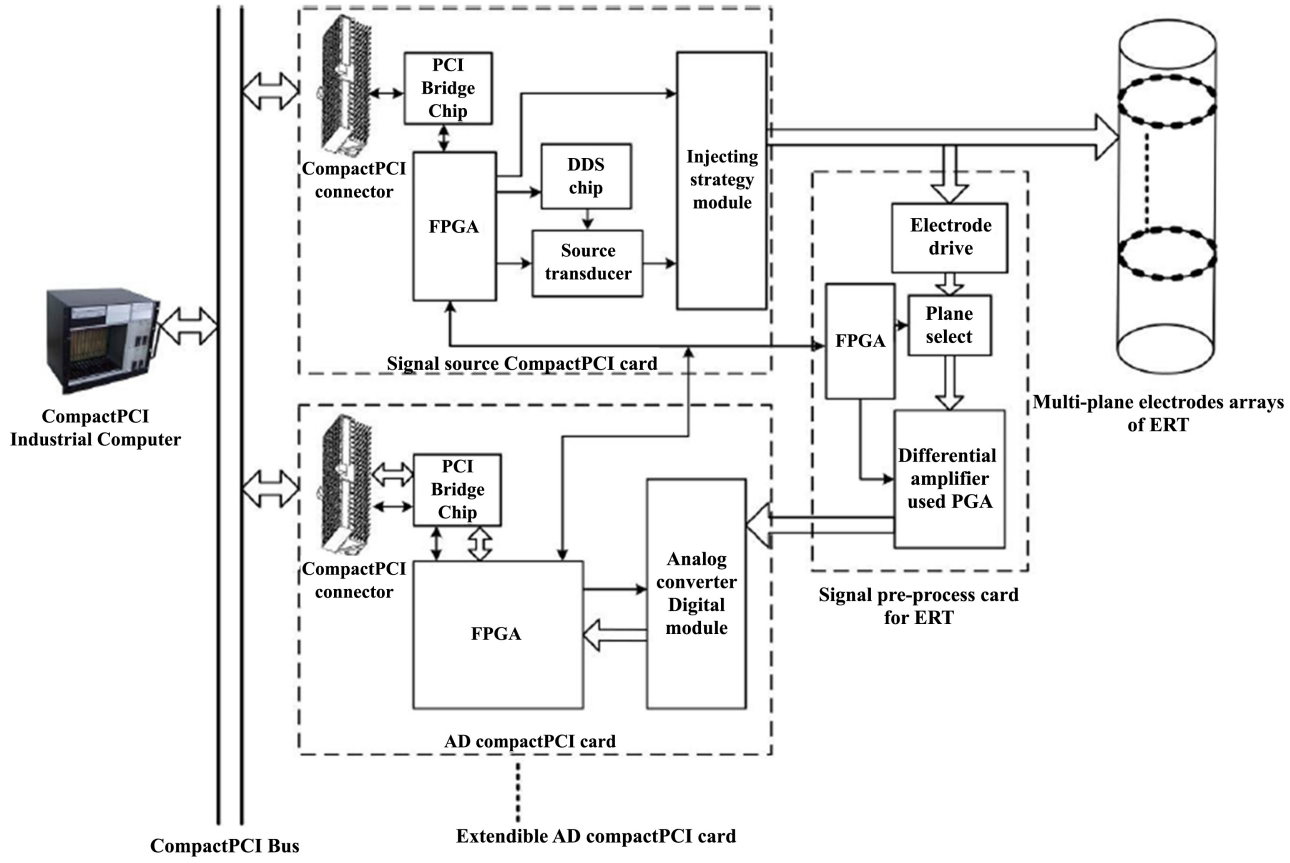

Figure 3. Architecture of the DAS based on CompactPCI Bus and FPGA [12].

The electrical capacitance volume tomography (ECVT) is a volumetric in real time three dimensional is an improvement from the two-dimensional slicing ECT [14]. The FPGA in the ECVT by [15] is used as control processing core, excitation signal generation, and signal demodulation. The advantages of FPGA modular design includes minimal hardware overhead, is flexible, fast, and stable in order to facilitate further development of measurement system. They managed to improve systematic SNR and simplify peripheral circuits by integrating Direct Digital Synthesizer (DDS) and Phase Shift Demodulation (PSD) module into one FPGA hardware. FPGA is suitable for large amount of data on frontend in real-time processing with high-speed and relatively simple pre-processing architecture [16]. Phase detection algorithm or the Phase Shift Demodulation implemented on Xilinx FPGA IP Core. The DDS IP Core implemented in FPGA which produces synchronous sine and cosine signal are directly used in digital domain for demodulation. The digital method implemented could avoid the frequency mismatch and phase variation between signals problems. The conclusions that could be made include the FPGA platform could be successfully used as a core processing for calculating phase and amplitude of the detected signal.

Wang [17] had implemented a new image reconstruction algorithm on Electrical Capacitance Tomography (ECT) with Least Squares Support Vector Machines (LS-SVM) and Simulated Annealing Particle Swarm Optimization (APSO),

named SAP. Figure 4 constitutes of Electrical Capacitance Tomography system. Particle Swarm Optimization (PSO) which adopts cooling process functions to replace the inertia weight function and constructs the time variant inertia weight function featured in annealing mechanism. The APSO was improved by implementing for exercise results from LS-SVM for errors caused by the fixed sensitivity matrix for ECT reverse questions to obtain the optimized resolution of reconstructed images. A conclusion was drawn that the high precision reconstruction images could be obtained via the SAP algorithm. The chaotic search process was integrated into SAP to further improve the said algorithm. Although the algorithm time complexity could be significantly fastened by embedding chaotic search, the same could not be said about imaging precision which improves slightly. Overall, their SAP work is worked better than the classic Landweber algorithm and Newton-Raphson algorithm on image reconstruction.

Firadus [18] in his real-time Electrical Capacitance Tomography (ECT) with a novel embedded hardware architecture of 1) Capacitance Data Acquisition and switching board and 2) Field Programmable Gate Array (FPGA) Board modules using Xilinx Virtex-II XCV1500. Figure 5 shows the Hardware System Overview: Overall Block Diagram while Figure 6 shows Image Reconstruction Implementation Block Diagram on FPGA. The performance of the ECT done via experiment would be sufficient for most real-time industrial purposes of a throughput

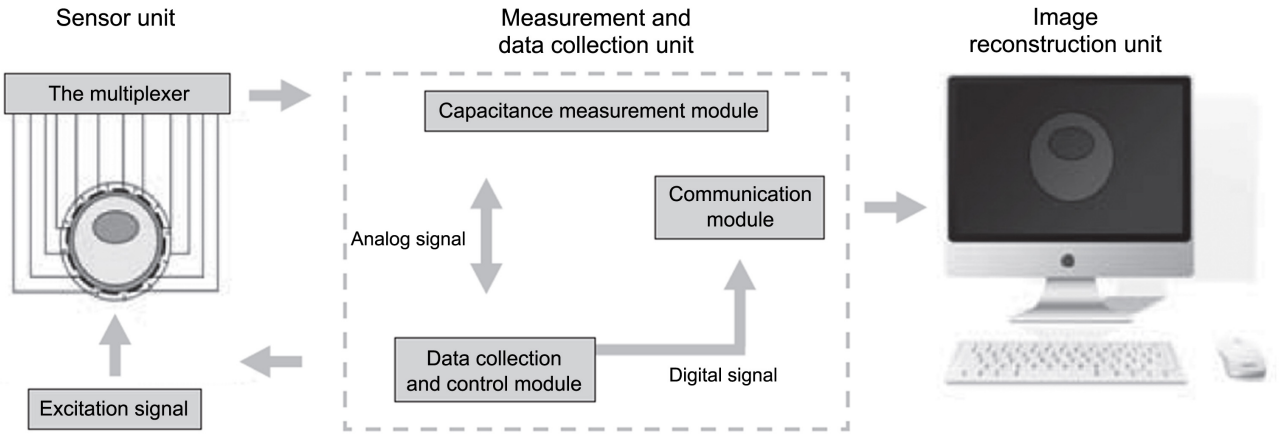

Figure 4. Constitutes of electrical capacitance tomography system [17].

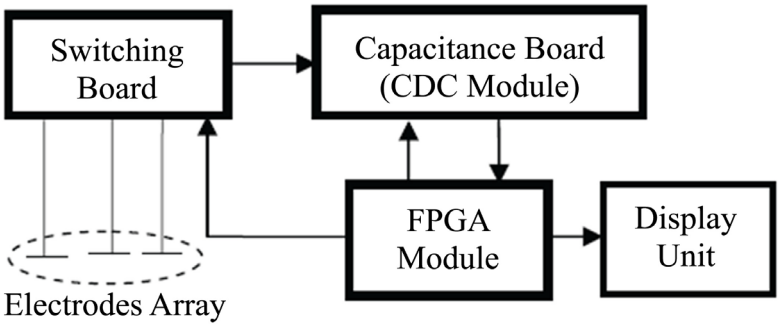

Figure 5. Hardware system overview: overall block diagram [18].

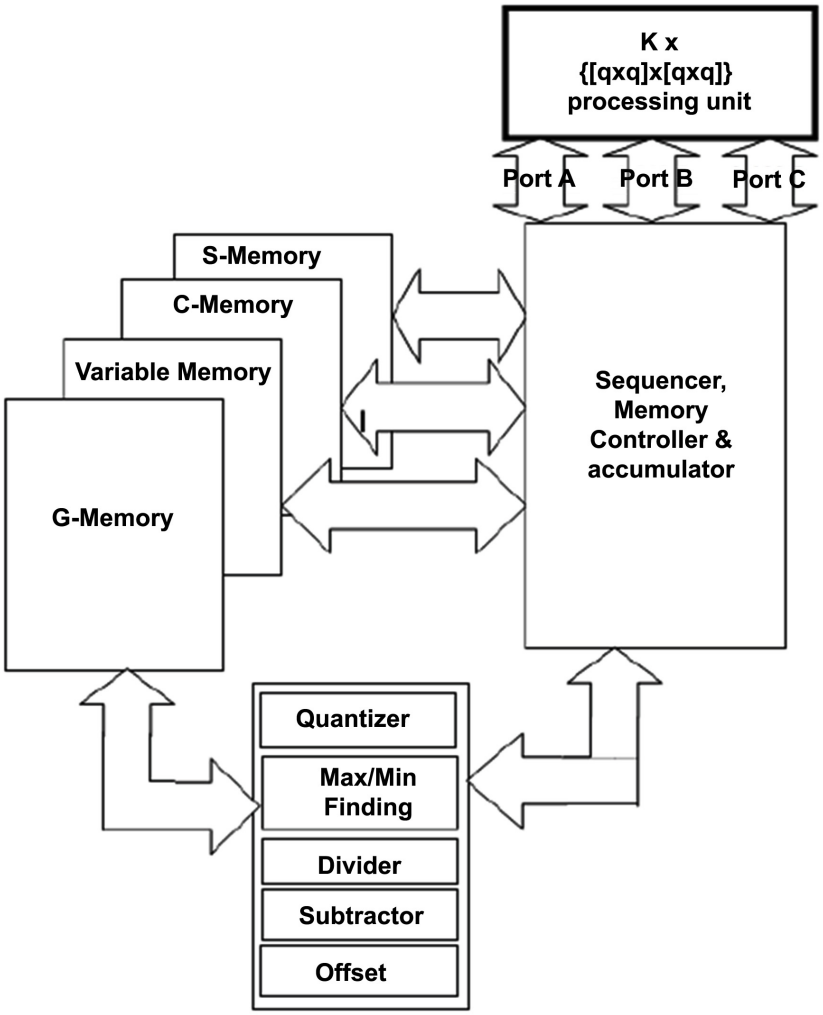

Figure 6. Image reconstruction implementation block diagram on FPGA [18].

of 17 Kframes/sec for the Linear-Back Projection (LBP) algorithm with 200 iterations. The FPGA which play its role in image reconstruction consisted of four modules *i.e.* 1) A parallel processing module, 2) A data-variable input/output memories module, 3) A sequencer and memory controller module and 4) A post-processing module. The concerns of the execution speed and the hardware scalability will need to be address when designing FPGA module. A relative error of less than 15% when 18 - 24 bits are used of quantization effect caused by finite bit widths is observed.

4. Electrical Impedance Tomography (EIT)

The Electrical Impedance Tomography (EIT) images the conductivity distributions inside the human body by injecting currents and measuring induced voltages using electrodes on the surface [19]. The authors in [20] have concluded that the EIT could consist of Digital Signal Processor (DSP) or Field Programmable Gate Array (FPGA) as the main component for waveform generation and phase-sensitive demodulation at this point of time. Attempts have been initiated

using Application Specific integrated circuits (ASIC) for EIT systems [21] but yet to be successful.

The authors in [20] have presented an EIT system with the features of fully parallel, multi-frequency, automatic calibration, pipelining, and long term stability [22]. **Figure 7** displays the block diagram of the KHU Mark2.5 EIT system. The system consists of a DSP-based main controller, FPGA-based intra-network controller, and FPGA-based multiple IMMs. CCS and VM stand for constant current source and voltmeter, respectively. FPGA are selected in the digital design due to its ability to add new functions by only manipulating the FPGA. The FPGA was categorized into two kinds. *i.e.* the intra-network controller FPGA and Impedance Measurement Module (IMM) FPGA. The objective of the work using FPGA is to provide a basis for their future ASIC based work.

Khan [23] has introduced a Field Programmable Gate Array (FPGA) based in Electrical Impedance Tomography system as a medical imaging device. **Figure 8** shows the FPGA design block diagram. It consisted of system controller, FPGA (NI FlexRIO 7952R), ADC modules (NI 5751), Signal Generator (SigGen), Timing and Synchronization (TSync) Module (NI 6674t), relay control, power monitor board (NI X-Series Card 6341) and Analog Front End (AFE). As can also be seen in this work, the motivation of the work is to have a system quickly prototyped and upgraded besides for high frame rate of acquisition. By offloading the computing onto Field Programmable Gate Array (FPGA), they are able to achieve a reduction in throughput required between Field Programmable Gate Array (FPGA) and PC by a factor of 32:1. Signal demodulation and spectral characteristics of higher order harmonics were computed using dedicated FFT-hardware built into the FPGA module to achieve high frame rates.

Wu [24] in their 16 electrode EIT implemented XC3S500E-5FG320 of Spartan3E in their DAQ. The multiplexed switches which controls the excitation

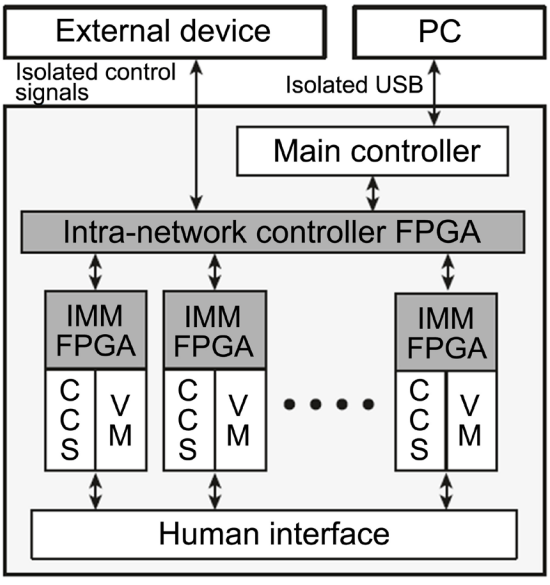

Figure 7. Block diagram of the KHU Mark2.5 EIT system [20].

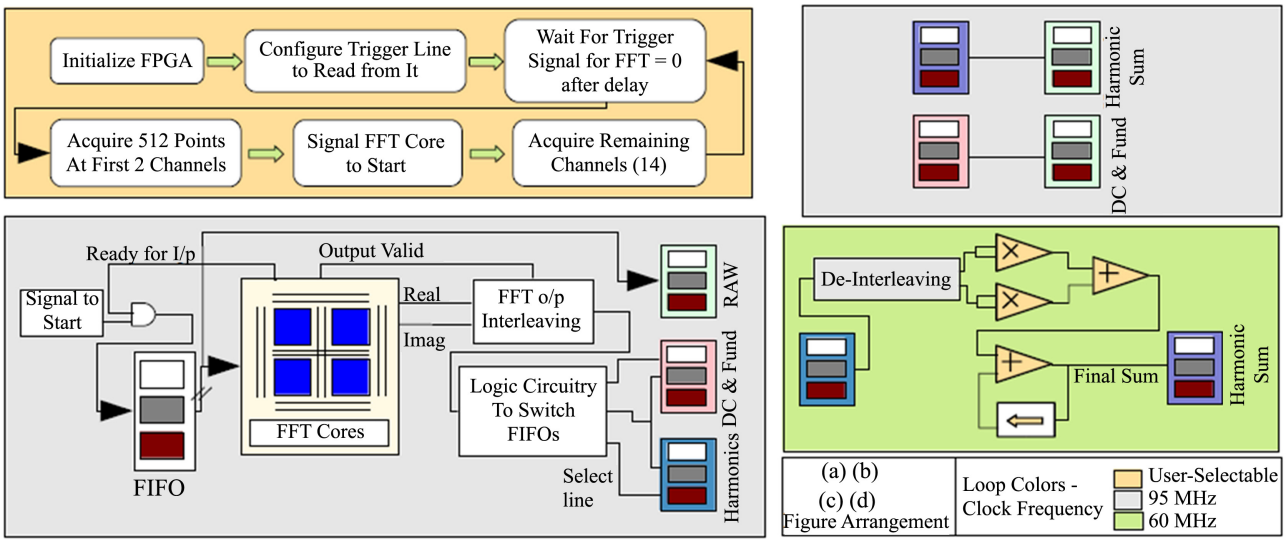

Figure 8. FPGA design block diagram [23].

electrodes and the measured electrodes is controlled by FPGA. Considering the importance of a precise clock for a high-speed digital system to determine work status and accuracy, the XC3S500E was integrated with three digital clock manager (DCM) modules with output of 1) 50 MHz would be the FPGA working clock, 2) 5 MHz to a AD9240, as a sampling clock signal and 3) 125 MHz pulse signals to AD9754, as a digital-to-analog conversion clock signal. In the design, four data-buffering chips 74HC574 are used as buffers to save IO ports of FPGA. Orthogonal sequence demodulation method using FPGA to overcome the short comings appeared in analog demodulation [25]. The performance of their system when 1 mA 100 KHz current implemented on a homogenous tank produces 36 dB signal-to-noise ratio (SNR). On the other hand, Chen [26] has introduced a PXI-based biomedical electrical impedance tomography (BEIT). In the hardware design, there are three main parts, *i.e.* sensor array, data acquisition system (DAQ) and imaging computer. The DAQ system consisted of the signal source module, the switch module, the signal conditioner module and data acquisition card module. A FPGA, Xilinx Spartan-3E direct digital synthesizer (DDS) module will be used to produce a 100 kHz sinusoidal digital signal. In conclusion, the hardware system could be simplified and system scalability enhanced using PXI platform besides reducing the time of development process and increasing measurement accuracy.

5. Ultrasonic Tomography

Ultrasonic, by definition are sound waves that propagate above 20 kHz at the range above a normal human hearing [27].

Bharath [28] has applied FPGA based kintex7 board in the low complex adaptive speckle suppression filter. **Figure 9** shows the hardware architecture of low complex adaptive filter for FPGA Kintex7. In the B-mode ultrasound images, the speckles will always tried to be reduced as it masks the fine information available.

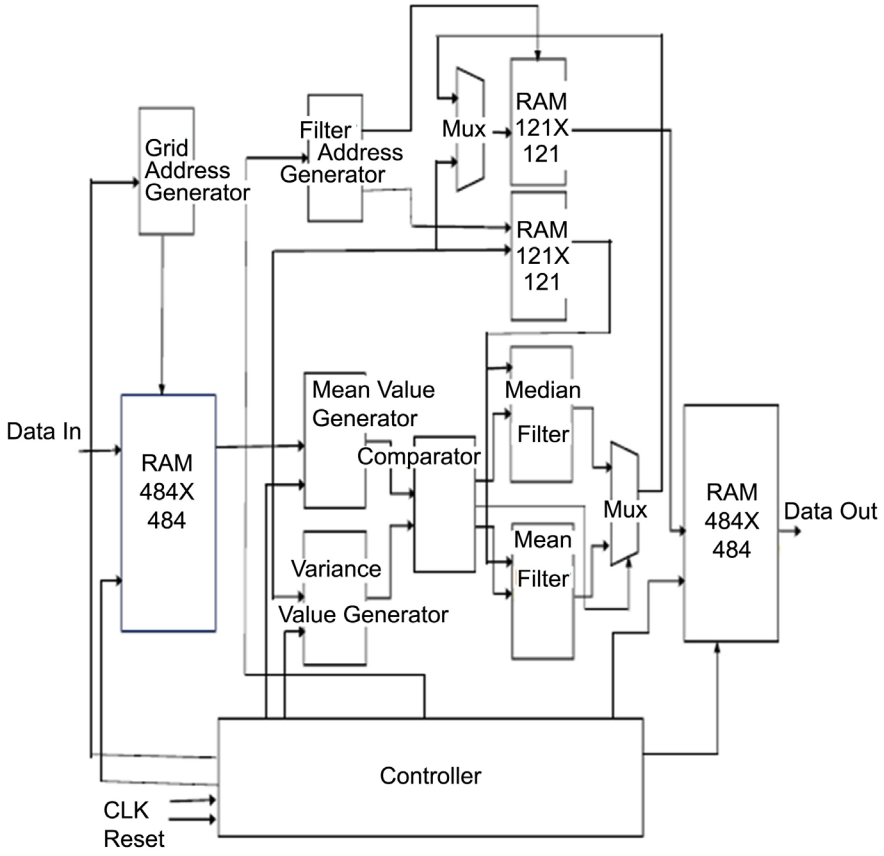

Figure 9. Hardware architecture of low complex adaptive filter for FPGA Kintex7 [28].

The filtered image of an ultrasound phantom is used to evaluate the filter performance via plotting the pixel variations of original image. It has 50% less computations per pixel with respect to typical adaptive speckle suppression algorithms when implemented on mobile ultrasound platforms. The FPGA in the device usage of 0.974% of slice logic of kintex7 board helps to minimize the area overhead when implemented in Application Specific integrated circuits (ASIC). 2.31 ms per pixel was obtained when Low Complex Adaptive Speckle Suppression Filter in kintex7 was operated at 100 MHz for an ultrasound image of dimension 484 × 484.

Krishna [29] designed an algorithm on FPGA of ultrasound imaging for automatic detection of kidney abnormality based on wavelet based noise removal, automated feature selection and supervised classification. Noises are reduced via wavelet based pre-processing methods [30]. The author classified the kidney using Intensity Histogram and Haralick features depending on range of feature values. **Figure 10** shows the system architecture on FPGA which consists of pre-processing, feature extraction, feature selection, classifier and diagnosis. Kintex 7 Field Programmable Gate Arrays (FPGA) was synthesized and processes the HDL code using Xilinx ISE. The achievement on the work is the abnormality could be identified without any error by using the designed classifier.

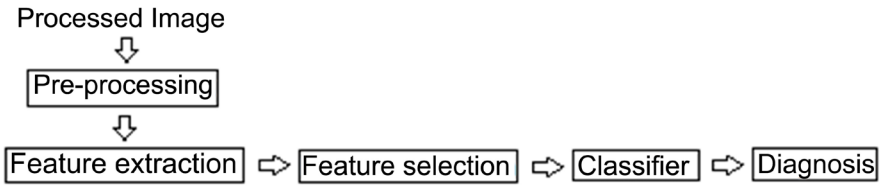

Figure 10. System architecture on FPGA [29].

6. Other Types of Tomography

Choi [31] has implemented three dimensional computed tomography (CT) using an expectation maximization (EM) in which their contributions lies in external memory bandwidth reduction strategy by reusing both the sinogram and the voxel intensity. The customized computing engine was using FPGA to increases the effective memory bandwidth. A saturation point *i.e.* a condition where the performance will be stagnant on the improvement in computing elements is applicable to GPU and FPGA [32]. Thus, it is observed that previous work such as shown in [32] [33] [34] focused on minimizing the memory accesses but often had a cap. The author has suggested that significant speedup could be obtained via EM repetitive access pattern. When comparing the performance of FPGA with respect to GPU, FPGA had higher reuse opportunity and the customized architecture but has 8 times slower clock frequency. The work on FPGA is 85 times faster than single-threaded CPU on an actual patient.

Shinde [35] had implemented image fusion system hardware which implementing FPGA to get fused image. Image fusion is a process of getting a single image via combining relevant information of at least two images. Information obtained from Magnetic Resonance Image (MRI), Computed Tomography (CT), Positron Emission Tomography (PET), and single Photon Emission Computed Tomography (SPECT) is used to form fused images, which could be either from the same imaging modality or multiple modalities. **Figure 11** shows the flow chart for FPGA implementation of image fusion. The author has carried out the implementation as follows. Input images are converted into header files using Matlab GUI feature. Xilinx Platform Studio (XPS) is included to process hardware and software components. The steps taken are 1) select hardware configuration, 2) selection of software architecture and 3) finally download the hardware and software architecture bit streams into FPGA and execute it.

Rohan [36] had successfully accelerated Single-Photon Emission Computed Tomography (SPECT) Monte Carlo simulations by two orders of magnitude. The Monte Carlo simulations architecture shares a data set which could not be replicated for each processing unit due to its huge size. All the four modules of Arbiter, Cordic Processor, SPECT Image and Monte Carlo simulation are designed by VERILOG and synthesized by using Xilinx ISE 12.2 version tool. Verification of design functionality is done using Modelsim tool. The challenge that needs to be issued is on the matter of the method to arbitrate access between the hundreds of PUs and the single copy of the data set so that each experiment can

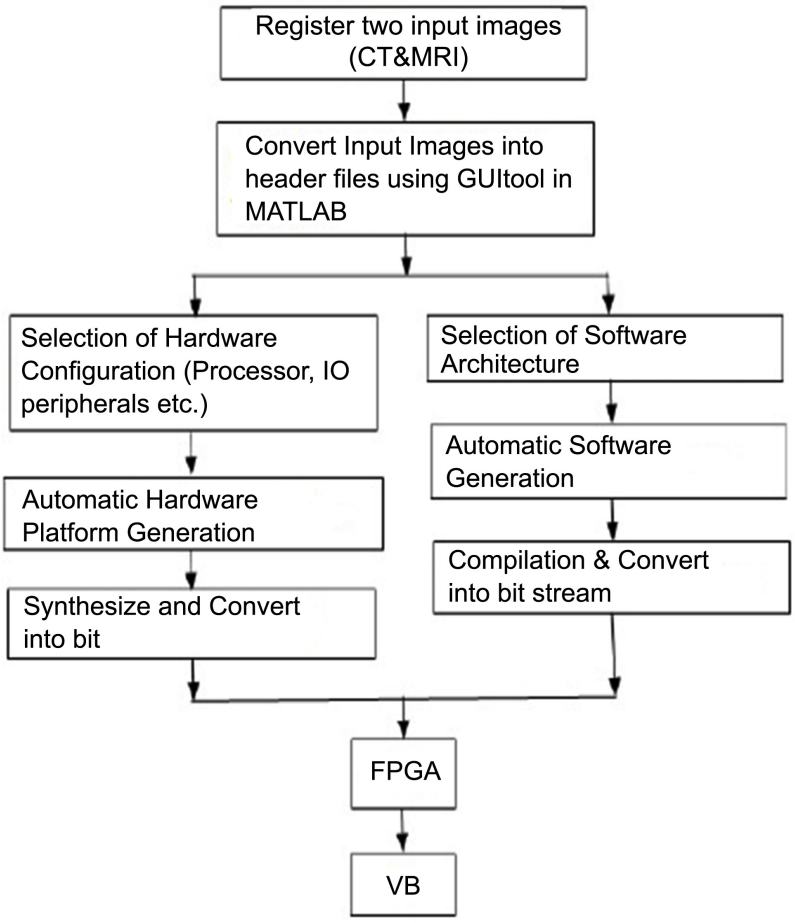

Figure 11. Flow chart for FPGA implementation of image fusion [35].

continue without being data starved. Higher data latency is needed to locate the data set centrally and arbitrate access to it. In their design, over 40% are on-chip network from the device's logic resources. The conclusion that could be drawn from the work is the significant speedups could be obtained via parallel architecture FPGA with respect to single core implementations on SPECT imaging without sacrificing the image reconstruction accuracy. The Network-on-chip (NoC) method could support FPGAs of larger capacity because it is modular.

Chen [37] in their work on the other hand has shown that a hybrid approach (CPU + GPU + FPGA) could be better than only GPU implementation in terms of performance and energy efficiency. It also has 13 times improvement of throughput compared to a dual-core CPU implementation. The author had implemented a combination of Expectation Maximization (EM) and Total Variation (TV) or EM + TV reconstruction algorithm using virtex 6 FPGA. In the streaming architecture, the function *tracer_precal* (refer to original paper) and the tracer loop computation can be run in a task-level pipeline (**Figure 12**). For a 128^3 test data, the latency of the tracer loop is approximately 4 times the latency of the *tracer_precal*. Thus, they have implemented two *tracer_precal* modules and eight tracer loop module in a single FPGA. Each FPGA has 16 virtual

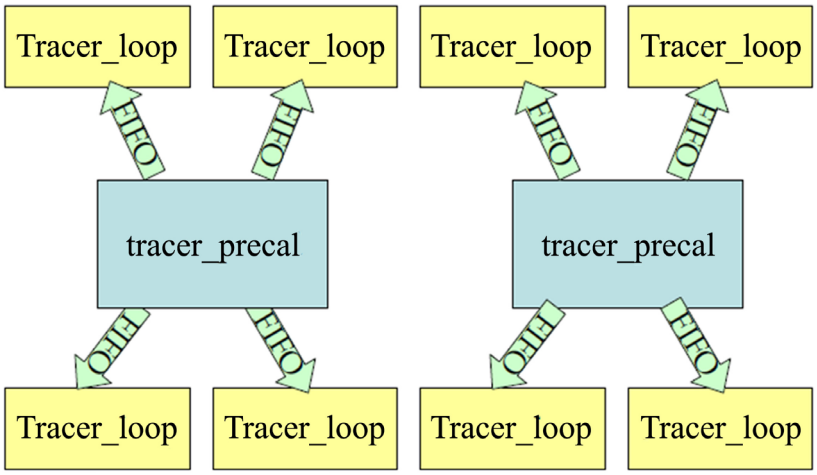

Figure 12. Overall streaming architecture inside one FPGA AE [37].

memory channels, and each tracer loop module talks to two of them *i.e.* one for read and one for write. The multi-FPGA system has 4 user FPGAs (Application Engine or AE) and they have distributed the work-load using SIMD fashion. The ability to reconstruct two images simultaneously resulted into better throughput of the FPGA design than the latency. Thus, the FPGA-engine is 3X faster than Tesla C1060 and in par with Fermi GTX480. Besides that, when the latency of forward and backward is added together, their multi-FPGA engine is about 50% faster than the CUDA implementation on Tesla C1060, but about 2X slower than Fermi GTX480. Overall, the FPGA platform provides a good performance with a much lower energy.

Tiemei Yang [38] has used a high frequency and highly integrated Field Programmable Gate Array (FPGA) based induction measurement system which applicable for low conductivity objects measurements. **Figure 13** shows their system hardware structure. The Field Programmable Gate Array (FPGA) is used in their main board as the Data Acquisition Board (DAQ), interfaced with two A/D converters, two D/A converters and uses an USB module to communicate with a PC. Field Programmable Gate Array (FPGA) was used to perform measurements at frequency steps of 10 kHz. Higher excitation frequencies (above 1MHz) are required to get acceptable sensitivity for lower conductivities liquids for applications of multiphase flow imaging and level measurement [39]-[44].

7. Comparison of FPGA with Competitor Technologies

Application Specific Integrated Circuits (ASIC) are customized ICs whose internal functional operation is user defined. *FPGA* requires user hardware programming to perform the desired operation. The *circuit level design* of an *ASIC* chip involves circuit components design, placement, and interconnect routing.

When comparing between FPGA and ASIC, FPGA are better for the following reasons [9]: 1) Costs and Flexibility due to reprogrammable after manufactured; 2) Design Time Risk Reduction Versus Speed. For the later reason, the FPGA,

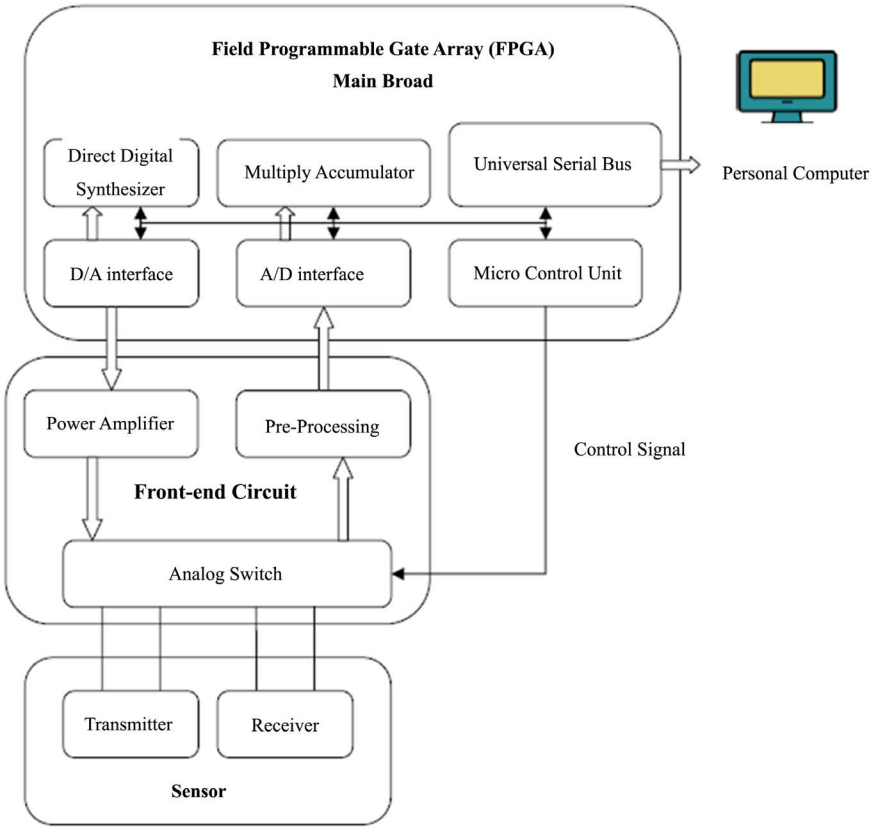

Figure 13. System hardware structure [38].

usually, could provide sufficient performances which are better than non-latest ASIC with a lower total cost of ownership (TCO) and greater flexibility. Nevertheless, the best ASIC could always out beat the fastest FPGA as these two technology progresses.

Syed M. Qasim, [8] has introduced a Field Programmable Gate Array (FPGA) based matrix multiplication provides speed-up in computation time and flexibility compared to software and ASIC based method. Two advantages of using Field Programmable Gate Array (FPGA) *i.e.* able to run at a speed more than 500 MHz [45] and potential for dynamic reconfiguration [46]; that is, reprogramming part of the device at run time so that resources can be reused through time multiplexing. Syed M. Qasim design methodology is based on a parallel array design that maps a nested loop algorithm onto the parallel architecture. Their contributions lies on firstly has better speed and required less area as compared to previous reported FPGA implementation of matrix multiplication and secondly, high throughput architecture for matrix multiplier is developed using advanced design techniques. In FPGA, the advantages of fixed point implementations are fast, consume less power and less gates compared to floating point while the disadvantages are representation of very small numbers and very large is not possible besides the range is limited to bit-width of the number. Potential application would be in the Linear Back-Projection (LBP), an image reconstruction algorithm [47], higher-order cross moments are commonly used in

digital signal processing applicable sonar, radar, seismic data processing, adaptive filtering, array processing, speech and image processing, motion estimation and biomedical signal processing [48] and for the fast estimation of higher-order cross moments, the problem is formulated as a series of matrix multiplication operation. Their implemented matrix multiplier supports partial reconfiguration *i.e.* possibility of changing the design implementation without stopping the whole execution process.

An example of performance comparison between FPGA and graphics processing unit (GPU) is investigated by Birk [49]. **Figure 14** shows the block diagram of the digital part of a First Level Cards (FLC) in the DAQ system. The motivation of his work is due to the need to improve the duration of the image reconstruction which currently limits the clinical applicability of the overall imaging method. The core element is a Synthetic Aperture Focusing Technique (SAFT) [50], which exploits the pressure over time information in the A-Scans in order to create reflectivity images. Parallel processing in application-specific hardware would be an alternative worth exploring to reduce time for image reconstruction. The Graphics Processing Unit (GPU) and Field Programmable Gate Arrays (FPGA) are both used in the DAQ system and compared with respect to the SAFT reconstruction kernel performance. The GPU has the highest performance although all system architecture accelerates processing.

A comparison on performance of FPGA, CPU and GPU was done by Asano *et al.* [51] on different image processing applications with the findings of the FPGA have improve significantly the speed of stereo-vision and k-means clustering application except for two dimensional filtering. In another example, when comparing the performance and development time for a real-time capable optical

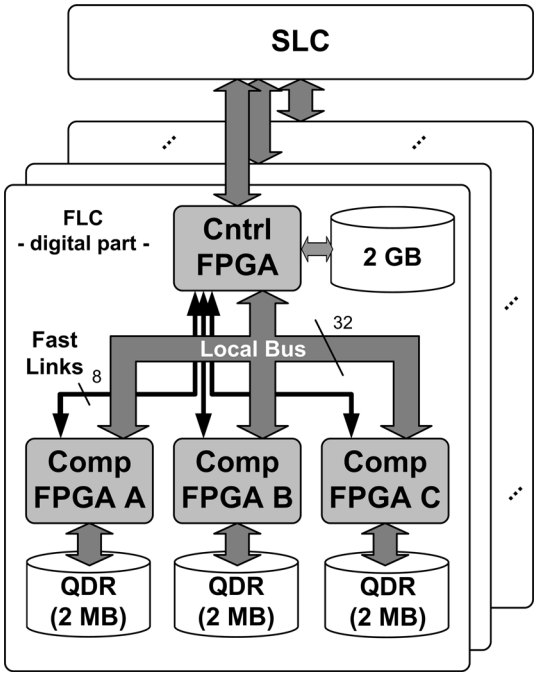

Figure 14. Block diagram of the digital part of an FLC in the DAQ system [49].

flow algorithm between a FPGA and GPU, both architectures are in agreement from the point of performance but FPGA is 10 times faster in terms of development time [52]. Kalarot *et al.* [53] found custom tailored FPGA is better for processing performance but GPU are more flexible and shows the 50-fold performance of a single-core CPU for real-time stereo vision. In a comparison for Gaussian-Elimination, Data Encryption Standard (DES) and the Needlemam-Wunsch algorithm [54], the three compute-intensive applications concluded that GPU has better performance whereas the FPGA is more computational efficient, measured in number of execution cycles.

Nicolas introduced an architectures of general purpose CPU, GPU, and FPGA/ASIC are used to improve the speed of Back-projection (BP) algorithm [55]. Temporal and 3D spatial locality in the BP algorithm was exploited. The prefetched and parallelized architecture for PET, 3PA-PET. According to the author, the reconstruction time is the best in the following order, firstly GPU, 3PA-PET and finally the CPU. The 3PA-PET makes the best use of the pipeline and the clock cycles. Under the same variable, ASIC would save more energy and would be 2 times faster with respect to GPU and 20 times with respect to CPU. In another comparison between FPGA and General Purpose Processors (GPP) in Fourier Domain Optical Coherence Tomography (FD-OCT) [56], the GPP implementation was not able to scale as the data resolution and acquisition speeds from newer cameras increases. At this point of time, a quad core Intel i7 3 GHz with 3GB of RAM and FD-OCT software could have a throughput rate of 30 MB/s [57]. In the work, the predicted required throughput rate for the DAQ was 8GB/s [58]. The need of higher processing speeds also comes with by stacking multiple 2D FD-OCT images in real time to form real-time 3D volumetric. In FD-OCT, the low production volume resulted in the ASIC solutions would not be an option. On the other hand, the General Purpose Graphical Processing Units (GPGPU) are coarse-grained parallelism available via many processing cores and a large on-chip cache. FPGA, the fine-grained parallelism would be available although have less on-chip memory. The contributions in the work includes 1) The GPGPU has a maximum throughput of 527 MB/s in the complete FD-OCT system; 2) The Xilinx Virtex 5 FPGA devices in a fully-pipelined FD-OCT processing with the maximum processing throughput of one pipeline is 465 MB/s, which can be increased by replicating it.; and 3) FPGA could do what GPGPU could not to meet future data acquisition rates.

Finally, it is possible to implement a combination of these technologies complementing each other in a single tomography system. For instance, in the Positron Emission Tomography (PET) system by [59] had implemented a FPGA based Time to Digital Converter (TDC) which is controlled by a 32-bit MicroBlaze microprocessor. The purpose of TDC is to identify events and provide a digital representation at the time they occurred.

8. Conclusion

Overall, there is no absolute superiority between competing processor technolo-

gies when it comes to their application in process tomography system. However, there is a slight preference among researchers to use FGPA due to its ability to be reprogrammed and yet still provides impressive performance. Due to these characteristics, most researchers took advantage to test their prototype using FPGA before using other processor technologies in their final product.

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Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

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