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Dual-Delay-Path Ring Oscillator with Self-Biased Delay Cells for Clock Generation

Agord de Matos Pinto Jr[1,2], Raphael Ronald Noal Souza[1,2], Mateus Biancarde Castro[2], Eduardo Rodrigues de Lima[2], Leandro Tiago Manêra[1]

[1]School of Electrical and Computer Engineering (FEEC), University of Campinas, Campinas, Brazil
[2]Eldorado Research Institute, Campinas, Brazil
Email: agord@dsif.fee.unicamp.br

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Abstract

This work summarizes the structure and operating features of a high-performance 3-stage dual-delay-path (DDP) voltage-controlled ring oscillator (VCRO) with self-biased delay cells for Phase-Locked Loop (PLL) structure-based clock generation and digital system driving. For a voltage supply $V_{DD} = 1.8\,\text{V}$, the resulting set of performance parameters include power consumption $P_{DC} = 4.68\,\text{mW}$ and phase noise $PN@1MHz = -107.8\,\text{dBc/Hz}$. From the trade-off involving P_{DC} and PN, a system level high performance is obtained considering a reference figure-of-merit ($FoM = -224\,\text{dBc/Hz}$). Implemented at schematic level by applying CMOS-based technology (UMC L180), the proposed VCRO was designed at Cadence environment and optimized at MunEDA WiCkeD tool.

Keywords

Phase Locked Loop (PLL), Voltage-Controlled Ring Oscillators (VCRO), Dual-Delay-Path DDP, Delay Cells

1. Introduction

Oscillating structure design plays a critical role in the telecommunication systems operation [1]. In this context, voltage-controlled oscillators (VCO) are applied in analog-to-digital converters (ADC), in phase-locked loop (PLL)—based frequency synthesizers (FS) for clock and data recovery circuits (CDR) in serial data communication [2] [3], disk-drive read channels [4], on-chip clock distribution [5], and also for the local oscillator (LO) signal generation in radio frequency RF transceivers [6]. When compared with LC tank resonance-based oscillators, the set of structure and operating features of ring oscillators involves higher integration level in CMOS-based technologies (smaller area), the possibility of voltage or cur-

rent-based frequency control, extended linearity and wider tuning range.

In this application context, different ring oscillators-based proposals have been reported in the literature [7]-[13], by applying the design flexibility involving the delay cells topology implementation, the number of delay cells and the corresponding connection pattern architecture. This architecture-based flexibility allows a multi-phase signal generation (multiple oscillation nodes) but, on the other hand, implies an increased number of delay cells and additional resulting features: increased power consumption, higher area, lower oscillation frequency and degraded phase noise. The work in [8] proposes a 3 delay cell-based digitally controlled ring oscillator by applying single-ended tri-state inverters. The work in [9] applies a four-stage ring structure with fully differential delay-cells for maximizing phase noise performance. A three-stage structure with differential cells is proposed in a proper frequency range for RFID applications, according to the work in [10]. On the other hand, by applying a wideband two-stage ring structure, the work in [12] presents a linear modeling proposal and defines a correlation in frequency with the 3-stage counterpart. Finally, from the referred architecture level flexibility, a multi-loop differential ring VCO is presented in [11] considering a proprietary differential delay cell with additional interconnection pins for comprising additional loops for signal flow. In this context, implying an extended design complexity, multi-loop or dual delay-path (DDP) based-architectures have been applied for rebalancing the parameter trade-offs through additional delay path or operating loop generated through auxiliary devices at delay cell topology level. From this solution, the resulting level of oscillation frequency and phase noise performance trades with dynamic power consumption and additional routing lines in the physical level.

Considering these set of reference concepts and operating trade-offs, this work describes the implementation features concerning a 3-stage dual-delay-path DDP voltage controlled ring oscillator VCRO designed for clock generation with self-biased pseudo-differential delay cells and interconnection buffer. The reference VCRO were designed at schematic level from Cadence Analog Design Environment (ADE) and optimized at MunEDA WiCkeD environment [14] [15] [16] [17] by applying standard CMOS-based technology (UMC L180 MM/RF).

This work is organized as follows: section 2 describes the implementation features for the reference VCRO (architecture, delay cells topology and buffer structure), section 3 indicates the adopted EDA-based analog design flow and the reference metrics for final results evaluation, section 4 summarizes the resulting curves and wavesforms and section 5 reports the final conclusions.

2. Reference Circuits: Structure and Operation

Considering a general top level representation for the implemented system, according to **Figure 1**, the building block on the left (**Figure 1(a)**) represents the ring oscillator RO-based module and the block on the right (**Figure 1(b)**) indicates the interconnection buffer IB (connected to one of the RO output voltage nodes) for providing a higher level of driving capability.

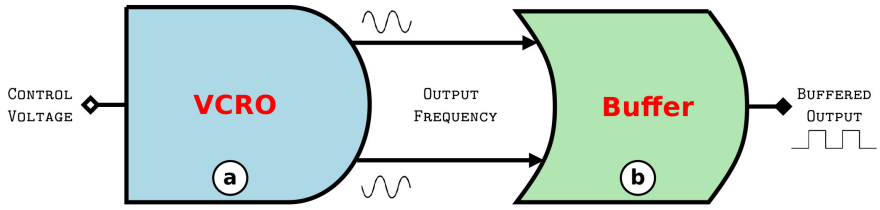

Figure 1. Block diagram: (a) ring oscillator and (b) output buffer.

2.1. Voltage-Controlled Ring Oscillator

A number of delay cells connected in a positive or regenerative feedback loop compose a main basis for ring oscillator structures [18]. In contrast with the single-ended counterpart, differential delay cells are widely used for providing both differential output signal and a higher level of common-mode rejection from supply disturbances and substrate induced-noise [19]. In this context, the differential topology can be further classified as fully-differential or pseudo-differential, according to the presence or absence of a tail current source [20]. Thus, ring oscillator design process involves a proper selection of the adopted delay cell topology and the optimum number of delay cells. In general, a variable number of 2 to 4 stages are commonly applied for typical design in communication systems [18].

The architectural features associated with the 3-stage DDP-based VCRO are represented through the diagram in **Figure 2**. Considering the illustrated diagram, the black connection lines indicate the main signal path, and the set of additional lines indicate the auxiliary path for composing a fast sub-feedback loop.

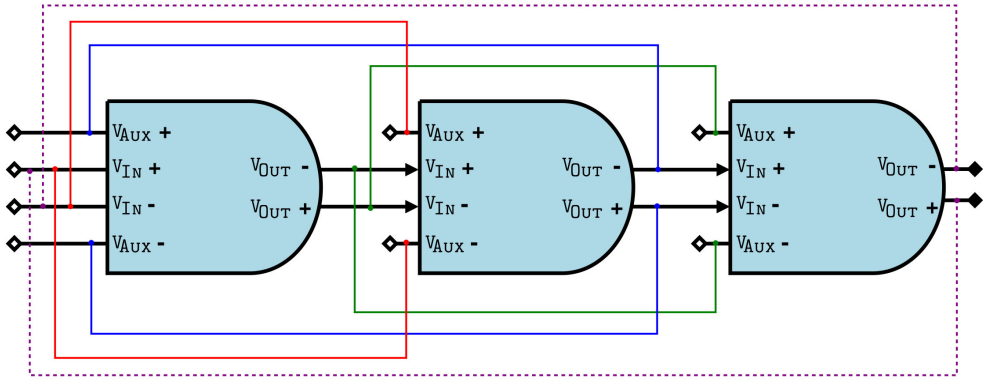

Figure 2. DDP-based VCRO architecture: interconnection pattern.

By applying a self-biased topology, the adopted structure for delay cell implementation is represented at schematic level through the diagram in **Figure 3**. In this case, according to the referred scheme, the adopted topology can be described from the set of 4 indicated device-based structures. NMOS differential pair (M1/M2—lower dashed rectangle) is associated with the primary signal path, and the PMOS differential pair (M5/M10—upper dashed rectangles) is associated with the auxiliary signal path. Additionally, a PMOS varactor (M3/M4—middle dashed rectangle) is applied for voltage-based frequency control.

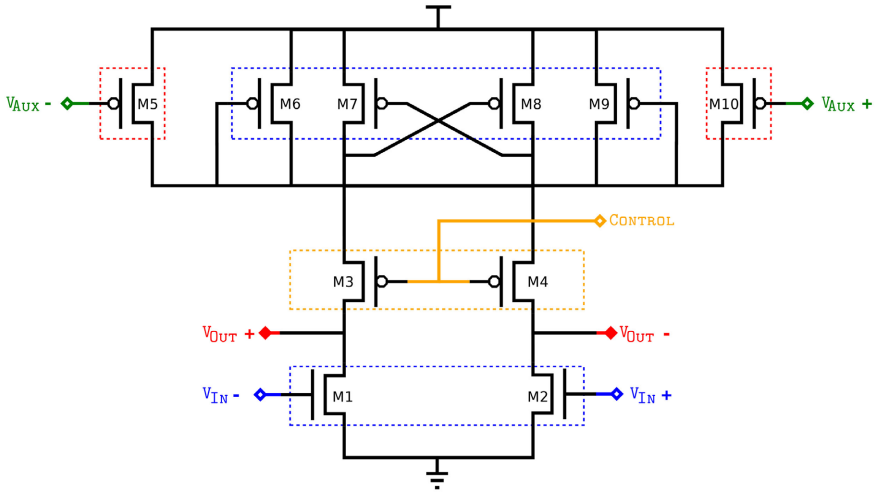

Figure 3. VCRO delay cell topology.

Finally, PMOS-based self-biased active loads (cross-coupled pair M7/M8 and diode connected structures M6/M9—upper dashed rectangle) provide complementary design variables for performance parameters sizing (dynamic behavior, output DC level and oscillation frequency).

By applying linear analysis, the dynamic behavior (DC gain and frequency response) of the applied delay cell can be approximated through the expressions in (1) and (2), considering both 2 pairs of differential inputs.

$$A_{v_{12}} = \frac{gm_{2-10}\left(r_{02} /\!/ r_{06}\right)}{1+\left(gm_{10}-gm_{8}\right)\left(r_{02} /\!/ r_{06}\right)} = \frac{gm_{2-10}R_p}{1+\Delta gmR_p} \tag{1}$$

$$H(s) = \frac{A_{v_{12}}}{1+\dfrac{\Delta gmR_pC_{in}s}{R_p}} \tag{2}$$

Thus, the model in (1) applies the variable gm_{2-10} to indicate gm_2 or gm_{10}, considering the contribution of 2 DC gains (A_{v_1} and A_{v_2}) for composing the resulting output signal. Additionally, considering a reference DC level of output voltage and current consumption, the dynamic behavior of each delay cell can be adjusted from the bias current distribution in each branch of the active loads (M6, M7, M8 and M9).

2.2. Interconnection Buffer

Output buffer circuit magnifies and regulates the output signal of the front circuit and, at the same time it provides large enough current and voltage to drive follow-up circuit. Even more important, it provides the ability of better capacitive isolation, and avoids the VCRO oscillation frequency to increase the frequency traction's impact when there are external effects of loads.

From the requisition for driving capability, 3 stages of signal processing are provided for interconnection buffer implementation, according to **Figure 4(a)**. Thus, considering **Figure 4(b)**, the first stage (topology on the left) provides a single-ended output from a pair of differential inputs, and the remaining stages

(standard CMOS inverter topology represented on the right) provides the required output wave shaping.

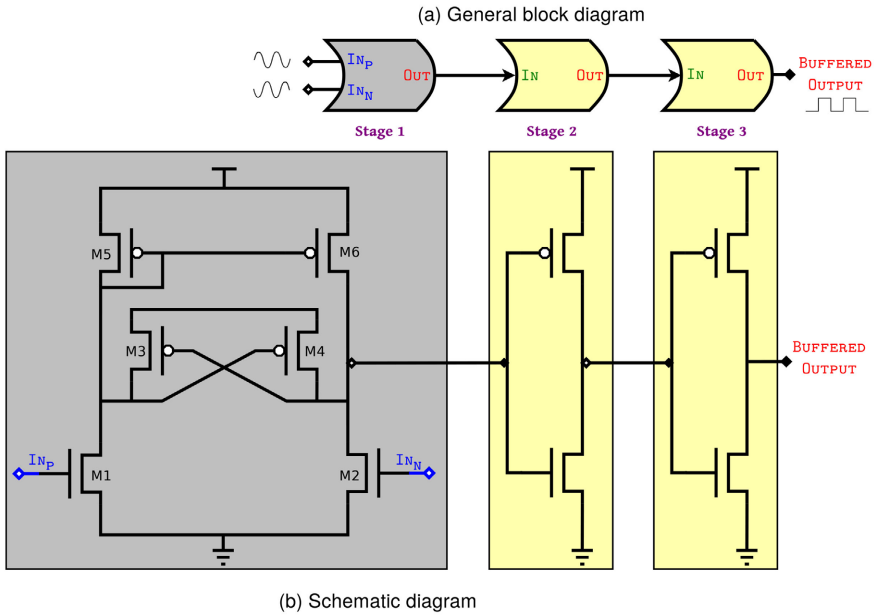

Figure 4. IB architecture and topologies for output driving.

3. Design Environment

3.1. EDA-Based Design Flow

Optimization tools-based design methods for analog blocks implementation represent an effective resource for improving the circuit performance. Thus, the considered analog design flow for electronic design automation (EDA) at schematic level and performance parameters optimization was applied according to **Figure 5**.

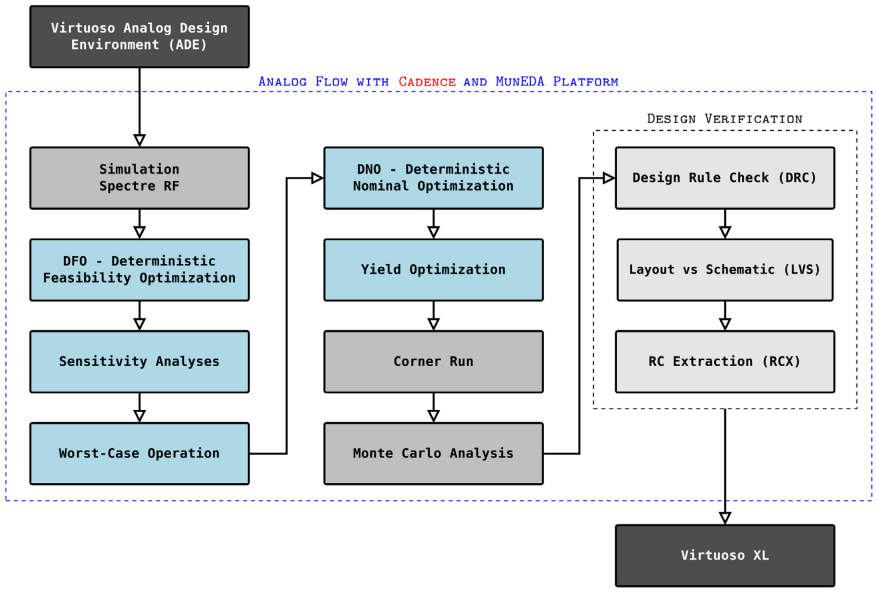

Figure 5. EDA tool-based schematic environment for analog design flow.

3.2. Evaluation Metrics

The primary standard of Figure-of-Merit (FoM), as reported in the literature [21] [22], is applied in this work as a reference metric for oscillators performance evaluation, by considering the trade-off between power consumption (P_{DC}), phase noise $PN(\Delta f)$—(associated with a reference offset frequency Δf) and oscillation frequency f_{Out}, according to (3).

$$FoM = 10\log\left(\frac{P}{1\,\text{mW}}\right) + PN(\Delta f) - 20\log\left(\frac{f_{Out}}{\Delta f}\right) \tag{3}$$

After the optimization-based design stage, a schematic level characterization was applied for obtaining the final performance analysis.

4. Results

Thus, resulting from the operating features associated with the PMOS varactor for voltage-based frequency control, Figure 6 characterizes the resulting VCRO tuning sensitivity K_{VCO} indicating the obtained linear range for the output frequency ($\Delta f_{Out} = f_{Max} - f_{Min} = 880\,\text{MHz} - 280\,\text{MHz} = 600\,\text{MHz}$) and the corresponding range for input control voltage (V_C).

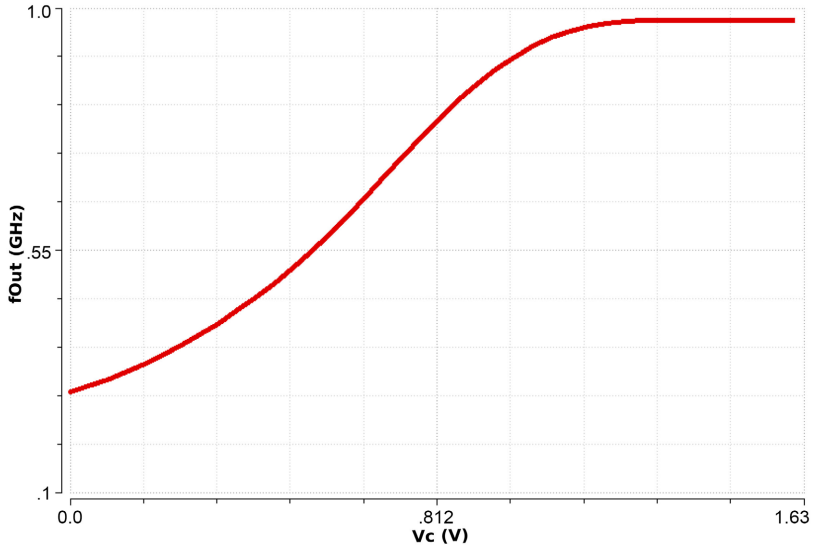

Figure 6. Tuning sensitivy K_{VCO} characterization: $f_{Out} \times V_C$.

Considering an average value for the frequency linear range ($f_{Out} = 550\,\text{MHz}$), Figure 7 illustrates the VCO output waveform (sinusoidal waveform in the upper red line—at the voltage node with buffer connection), and the squared output waveform generated from the buffer (lower blue line) for a capacitive output load $C_{Out} = 3\,\text{pF}$.

Considering a predefined frequency range $f = 10\,\text{Hz}$ to 10 MHz, Figure 8 presents the phase noise (PN) variation with respect to the offset frequency Δf . Finally, Table 1 summarizes a set of reference works for performance comparison (through the standard FoM) by applying the indicated references.

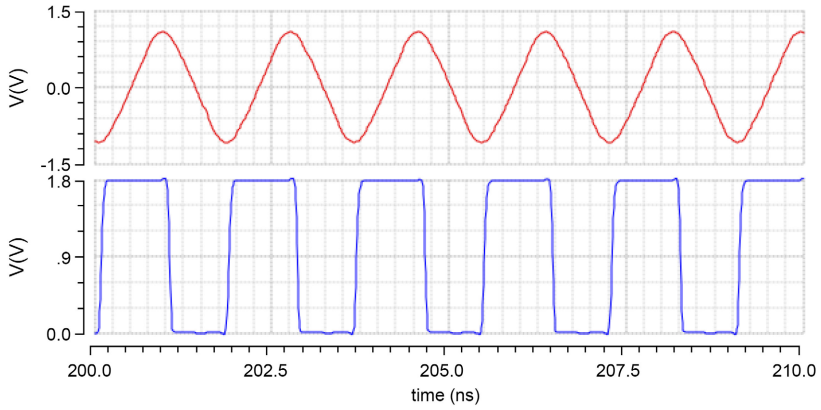

Figure 7. Output waveforms ($f_{Out} = 550$ MHz): ring oscillator and buffer.

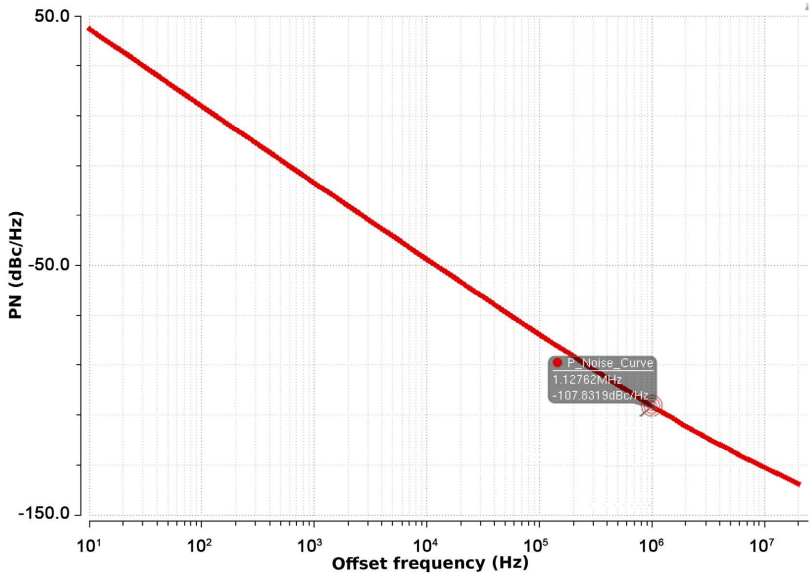

Figure 8. Phase noise characterization: $PN(\Delta f) \times \Delta f$.

According to the table, the first column indicates the set of reference system level design parameters (Process and V_{DD}) and performance parameters (P_{DC}, PN, f_{Out}, Δf) for distributed comparative evaluation. Considering the model in (3), the last parameter indicates the VCO standard Figure-of-Merit (FoM) for characterizing the trade-off between power consumption, running frequency and phase noise through a concentrated comparative evaluation.

Comparatively to the references in Table 1, this work demonstrates the main performance advantage in the power consumption. Despite the performance level evaluated through the comparative table, the VCRO operating features are limited from the poor linearity in the transfer curve. Under a block level perspective, further levels in linearity implies a slope reduction with higher stability and phase noise performance. Under a system level operation perspective, the transfer curve linearity contributes with the stability improvement in the PLL bandwidth and with the availability of an extended range in the frequency operating points for output generation.

Table 1. Performance comparison.

Parameter Symbol (Unit)	References						This work
	[8]	[9]	[10]	[11]	[12]	[13]	
Process (nm)	350	500	180	--	180	180	180
Voltage Supply— V_{DD} (V)	3.3	1.8	1.8	1.8	--	--	1.8
Power— P_{DC} (mW)	63.4	1.2	11.25	72	135	80	4.68
Phase Noise—PN (dBc/Hz)	−106	103.9	−112	−107.7	−82	−85	−107.8
Output Freq.— f_{Out} (GHz)	1.1	0.15	2.45	6.25	5	5	0.56
Offset Freq.— Δf (MHz)	1	1	10	10	1	1	1
FoM	−204	−216	−197	−193	−203	−211	−224

5. Conclusions

This work presented a set of implementation and characterization features regarding a 3-stage dual-delay-path DDP VCRO designed for PLL-based clock generation with self-biased pseudo-differential delay cells and interconnection buffer.

Considering the adopted self-biased delay cell topology and the power consumption level, a proper sizing stage was applied for minimizing the area and maximizing the resulting linearity on the tuning sensitivity ($f_{Out} \times V_C$) by applying the varactor-based frequency control.

From the reference FoM, the final results indicate a higher operating performance when considering the trade-offs involving power consumption and the phase noise. On the other hand, further implementations in this research line should comprise additional improvements in the frequency tuning linearity and alternative hardware strategies for tuning range and phase noise performance.

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Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

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