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CMOS Realization of VDVTA and OTA Based Fully Electronically Tunable First Order All Pass Filter with Optimum Linearity at Low Supply Voltage ± 0.85 V

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Abstract

This paper presents a new first order all pass filter configurations. The proposed all pass filter configuration employs two configurations namely VDVTA and OTAs based first order all pass filter configuration. The first proposed configuration employs a single VDVTA and one grounded capacitor whereas the second proposed configuration employs two OTAs and one grounded capacitor. Both types of proposed configurations are fully electronically tunable and their quality factors do not depend on tunable pole frequency range. The reported configurations yield low active and passive sensitivities and also have low power consumption with very low supply voltage ± 0.85 V with Bias Voltage ± 0.50 V. The PSPICE simulation of the proposed VDVTA and two OTAs based first order all pass filter configurations are verified using 0.18 μm CMOS Technology Process Parameters.

Keywords

Operational Transconductance Amplifier (OTA), Voltage Differencing Transconductance Amplifier (VDVTA), CMOS Technology

1. Introduction

Due to recent development in the fields of microelectronics, analog signal processing as well as digital signal processing and all the fields of communication, size of the transistors and power supplies are reduced. Last few decades, current mode active building blocks have been evolved in the realization of ac-

tive filters and oscillators. Current mode building blocks have higher bandwidth, higher dynamic range and higher slew rate with low power consumption. First order all pass filter and higher order filters are widely used in the fields of analog signal processing, measurement, instrumentation, voice or audio frequency range. The magnitude characteristics play vital role due to insensitivity of ear and Biomedical applications. Recently, most widely active building blocks are used in the designing oscillators, grounded Inductor and active filter applications. These active building blocks namely operational Amplifier, Current-mode current, gain first-order all pass filters employing CFTAs [1], A voltage-mode first order all pass filter based on VDTA [2], Voltage-mode all-pass filters including minimum component count circuits [3], Voltage-mode cascadable all-pass section using single active element [4], Single VDVTA Based Voltage-Mode Biquad Filter [5], Single MO- CCCCTA-Based Electronically Tunable Current/Trans-Impedance-Mode Biquad Universal Filter [6], Electronically Tunable Low Voltage Mixed-Mode Universal Biquad Filter [7], Current-tunable current-mode all-pass section using DDCC [8], Electronically tunable first-order all pass section using OTAs [9], Current-mode multi phase sinusoidal oscillator using CDTA-based all pass sections [10], New resistorless and electronically tunable realization of dual-output VM all-pass filter using VDIBA [11], Cascadable Current-mode first order all-pass filter based on minimal components [12], Voltage-mode all-pass filters using universal voltage conveyor and MOSFET-based electronic Resistors [13], Voltage mode cascadable all-pass sections using single active element and grounded passive components [14], Electronically tunable first-order all-pass circuit employing DVCC [15], Novel voltage-mode all-pass filter based on using DVCCs [16], A Resistorless realization of the first-order all-pass filter [17], High input impedance voltage-mode first-order all-pass sections [18], Unity/variable-gain voltage-mode/current-mode first-order all-pass filters using single DXCCII [19], First-order voltage-mode all-pass filter employing one active element and one grounded capacitor [20], Component reduced all-pass filter with a grounded capacitor and high-impedance input [21], Realization of Grounded Inductor Based Band Pass Filter Design to Achieve Optimum Linearity with Bandwidth using Single VDVTA [22], Multi output filter and four phase sinusoidal oscillator using CMOS DX-MOCCII [23], FDCCII based Electronically Tunable Voltage Mode Biquad Filter [24], CDBA Based Inverse Filter [25].

2. Description of the Proposed Active Building Blocks VDVTA and OTA for First Order All Pass Filter

The symbolical representation of the VDVTA as an active element is shown in **Figure 1** contains three input terminals namely P, N, V and Z, X$^+$, X$^-$ are output terminals. All input terminals and output terminals exhibit high impedance values. The symbolic representation of OTA is shown in **Figure 2(a)** and **Figure 2(b)** represents Equivalent Circuit of OTA respectively. The symbolical representation of the VDVTA as an active element is shown in **Figure 1** contains three input terminals namely P, N, V and Z, X$^+$, X$^-$ are output terminals. All
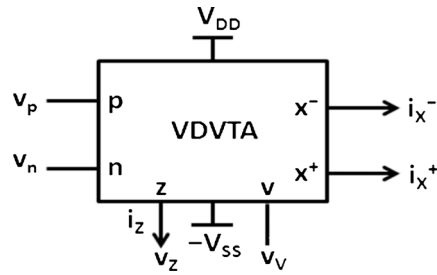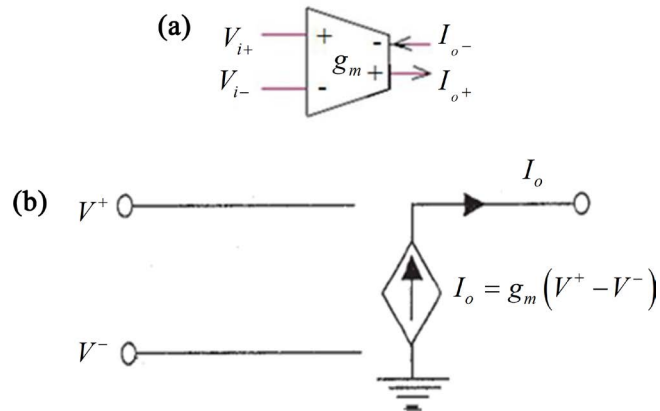
Figure 1. Symbolic representation of VDTA.

Figure 2. (a) Symbolic Notation of OTA; (b) Equivalent Circuit of OTA.

input terminals and output terminals exhibit high impedance values.

The characteristics equations of the proposed VDVTA as active building blocks for realization of first order all pass filter can be reported as Equation (1.0):

$$\begin{bmatrix} I_{X+} \\ I_{X-} \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & g_{m2} \\ 0 & 0 & -g_{m2} \\ g_{m1} & -g_{m1} & 0 \end{bmatrix} \begin{bmatrix} V_N \\ V_Z - V_V \\ V_P \end{bmatrix} \tag{1.0}$$

$$I_{x+} = g_{m_2}\left(V_z - V_v\right) \tag{1.1}$$

$$I_{x-} = -g_{m_2}\left(V_z - V_v\right) \tag{1.2}$$

$$I_z = g_{m_1}\left(V_p - V_n\right) \tag{1.3}$$

The currents I_{x+}, I_{x-} and I_z are characterized by the Equations (1.1). (1.2) and (1.3). The operational transconductance amplifier is the basic building block for realizing all pass filter and I_o is the output current of proposed OTA as an active building block. All terminals of OTA exhibit high impedance values. For an ideal OTA the transconductance g$_m$ and the output current I$_o$ is characterized by Equation (2.0)

$$I_o = g_m\left(V_+ - V_-\right) \tag{2.0}$$

The transfer functions of transadmittance mode all pass filter are employed single VDVTA with one grounded capacitor is shown in **Figure 3** and two OTAs with one grounded capacitor is shown in **Figure 4**.
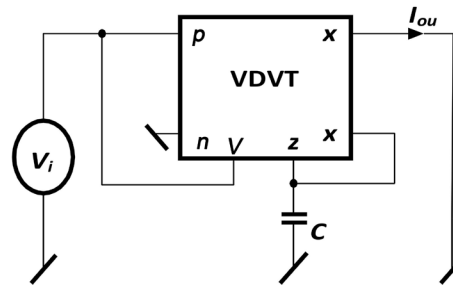
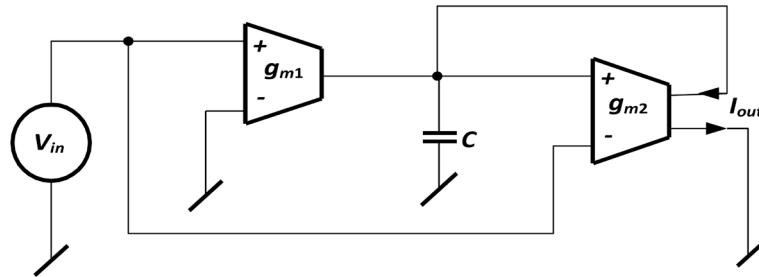**Figure 3.** Proposed VDVTA based all pass filter.

Figure 4. Proposed OTA based all pass filter.

The transfer functions of transadmittance mode all pass filter is given in Equation (2.1)

$$\left|\frac{I_{out}}{V_{in}}\right|_{APF} = \left(\frac{g_{m1} - SC}{g_{m2} + SC}\right)g_{m2} \tag{2.1}$$

The proposed transimpedance mode all pass filter using two OTAs.

OTAs contains high impedance input terminals and the implementation of the proposed transimpedance mode all pass filter using single VDVTA and one grounded capacitor respetively.

Transfer function of proposed OTAs based all pass filter is characterized by the Equation (2.2):

$$\left|\frac{V_{out}}{V_{in}}\right|_{APF} = \left(\frac{G_{m1}}{G_{m2} + SC_1 + 2g_0}\right) \tag{2.2}$$

The phase margin and gain of the proposed all pass filters using two VDVTA and OTAs can be described in Equation (2.3):

$$\frac{V_o(s)}{V_{in}(s)} = \varphi(\varpi) = 180° - 2\tan^-1(\varpi RC) \tag{2.3}$$

3. CMOS Simulation Result

The CMOS Simulation result shows that the workability and functionality of the proposed VDVTA and OTAs based first order all pass filters have been verified using PSPICE. The aspect ratios of MOS transistor for OTA and VDVTA are reported in Table 1. The CMOS realization of the proposed VDVTA and OTAs based first order all pass filters are shown in Figure 5 and Figure 6 respectively. The proposed first order filter configurations are biased with VDD = −VSS =

Table 1. Aspect Ratio of MOS Transistors for OTA and VDVTA.

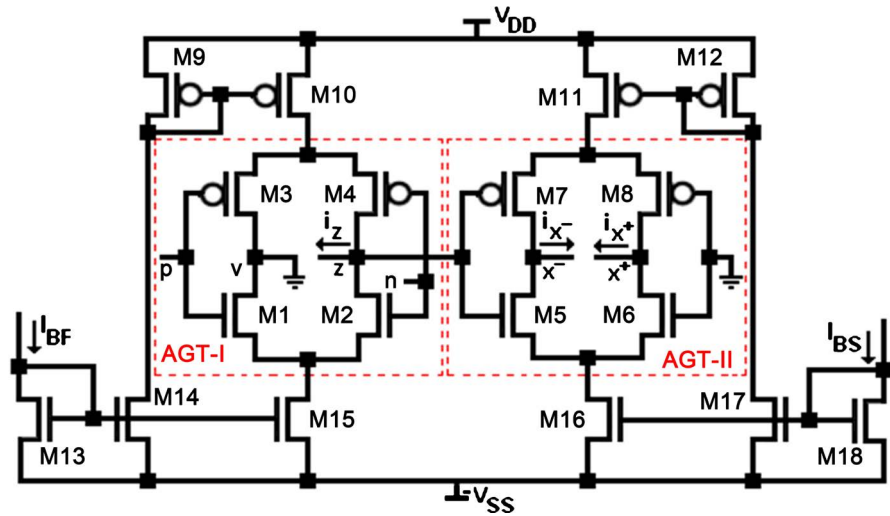| OTA			VDVTA		
MOS Transistor	Width (μm)	Length (μm)	MOS Transistor	Width (μm)	Length (μm)
M1, M3, M5, M7	8.24	0.36	M1, M3, M5, M7, M9, M11	3.6	0.6
M2, M4, M6	7.2	0.36	M2, M4, M6, M8, M10, M12	8.24	0.6
M8, M9	14.4	0.36	M13, M15, M17	7.2	0.6
M10, M11	3.6	0.36	M16, M18	3.06	0.6

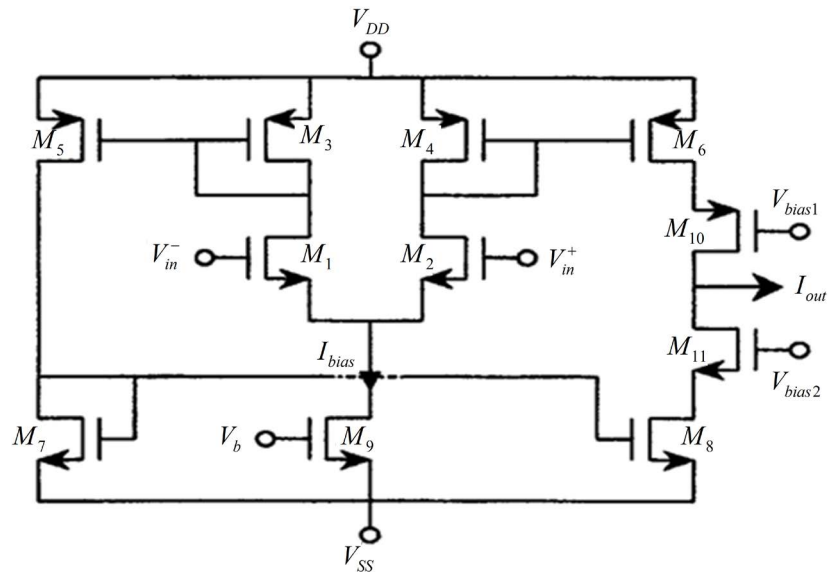Figure 5. CMOS Realization of VDVTA Based All Pass Filter.

Figure 6. CMOS Realization of OTA for the proposed First order all pass filter.

±0.5 V with transconductances at different bias currents are $g_{m1} = g_{m2} = 68.96$ μA/V - 103.7 μA/V for $I_{Bias} = 10$ μA, $g_{m1} = g_{m2} = 86.24$ μA/V - 104.65 μA/V for $I_{Bias} = 20$ μA, $I_{Bias} = 30$ μA, $g_{m1} = g_{m2} = 789$ μA/V for $I_{Bias} = 50$ μA - 70 μA, $g_{m1} =$

g_{m2} = 68.16 - 734 μA/V for I_{Bias} = 100 μA - 150 μA, g_{m1} = g_{m2} = 86.16 - 734 μA/V I_{Bias} = 170 μA - 300 μA. The simulated gain magnitude response 24 dB - 35.13 dB of OTAs based first order all pass filter is in **Figure 7** and the transient response of input and output for proposed first order all pass filters configuration is presented for 0 - 60 mV input and output signal as shown in **Figure 8**. The **Table 2** presents the comparison of the proposed first order all pass filter configuration with the previous reported all pass filter configurations. The percentage of total harmonic distortion for the input of proposed first order all pass filters configuration is observed 1.21% - 2.83% with minimum power dissipation 1.6 mW - 4.76 mW as shown in **Figure 9** and the simulated phase margin of VDVTA based first order all pass filter is approximately from 0 to 180 and 0 to 360 deg or vice versa as shown in **Figure 10**. The pole frequency varies with 90 deg at 1.53 KHz - 10.498 MHz The simulated frequency response of proposed all pass filter configuration is presented in **Figure 11** which yields open loop gain of is 5.045 - 6.020 dB and typical values 30 dB - 71 dB with 4.10 $nV/\sqrt{Hz}$ at the input and 3.8 $nV/\sqrt{Hz}$ noise spectral density at the cut off
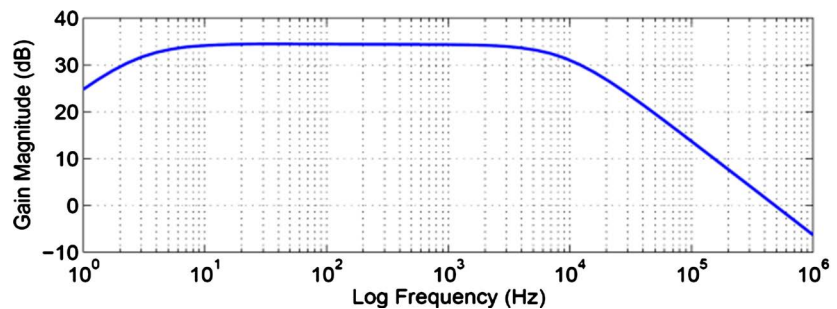

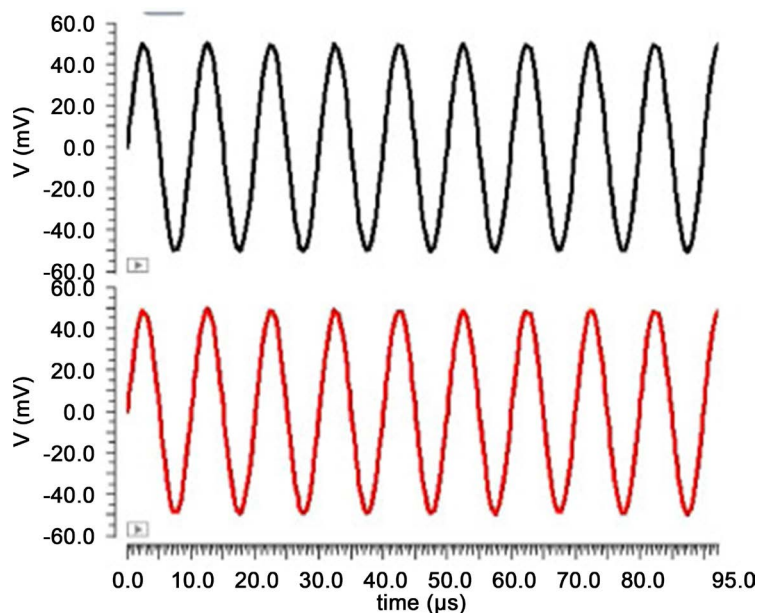**Figure 7.** Simulated gain magnitude response of proposed OTA based all pass filter.

Figure 8. Transient response of the input and output for proposed VDVTA and OTA based all pass filter.

Table 2. Comparison of the proposed All Pass filter Configuration With various All Pass filter configuration.

| Ref No	No of Active Components	No Passive Components floating or Grounded: R - C	Grounded Capacitor	Electronic tunability	Component Matching Condition
1	CFTA	1 Resistor, 1 Capacitor	Yes	Yes	No
2	VDTA	1 Capacitor	No	Yes	No
8	DDCC	3 Resistor, 1 Capacitor	Yes	No	No
9	OTA	1 Capacitor	Yes	Yes	No
10	CDTA	1 Capacitor	No	Yes	No
11	VDIBA	1 Capacitor	No	Yes	No
24	FDCCII	2 Resistor, 1 Capacitor	Yes	No	No
25	CDBA	3 Resistor, 1 Capacitor	No	No	Yes
Proposed Work	VDVTA, OTA	1 Capacitor	Yes	Yes	Yes
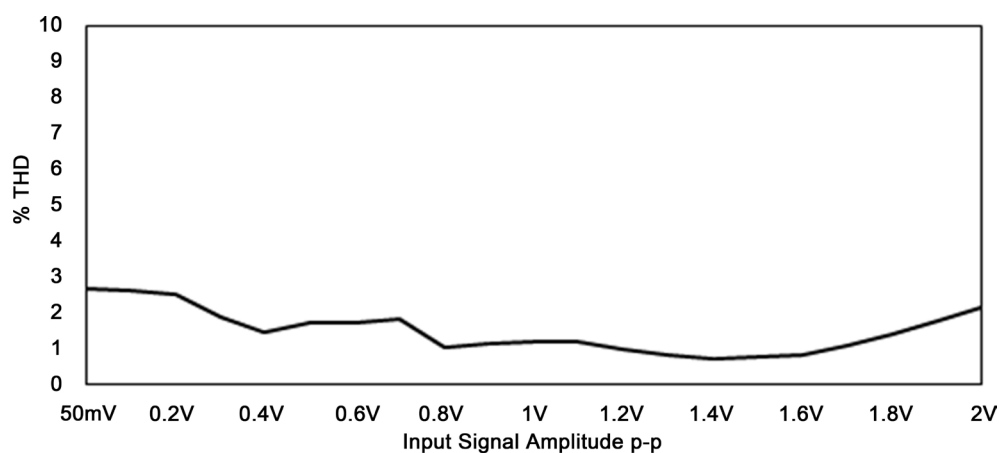
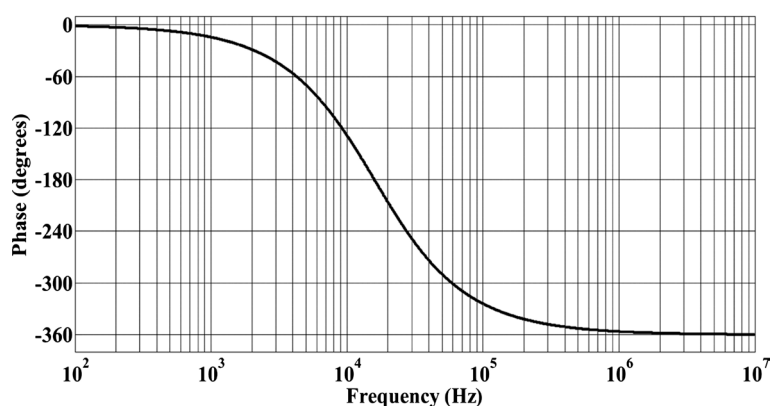**Figure 9.** % THD at the input signal of all pass filter.

Figure 10. Simulated phase margin of proposed all pass filter configurations.

frequency 1.53 KHz - 10.498 MHz and Theoretical (F_{in}) approximately 1.499 KHz with power supply ±0.85 V and Bias voltage ±0.5 V.

The device model parameters are taken from TSMC 0.18 μm have been simu-

lated in PSPICE with high linearity at ±0.5 V Supply Voltage at different bias current. The simulated parameters of the proposed VDVTA and OTAs based first order all pass filters are reported in Table 3. are taken from TMSC 0.18 μm CMOS technology parameters at ±0.5 V supply voltages all gm equal to 639.7 μA/V or 734 μA/V are used for the proposed VDVTA and OTAs based first order all pass filters yield high linearity.

4. Performance Evaluation

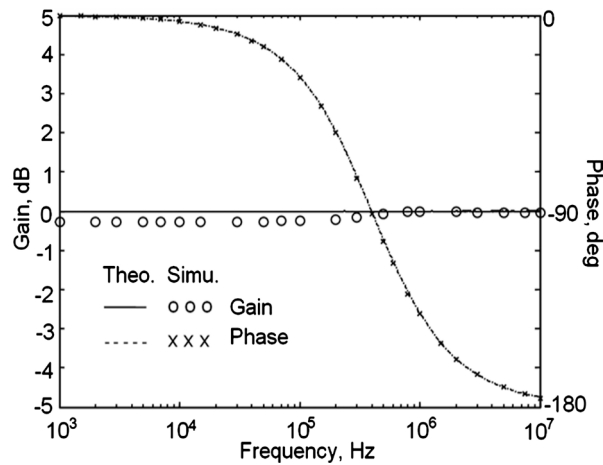The performance of the proposed VDVTA and OTAs based first order all pass

Figure 11. Simulated frequency response with phase of proposed all pass filter.

Table 3. Simulated Parameters of Proposed VDVTA and OTA based All Pass Filter at Different Bias Currents: I_{Bias} = 10 μA - 300 μA.

S. No	Specifications	Simulated
1	CMOS Technology	0.18 μm
2	Transconductances (μA/V)	68.16 μA/V - 789 μA/V at 10 μA - 300 μA
3	Bias current (μA)	10 μA - 300 μA
4	% Total Harmonic Distortion	1.21% - 2.83%
5	Power dissipation (mW)	1.6 mW - 4.76 mW
6	Maximum Input noise (nV)	33 nV- 42 nV
7	Maximum output noise (nV)	24 nV
8	Maximum Supply Voltage (V)	±0.85 V
9	Bias Voltage (V)	±0.50 V
10	Phase Margin	23- 45
11	Input output Voltage Swing (mV)	0 - 60 mV
12	Open loop Gain (dB)	5.045 - 6.020 dB with typical values 30 dB - 71 dB
13	Frequency (KHz)	1.53 KHz and 10.498 MHz
14	Noise Spectral Density	4.10 $nV/\sqrt{Hz}$ at the input and 3.8 $nV/\sqrt{Hz}$

filters are taken from TMSC 0.18μm CMOS technology parameters. The both types of configurations yield low noise and high stability at the desired range of pole frequencies. Transconductance gain is directly proportional to the bias current. The simulated results of all pass filters by OTA observed agree with the simulated results of VDVTA based all pass filter.

5. Conclusions

The workability and functionality of the proposed OTAs and VDVTA based all pass filter are verified with CMOS simulation in the SPICE 0.18 um CMOS Technology. In an analog Signal Processing, first order all pass filter is widely used to shift the phase of input signal.

The reported OTAs and VDVTA based all pass filter yields some advantageous features:

1) Fully integrated with monolithic ICs.

2) Electronic tunability with different pole frequencies at different bias currents.

3) The proposed VDVTA based all pass filter configuration exhibits low input impedance and high output impedance.

4) The proposed VDVTA based all pass filter configuration exhibits good sensitivity performance.

5) The reported work represents wideband bulk-driven OTA with tunable transconductance was designed.

6) The natural frequency (ω_0) of the reported OTAs and VDVTA based all pass filter can be tuned with g_{m2} or gm_2 and with capacitor C2 at constant bandwidth.

7) Bandwidth can be controlled with the help of transconductance (g_{m1}) and quality factor (Q) can be controlled independent of natural frequency (ω_0) with transconductance (g_{m1}).

8) For the first configuration using single VDVTA, we can change cut off frequency or pole frequency by changing g_m.

9) Whereas in second configuration OTAs based all pass filter, the cut off frequency or pole frequency can be changed by tuning g_{m1} or g_{m2}.

10) The integration of proposed OTA and VDVTA based first order all pass filter is open area in future research using modern mixed analog signal processing based integrated circuits for achieving high linearity at low voltage.

Conflicts of Interest

The author declares no conflicts of interest regarding the publication of this paper.

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