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A High-Speed DLL-Based Hybrid Phase Conjugator for 5G Beamforming

Michael Bolt, Mark Adams

Department of Electrical and Computer Engineering, Auburn University, Auburn, AL, USA
Email: mtb0026@auburn.edu

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Abstract

A delay-locked loop based hybrid phase conjugator (DLL-HPC) is presented as a possible solution for 5G beamforming. Theoretical background, unique capabilities, and experimental verification are presented. The proposed DLL-HPC provides backwards compatibility with existing beamforming protocols as well as sub-millisecond beamsteering and automatic mobile target tracking with zero communication overhead. A proof-of-concept DLL-HPC prototype has been constructed from commercially available components to operate in the 5G NR-FR1 band, indicating that the technique can be readily adopted with available technology.

Keywords

Network Architectures and Protocols, Radio Frequency Subsystems, Transceiver Design, Experimental and Prototype Results

1. Introduction

Advanced beamforming techniques have been identified as a key enabling technology for coming Millimeter Wave (mmWave) 5G communications [1] [2] [3] [4] [5]. As carrier frequencies rise into the K and K_a bands, individual antenna element sizes shrink and make extremely narrow, highly directional beams easier to produce [2] [6] [7] [8] [9]. The gain provided by these pencil beams will be necessary to overcome the high path-loss of mmWave frequencies as well as to reduce the amount of interference among the many users [1] [6] [7] [10] [11] [12]. mmWave 5G communications are intended to enable multi-gigabit throughput among many dynamic users within a small area, meaning that new beamforming technologies must not only establish a strong physical link but also continually update it to track moving targets [1] [2] [5] [6] [7] [8] [13].

Many current beamforming techniques, such as those implemented in IEEE 802.11 ad/ay, have high costs associated with them [1]. They rely exclusively on the transmission of beamformer training information between users and can require many communication frames to establish a strong connection, raising communication overhead and reducing throughput [1] [6] [10]. Additionally, these methods only reevaluate the current point if the communication link degrades, making them unsuited for dynamic environments with mobile users [1] [8]. Furthermore, the utilization of pencil beams in mmWave 5G communications could lead to frequent beam switching and deafness when misaligned, owing to a tradeoff between beamwidth and data throughput [4] [7] [10] [13].

A promising solution for establishing and maintaining strong communication links is the retrodirective array (RDA), an antenna array constructed of phase conjugators which transmits back along the direction of arrival (DoA) of a received signal [14] [15] [16]. A phase conjugator design capable of being reconfigured as an actively controlled phase shifter could mitigate the shortcomings of existing retrodirective arrays, such as vulnerability to received signal dropout and a lack of backwards compatibility with existing protocols, while still providing automatic mobile target tracking and lock-on without *a priori* knowledge of the signal's DoA [15] [17] [18]. This work presents a new delay-locked loop based hybrid phase conjugator (DLL-HPC) with rapid settling time, backwards compatibility with existing protocols, received signal dropout immunity, and DoA reporting capabilities. The proposed DLL-HPC is modular in nature, can be used to construct arbitrarily sized and shaped antenna arrays, and is a promising new technology for 5G systems.

This paper is organized as follows. Section 2 details the theory of operation for the DLL-HPC and its functionalities. Section 3 outlines DLL-HPC unique capabilities. Section 4 presents experimental verification from a fabricated 5G NR-FR1 DLL-HPC prototype. Finally, conclusions are drawn and possible applications are outlined in Section 5.

2. Theory of Operation

The proposed DLL-HPC system is shown in **Figure 1**. It is important to note that this system is designed as a hybrid analog/digital system in order to leverage the advantages of each; these are most easily seen in the n^{th} downconversion chain's feedback path. The DLL-HPC provides the option to choose between controlling the phase of the $LO_{rx,n}$ signal manually through a digital-analog converter or through the feedback provided by the phase detector. By controlling this phase manually, the DLL-HPC functions as a traditional active beamformer when the intermediate frequency (IF) components are summed. By allowing the phase detector's output to control the phase delay, the DLL-HPC functions as a delay-locked loop (DLL) beamformer when the IF components are summed, leveraging a DLL's fast settling time and unconditional stability

[19] [20] [21].

In order for the DLL-HPC to function as a phase conjugator, the microcontroller present in the downconversion chain's feedback path controls the generated carrier signal's phase through $DAC_{n,2}$. Additionally, all downconversion and carrier generation chains must be frequency synchronized; this can be achieved by using a common reference signal for all local oscillators (LO). With all signal chains frequency synchronized, the phases and frequencies relative to the 0th, or reference, downconversion chain can be defined as shown in Table 1.

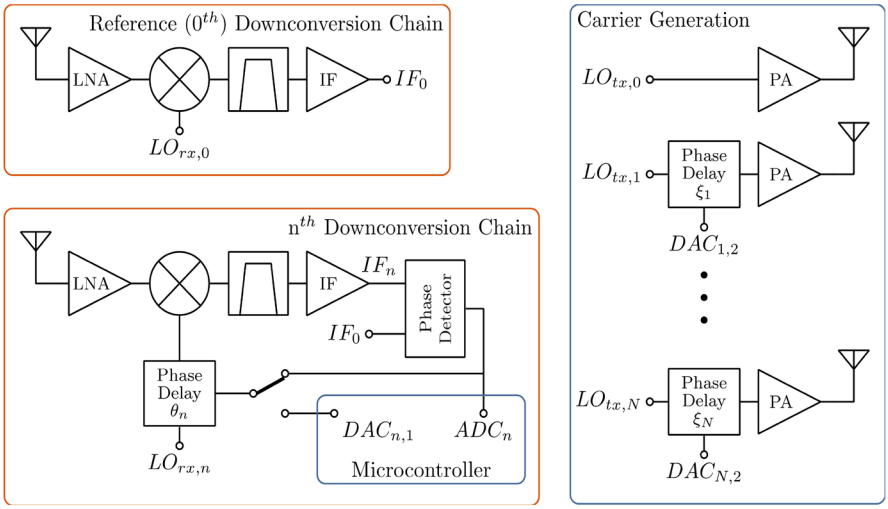

Figure 1. Delay-locked loop based hybrid phase conjugator (DLL-HPC) system diagram with isolated downconversion and carrier generation portions connected through a simple microcontroller.

Table 1. Frequency and phase definitions for the DLL-HPC.

Signal Name	*Element*	*Frequency*	*Phase*
Received Carrier (*RX*)	0^{th}	$f_{rx,0}$	$\phi_{rx,0}$
	n^{th}	$f_{rx,n}$	$\phi_{rx,n}$
Downconversion Local Oscillaator (LO_{rx})	0^{th}	$f_{lo,0}$	$\phi_{lo,0}$
	n^{th}	$f_{lo,n}$	$\phi_{lo,n}$
Intermediate Frequency (*IF*)	0^{th}	$f_{if,0}$	$\phi_{if,0}$
	n^{th}	$f_{if,n}$	$\phi_{if,n}$
Generation Local Oscillator (LO_{tx})	0^{th}	$f_{lo2,0}$	$\phi_{lo2,0}$
	n^{th}	$f_{lo2,n}$	$\phi_{lo2,n}$
Transmitted Carrier (*TX*)	0^{th}	$f_{tx,0}$	$\phi_{lo2,0}$
	n^{th}	$f_{tx,n}$	$\phi_{lo2,n}$
Downconversion Phase Delay (θ)	0^{th}		0°
	n^{th}		θ_n
Generated Carrier Phase Delay (ξ)	0^{th}		0°
	n^{th}		ξ_n

2.1. Received Signal Beamforming

By using a high-side LO and an appropriately designed IF filter and amplifier, the IF signal frequency will be:

$$f_{if} = f_{lo} - f_{rx} \tag{1}$$

So that:

$$\phi_{if} = (\phi_{lo} + \theta) - \phi_{rx} \tag{2}$$

From Equation (2), the phase difference between the n[th] and reference IF signals can be written as:

$$(\phi_{if,n} - \phi_{if,0}) = (\phi_{lo,n} - \phi_{lo,0}) + (\theta_n - \theta_0) - (\phi_{rx,n} - \phi_{rx,0}) \tag{3}$$

0˚ can be substituted for θ_0 because the reference downconversion chain contains no controllable phase delay element, and the ϕ_{lo} terms can be removed in favor of a Δi term. This new term encompasses any phase differences between the IF signals that are a product of the physical system: such as signal routing and the phase difference between the various LOs. Because all downconversion and carrier generation chains are frequency synchronized, this Δi term is a constant that depends only on the physical system. The final equation for the phase difference between the n^{th} and reference IF signals is now:

$$\Delta\phi_{if,n} = \theta_n - \Delta\phi_{rx,n} + \Delta i_n \tag{4}$$

In steady-state operation the DLL will drive the downconversion chain phase delay θ_n so that the IF signals will be in phase, or $\theta_n = \Delta\phi_{rx,n} - \Delta i_n$ [20]. In this state the IF signals can be summed to provide maximal beamforming gain [22]. Alternatively, θ_n can be controlled directly using $DAC_{n,1}$ to allow traditional active beamforming techniques to be used. As the Δi_n term is a constant, it can be calibrated out by a fixed offset when performing active beamforming.

2.2. Transmitted Signal Beamforming

By using frequency synchronized LO sources for the transmitted carrier signal generation chains, it can be seen from **Figure 1** that:

$$f_{tx} = f_{lo2} \tag{5}$$

And further:

$$\phi_{tx} = \phi_{lo2} + \xi \tag{6}$$

A similar approach to defining the phase difference between IF signals can be adopted for the phase difference between the n^{th} and reference generated carrier signals. Frequency synchronization allows a Δj term to be defined that encompasses the constant phase differences caused by the LOs and signal routing to arrive at:

$$\Delta\phi_{tx,n} = \xi_n + \Delta j_n \tag{7}$$

Because the Δj_n term is constant and depends only on the physical system, it can be calibrated out with a fixed offset stored in the microcontroller's memory.

This shows that active beamforming of the transmitted signal can be performed by applying arbitrary phase shifts to the n^{th} carrier frequency generation chain through $DAC_{n,2}$.

2.3. Phase Conjugation

The criteria for phase conjugation of a received signal states that the transmitted signal's phase must be the negative of the received signal's phase, or $\Delta\phi_{tx} = -\Delta\phi_{rx}$. Phase conjugation allows RDAs to transmit a signal back along the received DoA without *a priori* knowledge [14] [15] [18].

The DLL-HPC achieves quick phase conjugation through the use of look-up tables (LUTs) and well-characterized phase delay blocks. By monitoring the down-conversion chain's phase delay control signal while the DLL-HPC is in steady-state, a LUT can be used to determine what the current value of θ_n is at that given time. With this knowledge, it is a simple matter to set $\xi_n = -\theta_n$ through a second LUT to achieve phase conjugation. As the settling time of a DLL is extremely fast, the limiting factor of the speed of the DLL-HPC is the sampling rate of the microcontroller's analog-digital and digital-analog converters [21].

In order to remove the Δi_n and Δj_n terms in Equation (4) and Equation (7), a simple calibration procedure can be performed. In-phase signals can be applied to the DLL-HPC receiver so that $\Delta\phi_{rx,n} = 0^\circ$ and steady-state lock occurs at $\theta_n = -\Delta i_n$. This value of θ_n can be recorded as a constant offset to compensate for the Δi_n term. Likewise, the Δj_n term can be found by setting $\xi_n = 0^\circ$ so that $\Delta\phi_{tx,n} = \Delta j_n$. $\Delta\phi_{tx,n}$ can then be measured directly to find and compensate for Δj_n. This calibration procedure only needs to be performed a single time for each DLL-HPC, as both Δi_n and Δj_n are constants determined by the physical system.

Implementing the digital portion of the DLL-HPC requires only one analog-digital converter (ADC), two digital-analog converters (DACs), and two LUTs providing mappings for choosing θ_n and ξ_n values. A measured phase delay control voltage for θ_n can be used to directly calculate $\Delta\phi_{RX,n}$ through a LUT if Δi_n is known. Once $\Delta\phi_{RX,n}$ is known, it can be used to directly set $\Delta\phi_{TX,n}$ to $-\Delta\phi_{RX,n}$ through a LUT. This phase conjugation implementation requires far fewer resources than all-digital RDA solutions or most active beamforming techniques [1] [23].

3. DLL-HPC Unique Capabilities

The DLL-HPC maintains the core advantages of a traditional RDA, namely the ability to track moving targets and accurately transmit back along the DoA of a received signal in dynamic environments [15] [17]. Additionally, the presence of a digital control element in the DLL-HPC allows for the following extra functionalities:

3.1. Backwards Compatibility with Beamforming Protocols

The DLL-HPC's separation of downconversion and carrier signal generation

chains and ability to be reconfigured as an actively steered phase shifter allow for backwards compatibility with previous beamforming protocols, such as those outlined in IEEE 802.11 ad/ay [1].

3.2. Direction of Arrival Reporting

Phase-locked loop and mixer-based RDAs have no way of reporting the phase of the received carrier signal [15] [24]. Because the DLL-HPC's digital control element measures and conjugates the received signal phase directly, it is also able to record and report the received signal phase with little overhead. If the array geometry is known, this allows for real-time DoA monitoring and system environment analysis. If this information is shared among members of a network, a Spatial Division Multiple Access (SDMA) scheme can be used to allow for context-aware reuse of frequency bands as illustrated in **Figure 2**.

3.3. Received Signal Dropout Immunity

The DLL-HPC's ability to track and store the DoA of a received carrier signal can be used to prevent system decoherence in the case of received signal dropout. When no received signal is present the DLL-HPC is capable of choosing values for both θ_n and ξ_n based on their previous values by actively controlling each phase delay element. Furthermore, the DLL-HPC is capable of predictively tracking targets by monitoring the DoA over time. Simple digital operations can be used to maintain a continuously updated record of the DoA and its rate of change to provide predictive tracking during momentary dropouts. These capabilities lend themselves well to the dynamic environments of mmWave 5G systems and time-division duplex (TDD) applications [6] [11].

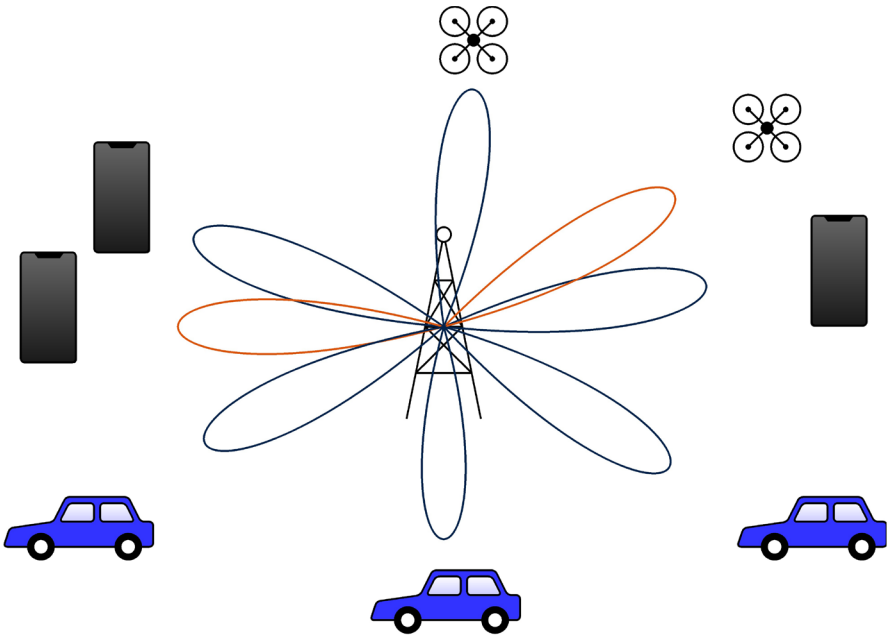

Figure 2. A spatial division multiple access (SDMA) scheme reusing two carrier frequencies, shown in orange and blue, based on user locations.

3.4. Initial Acquisition Scheme

The proposed DLL-HPC architecture would enable a new suite of beamforming techniques if adopted in a large-scale communication system. The greatest performance improvement would be seen in acquiring and maintaining beamformer patterns over the current standards [1]. Instead of reducing system throughput by continually reevaluating and retransmitting beamformer training information [1] [3], a point between two transceivers could be established quickly and with no continual communications overhead.

A possible methodology involves two transceivers switching between actively controlled and retrodirective modes as illustrated in Figure 3. Alternatively, a low-power beacon signal could be transmitted from base stations to allow users to automatically identify the DoA and beamform accordingly.

4. Experimental Results

In order to verify the operation and versatility of the proposed DLL-HPC system architecture, a proof-of-concept prototype was fabricated using only commercially available off-the-shelf components to operate at 5G NR-FR1 frequencies from 2.100 GHz to 2.600 GHz. The fabricated prototype operates with an IF frequency of 10 MHz and is capable of performing phase conjugation and beamforming of any combination of receive/transmit carrier frequencies within

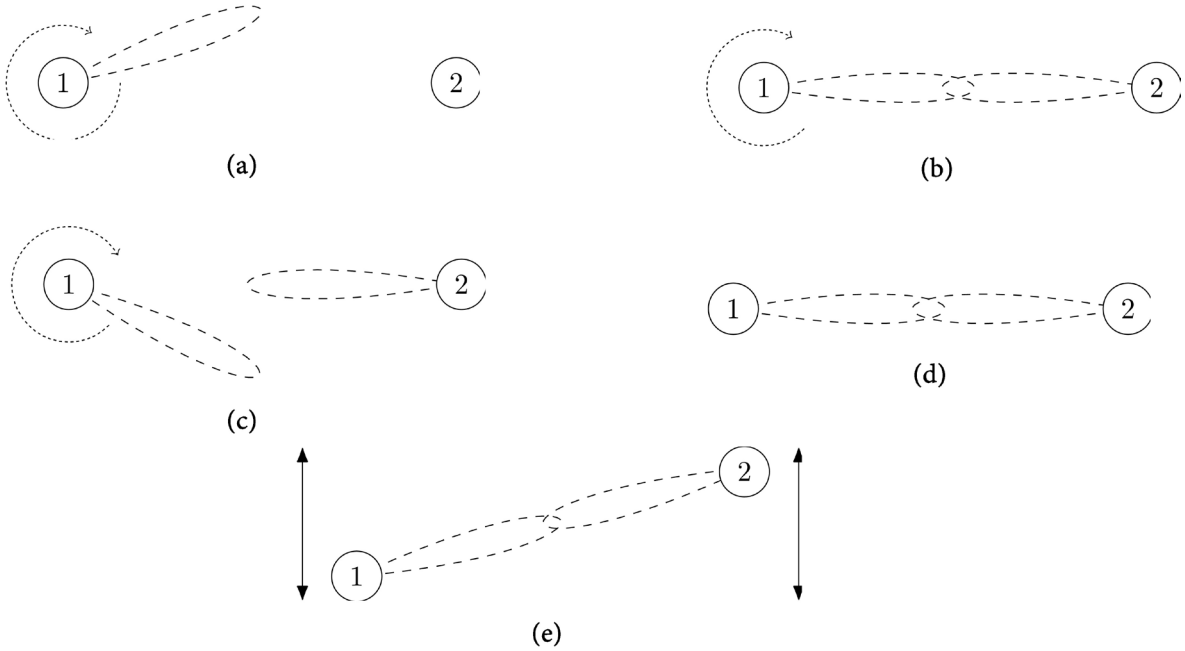

Figure 3. DLL-HPC beamforming strategy: (a) Transceiver 1 performs a field-of-view sweep while Transceiver 2 listens in closed-loop retrodirection mode. (b) Transceiver 2 locks onto the DoA of Transceiver 1's signal through phase conjugation. (c) Transceiver 2 maintains its point through active beamforming while Transceiver 1 finishes its field-of-view sweep. (d) Transceiver 1 switches to closed-loop retrodirection mode to establish a point towards Transceiver 2, which switches back to closed-loop retrodirection mode to maintain the point. (e) Transceivers 1 and 2 maintain an optimal beamforming point regardless of each transceiver's motion in closed-loop retrodirection mode operation.

the 5G NR-FR1 band. A phase-frequency detector (PFD) and charge pump were chosen as feedback in the DLL portion of the design due to their fast settling times and 0˚ steady-state error. Measurements were made using a Tektronix MSO64 oscilloscope, and a Keysight M8196A Arbitrary Waveform Generator (AWG) was used to generate phase-shifted sources for testing. The fabricated prototype system consumed 2.42 W of power in steady-state operation. Components used in the prototype design are listed in Table 2.

4.1. Phase Conjugation

Phase conjugation was verified by operating the DLL-HPC prototype according to the outlined algorithms and applying a known phase difference ($\Delta\phi_{RX}$) between the RX_1 and RX_0 inputs while measuring the steady-state phase difference ($\Delta\phi_{TX}$) between the TX_1 and TX_0 outputs. Both receive and transmit frequencies were set to 2.400 GHz. Figure 4 shows both the measured conjugated carrier signal phase and error magnitude versus the received signal phase alongside a plot of an ideal phase conjugator's output, where $\Delta\phi_{TX} = -\Delta\phi_{RX}$. Between one thousand and three thousand samples were taken and averaged for each data

Table 2. Components used in the DLL-HPC prototype.

System Component	*Commercial Part*
Local Oscillator	LTC6946-4 Phase Locked Loop
Mixer	LTC5562 Active Mixer
Phase Detector	ADF4002 Phase-Frequency Detector
RF Amplifier	PMA3-83LN+ Low-Noise Amplifier
IF Amplifier	LTC6253 Operational Amplifier
Microcontroller	TM4C1294NCPDT Microcontroller
Digital-Analog Converter	MCP4725 12-bit DAC
Analog-Digital Converter	Built-in to Microcontroller

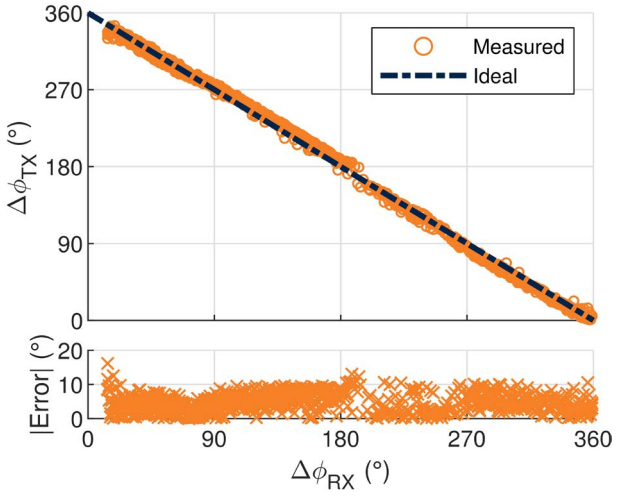

Figure 4. DLL-HPC prototype measured phase conjugation and error magnitude.

point presented to find the steady-state phase of the received and transmitted signals. The average standard deviation of these samples was 2.25˚, demonstrating the stability of the DLL-HPC in operation. The average error magnitude across all samples was found to be 4.65˚, with a worst-case error of 16.17˚. These phase conjugation measurements indicate that retrodirection could be performed on a multi-element array with comparable accuracy to a 5-bit digital beamformer with a resolution of 11.25˚.

4.2. Active Steering

Active steering capabilities were verified by measuring the generated carrier signal phase difference and comparing it to the chosen value at a frequency of 2.400 GHz. The average error magnitude was calculated to be 6.0˚, with an average error of +0.1˚. Further, the same performance can be expected for any carrier frequency, as the phase shifter was implemented and characterized on the LO oscillator reference signal. A small, well-characterized phase shifter was constructed to provide up to 17˚ of phase shift on a 100 MHz reference signal, which is then multiplied by 24 at the LO's 2400 MHz output to provide a controllable 408˚ phase shift. The LUT used to control this phase shifter can therefore be used to accurately control the phase at other generated frequencies by modifying the scalar factor applied by the LO. This allows for arbitrary selection of the generated carrier signal frequency.

4.3. Direction of Arrival Reporting

DoA reporting capabilities were verified by recording the DLL-HPC's reported received signal phase and comparing it to the actual phase generated by the AWG. The DLL-HPC prototype was able to report the received signal phase with an average error magnitude of 2.59˚ and an average error of +1.0˚. As this proof-of-concept prototype consisted of only a single DLL-HPC, no array-level DoA calculations can be shown at this time.

4.4. Settling Time and Dynamic Phase Tracking

The settling time of the DLL-HPC was found by recording the control signals for each phase delay block when a step change occurred in the received signal phase. The downconversion chain settled in 0.95 ms on average, while the carrier generation chain settled in 10.35 ms on average. The difference in settling times can be attributed to the selected components: the sampling rate for the ADCs and DACs used was set to 100 Hz, which causes the carrier generation chain to settle around one sample (10 ms) later than the downconversion chain. Likewise, the closed-loop design of the phase detector and loop filter in the DLL determined the downconversion chain settling time. Additionally, these tests verify the DLL-HPC's ability to track mobile targets. During the settling time tests the received signal phase step size was varied from 15˚ to 90˚ and swept through multiple full 360˚ rotations. The settling times across step sizes were found to be the

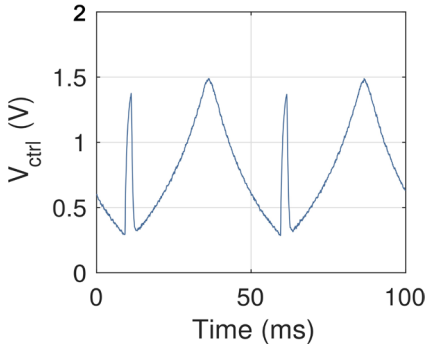

Figure 5. Measured DLL-HPC closed-loop control voltage for input phase difference varying at 15,000˚/s.

same, indicating a DLL-HPC will accurately track mobile targets of varying speeds.

In order to further verify the ability of the DLL-HPC to actively track mobile targets, the relative phase difference of the received signal was swept linearly from 0˚ to 360˚ to 0˚ in a cycle with various rates of change from 50˚/s to 15,000˚/s. In each test, the DLL-HPC's closed-loop received signal chain was able to accurately track the changing phase as shown in Figure 5. The transmitted signal beamformer portion of the DLL-HPC was not characterized in these tests, its settling time is limited by the ADC and DAC sampling rates of the prototype; however, sufficiently high sampling rates will allow the same transmitted signal beamformer tracking rates.

5. Conclusions

A novel DLL-based Hybrid Phase Conjugator architecture has been proposed alongside experimental verification. The proposed DLL-HPC has been shown to be capable of performing phase conjugation with small errors and rapid settling times. This system provides a unique combination of features that no other RDA or beamforming circuit/protocol is able to duplicate: retrodirection capability, active steering capability, rapid settling time, small phase errors, received signal dropout immunity, DoA reporting, automatic mobile target tracking, and backwards compatibility with previous beamforming solutions. See sources [14] [17] [18] [21] [24] for comparable phase conjugator implementations and sources [1] [4] [6] [10] [19] [21] [25] for information on current beamforming protocols, circuits, and techniques and their various shortcomings. This work serves as a step towards a mmWave 5G beamforming solution over the current circuits and techniques.

The characterization and simulation of DLL-HPC based antenna arrays in environments characteristic of mmWave 5G applications is currently underway, and results will be reported in a timely manner.

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Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

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