Scientific Research Publishing

Advances in Materials Physics and Chemistry, 2023, 13, 121-134
https://www.scirp.org/journal/ampc
ISSN Online: 2162-5328
ISSN Print: 2162-531X

Simulation Study of 50 nm Gate Length MOSFET Characteristics

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How to cite this paper: Chowdhury, T.A. (2023) Simulation Study of 50 nm Gate Length MOSFET Characteristics. *Advances in Materials Physics and Chemistry*, **13**, 121-134.
https://doi.org/10.4236/ampc.2023.136009

Received: May 6, 2023
Accepted: June 25, 2023
Published: June 28, 2023

Abstract

With the need to improvement of speed of operation and the demand of low power MOSFET size scales down, in this paper, a 50 nm gate length n-type doped channel MOS (NMOS) is simulated using ATLAS packages of Silvaco TCAD Tool so as to observe various electrical parameters at this gate length. The parameters under investigation are the threshold voltage, subthreshold slope, on-state current, leakage current and drain induced barrier lowering (DIBL) by varying channel doping concentration, drain and source doping concentration and gate oxide thickness.

Keywords

MOSFET, Threshold Voltage, Subthreshold Slope, Leakage Current, TCAD

1. Introduction

Enormous research work has been done in semiconductor industry for the accommodation of more complex circuits on a single semiconductor substrate. To accomplish this purpose the feasible method is device scaling [1]. There is continual scaling down of MOSFET size [2]. The drastic reduction of dimension will not always meet with device performances and creates problems that are yet to be solved.

Various investigations have been carried out to overcome every barrier to meet Moore's Law [3]. All the challenges have been surpassed by developing smaller and energy efficient devices with reliable function. New technologies developed, like complementary metal oxide semiconductor transistors (CMOS), which result in exponential development in both device performance and density. However, this classical shrinking down of MOSFET device dimension had been successful until 100 nm CMOS transistor. After that the effects get worse

due to the non-linearity of the physicals and electrical characteristics of the materials in the device at nanoscale [4] [5]. New phenomena such as short-channel-effects (SCEs) appear in low dimensions devices due to device size reduction. The significance to have a solid knowledge of the phenomena that appear in nanoscale MOSFETs is high because it provides us the understanding to control the SCEs and the restrictions of the device scaling.

The "constant-field scaling", that refers to that in the scaled transistor all electric fields remain the same, is a necessary condition for the successful geometric scaling of MOSFETs. Due to Robert Dennard's ideal scaling principles, with the increased doping concentration in the channel region by a factor, the device dimensions width (W), length (L), gate-oxide thickness (tox) and voltages VDD and threshold voltage (V_{th}) will be scaled down by the same factor a [6]. This way while maintaining the device reliability a higher circuit performance can be achieved. But for nanoscale devices, new problems arise that limit the size reduction. The challenges that occur in nanoscale transistors can be classified on where the issue arises. The channel region is the area where most phenomena occur. These phenomena result in increase in the subthreshold leakage currents, alter the threshold voltage and are a consequence of the interaction of drain and source regions.

As the channel length shrinks down, the drain depletion region starts to interact with the source and channel regions, decreasing the potential barrier between the source and the drain. As a result, the gate voltage is unable to control the drain current for values less than the threshold voltage. This results in a phenomenon known as drain induced barrier lowering (DIBL) effect. If the depletion region around the drain continues to lengthen to the source depletion region with the further increasing drain voltage, the drain current increases from the presence of a parasitic current path located below the gate. This phenomenon is called punch-through and adds to the subthreshold leakage current. To prevent these effects, an increase in the substrate doping concentration may be helpful to reduce drain/source depletion regions. However, in nanoscale devices, high doping concentration introduces new issues that limit size reduction [7].

The carrier mobility degradation is an issue resulting from high doping concentration. It occurs in the channel region and the drift velocity of the carriers is proportional to the electric fields. The increasing rate of carriers velocity decreases as the electrical fields across the channel keep increasing. The carriers reach their maximum velocity for specific values for the electrical field. The carrier mobility degradation is also called velocity saturation, and it originates from elastic scattering processes including phonon dispersion, acoustic phonon scattering and ionized impurity scattering [8].

Furthermore, the high electric fields could provide high kinetic energy to the carriers, sufficient to overcome barriers and penetrate in undesired areas such as the substrate and the gate dielectric. The continuous downscaling of device also impacts the gate region of a transistor resulting in gate leakage currents due to quantum mechanical tunneling. The gate oxide thickness reduces to control the

channel, but the very thin oxide increases phenomena like electrons direct tunneling. To increase transistor performance while also reducing gate leakage currents gate dielectrics with high permittivity (high-k) replaced the silicon dioxide (SiO_2) recently. This paper presents the impact of varying channel doping concentration, drain and source doping concentration and gate oxide thickness on MOS device electrical characteristics such as threshold voltage (V_{th}), subthreshold slope, on-state current (Ion), leakage current (I_{off}) and drain induced barrier lowering (DIBL). TCAD Silvaco software is used for simulation study of MOS device structure.

2. Methodology

To study the electrical parameters on n-type doped channel MOS (NMOS) a schematic cross-sectional view of the MOSFET is simulated using Silvaco TCAD device simulator, is shown in Figure 1. We assumed light channel doping concentration (5×10^{18} cm^{-3}) to avoid degrading of carrier mobility and more V_{th} variations. The doping concentration of source/drain region is kept at 1×10^{20} cm^{-3}. Gate length of the device that had been concentrated is 50 nm. Gate oxide (SiO_2) thickness is 1.2 nm. The total device length including drain, channel and source is 150 nm. Shockley-Read-Hall recombination, Lombardi CVT mobility model and impact ionization model from Selberherr [9] are used for the simulation. Numeric methods used for simulation are Newton methods. We assumed n-channel MOS (NMOS) device and simulated the device for different channel doping concentration, drain and source doping concentration and gate oxide thickness of MOSFET.

3. Results and Discussion

The simulation and investigation of electrical parameters of MOS has been carried out by using Silvaco TCAD simulation software. The MOS structure is created using Atlas syntax and the simulation results are displayed in TonyPlot. In this study, n-channel MOSFET structure has been designed and simulated

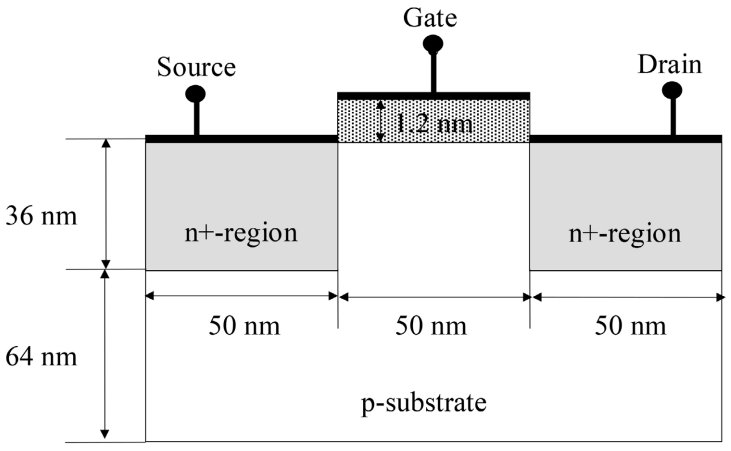

Figure 1. Schematic view of NMOS.

using DeckBuild. The simulation result of the MOSFET device structure is displayed in TonyPlot and this device has a gate length of 50 nm. The thickness of different material is defined when specifying the structure region. The simulated device structure is shown in Figure 2.

By changing the channel doping concentration, the electrical parameters of MOSFET are recorded as shown in Table 1. The results in Table 1 are analysed and graph of electrical characteristics versus channel doping concentration are plotted.

Figure 3 shows the Ids/Vgs characteristics of NMOS at various channel doping concentration.

By varying the channel doping concentration, the result of threshold voltage has been recorded and the graph of threshold voltage versus channel doping concentration is plotted and shown in Figure 4. From Figure 4, it can be said that the lower the channel doping concentration, the lower the threshold voltage. High performance device requires smaller value of threshold voltage [10].

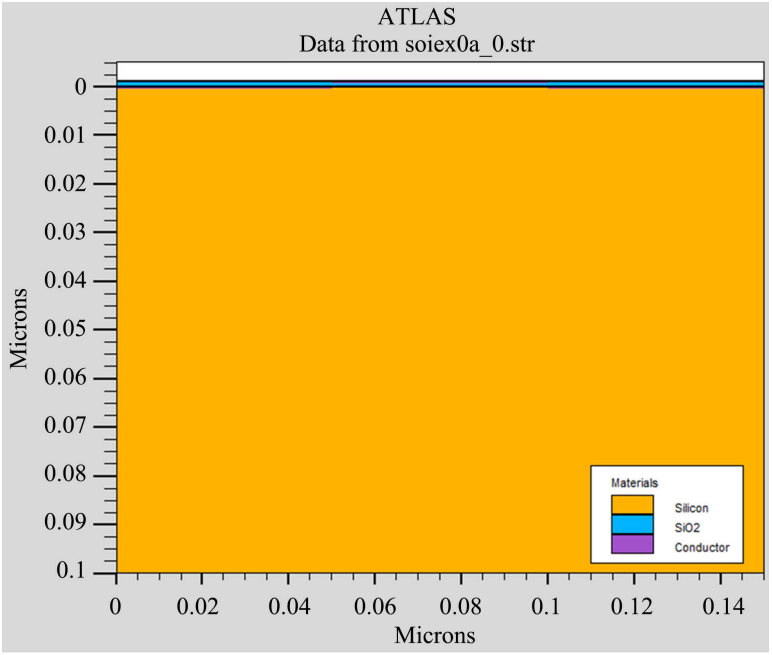

Figure 2. Simulated structure of NMOS.

Table 1. Electrical characteristics of NMOS at different channel doping concentration with the doping concentration of the source and drain regions is 10^{20} cm^{-3}.

Channel doping concentration (cm^{-3})	Threshold voltage, V_{th} (V)	Subthreshold slope (mV/dec)	On-state current, I_{on} (μA)	Leakage current, I_{off} (nA)	DIBL (mV/V)
4×10^{18}	0.27920	74.99	1006.10	27.11	53.14
5×10^{18}	0.33957	75.64	805.71	17.76	38.22
7×10^{18}	0.43427	78.47	510.87	0.03	29.42
1×10^{19}	0.58734	82.44	242.26	0.72	30.41

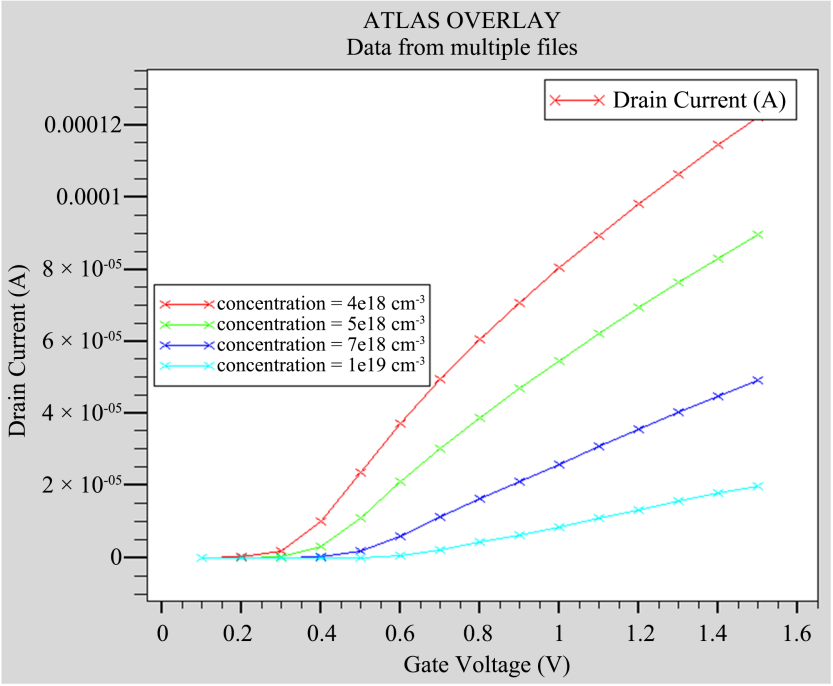

Figure 3. Ids/Vgs characteristics of NMOS at various channel doping concentration.

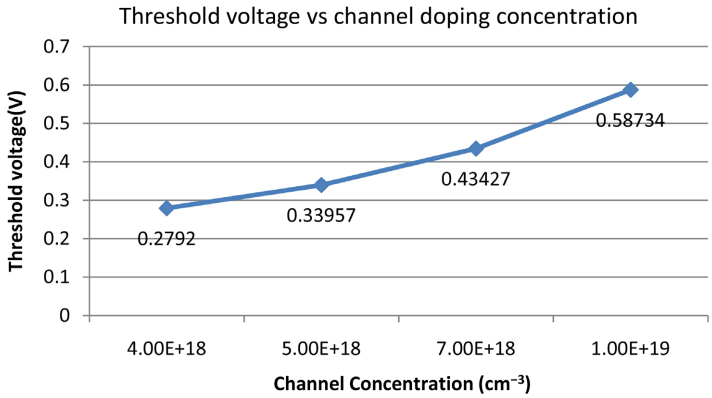

Figure 4. Graph of threshold voltage versus channel doping concentration.

Subthreshold slope is a measure of how quickly the transistor can be turned on/off. The smaller subthreshold value indicates the device rapidly switches from off to on state. The graph of subthreshold slope versus channel doping concentration is shown **Figure 5**. As channel doping concentration decreases, the steeper subthreshold slope becomes as from **Figure 5** which strongly increases the device speed. The reason of fast operation is because of a sharper sub-threshold slope and threshold voltage reduction which allows a more rapidly switching of MOSFET [11].

A high on-state current (I_{on}) helps to increase the operating speed of the device. The graph I_{on} versus channel doping concentration is shown in **Figure 6**. From **Figure 6**, it can be said that the lower the channel doping concentration, the higher the on-state current.

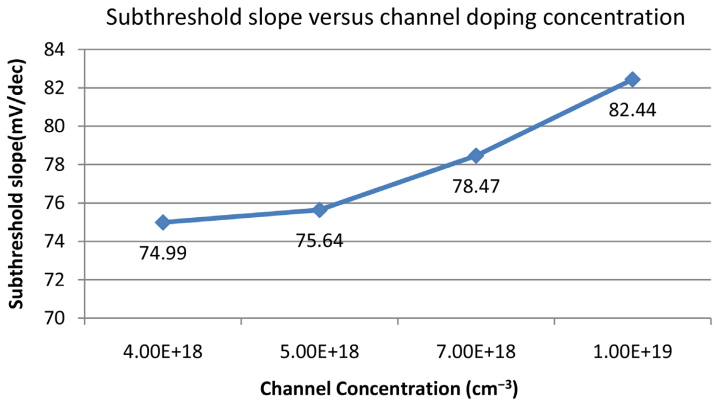

Figure 5. Graph of sub threshold slope versus channel doping concentration.

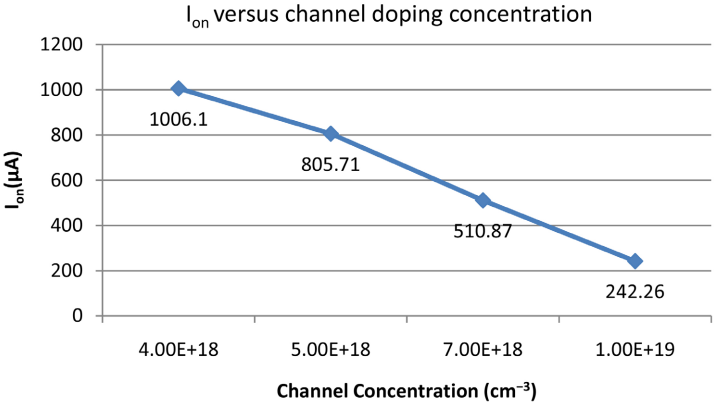

Figure 6. Graph of I_{on} versus channel doping concentration.

The result of leakage current (I_{off}) is inversely proportional to the threshold voltage [12]. This means that value of leakage current becomes smaller with the increasing of threshold voltage. The higher the threshold voltage, the smaller the leakage current. MOSFET device will fail when excessive leakage current occurs. Large leakage current of conventional semiconductor is caused by the electron-hole pair generation due to ionizing radiations. The graph of leakage current versus channel doping concentration is shown in **Figure 7**. Leakage current contributes to static power dissipation and leakage power dissipation is caused by current flow when input transition is absent and transistor achieved steady state [13]. Thus, by having a smaller leakage current, static power dissipation will be less. Thus, from the result of **Figure 7** the MOSFET will have a lower static power dissipation when channel doping concentration is increased.

Drain induced barrier lowering is a measure for short channel effects. The graph of drain induced barrier lowering (DIBL) versus channel doping concentration is shown in **Figure 8**. As channel doping concentration increases from 4e18 cm^{-3} upto 7e18 cm^{-3}, the DIBL value decreases from 53.14 mV/V to 29.42 mV/v which improves short channel effects. As channel doping concentration to 1e19 cm^{-3} DIBL value degrades slightly. Therefore MOSFET with channel doping concentration of 7e18 cm^{-3} has the best DIBL parameter value which

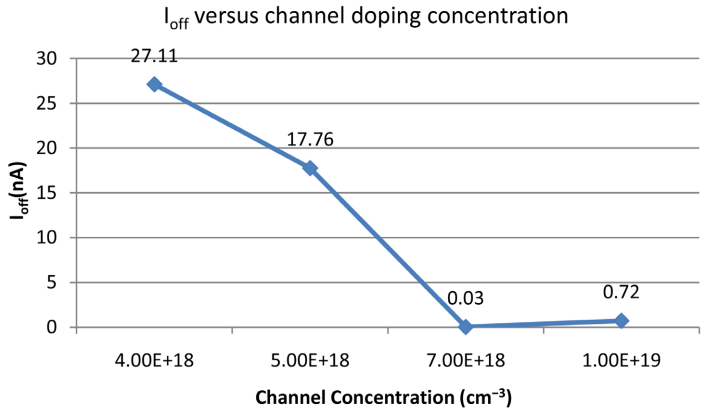

Figure 7. Graph of I_{off} versus channel doping concentration.

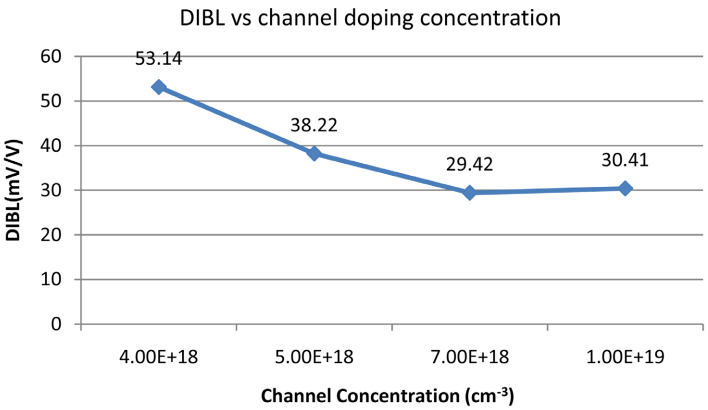

Figure 8. Graph of DIBL versus channel doping concentration.

makes it less sensitive to short channel effects. Therefore, the impact of drain voltage on the device threshold voltage reduces.

By changing the drain and source doping concentration, the electrical parameters of MOSFET are recorded as shown in Table 2. The results in Table 2 are analysed and graph of electrical characteristics versus drain/source doping concentration are plotted.

Figure 9 shows the Ids/Vgs characteristics of NMOS at various source/drain doping concentration.

By varying the drain and source doping concentration, the result of threshold voltage has been recorded and the graph of threshold voltage versus drain and source doping concentration is plotted and shown in Figure 10. From Figure 10, it can be said that the lower the drain and source doping concentration, the lower the threshold voltage.

The graph of subthreshold slope versus source/drain doping concentration is shown Figure 11. As source/drain doping concentration increases, the steeper subthreshold slope becomes as from Figure 11 which strongly increases the device speed. In Figure 11 standard error of the mean (SEM) error bars are used as source/drain doping concentration increases above 10^{20} cm^{-3}, subthreshold slope value saturates at around 75.5 mV/dec.

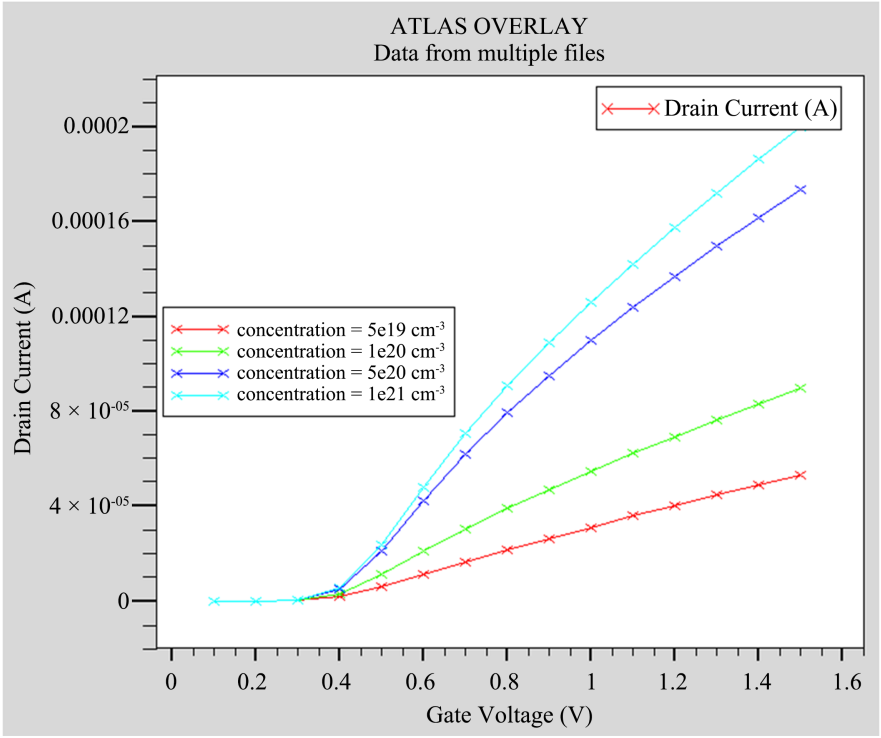

Figure 9. Ids/Vgs characteristics of NMOS at various drain/source doping concentration.

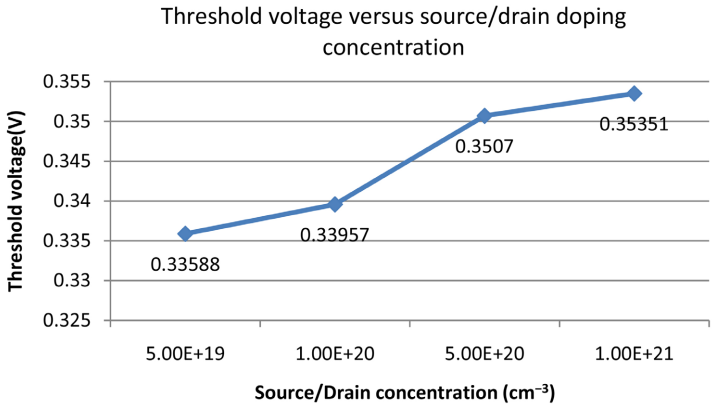

Figure 10. Graph of threshold voltage versus source/drain doping concentration.

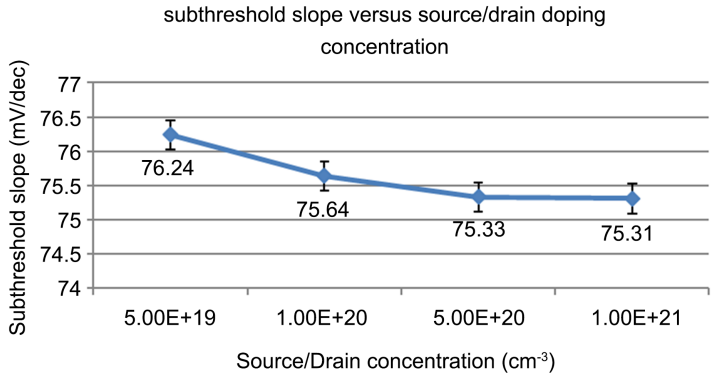

Figure 11. Graph of subthreshold slope versus source/drain doping concentration.

The graph of I_{on} versus source/drain doping concentration is shown in Figure 12. From Figure 12, it can be said that the higher the source/drain doping concentration, the higher the on-state current.

The graph of leakage current (I_{off}) versus source/drain doping concentration is shown in Figure 13. From Figure 13, it can be said that the higher the source/drain doping concentration, the higher the leakage current.

Table 2. Electrical characteristics of NMOS at different drain/source doping concentration with the doping of the channel is 5×10^{18} cm^{-3}.

Source/Drain doping concentration (cm^{-3})	Threshold voltage, V_{th} (V)	Subthreshold slope (mV/dec)	On-state current, I_{on} (μA)	Leakage current, I_{off} (pA)	DIBL (mV/V)
5×10^{19}	0.33588	76.24	0.66	1103.76	35.78
10^{20}	0.33957	75.64	0.81	1776.31	38.22
5×10^{20}	0.35070	75.33	1.05	3145.85	39.23
10^{21}	0.35351	75.31	1.13	3518.49	39.26

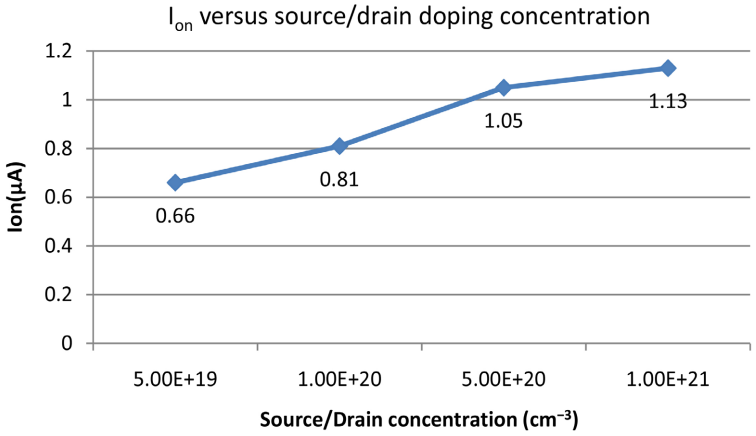

Figure 12. Graph of I_{on} versus source/drain doping concentration.

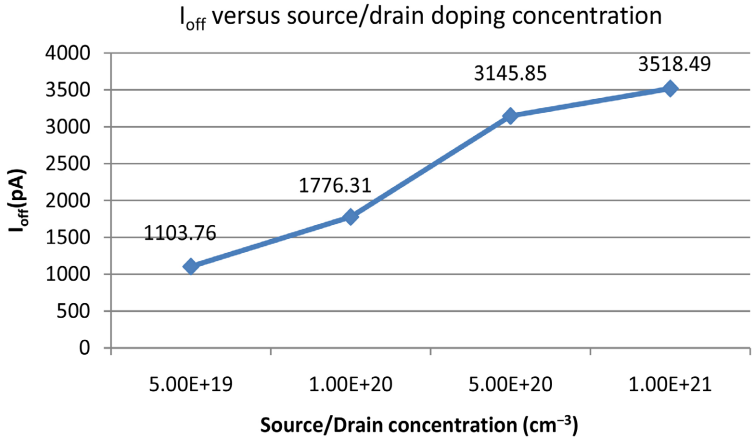

Figure 13. Graph of I_{off} versus source/drain doping concentration.

The graph of drain induced barrier lowering (DIBL) versus source/drain doping concentration is shown in Figure 14. From Figure 14 the lower source/drain doping concentration, the lower the DIBL. Therefore, the impact of drain voltage on the device threshold voltage is lower.

By changing the gate oxide thickness (T_{ox}), the electrical parameters of MOSFET are recorded as shown in Table 3. The results in Table 3 are analysed and graph of electrical characteristics versus gate oxide thickness are plotted.

Figure 15 shows the Ids/Vgs characteristics of NMOS at various gate oxide thickness.

By varying the gate oxide thickness, the result of threshold voltage has been recorded and the graph of threshold voltage versus gate oxide thickness is plotted and shown in Figure 16. From Figure 16, it can be said that the thinner the gate oxide thickness, the higher the gate oxide capacitance and consequently the lower the threshold voltage.

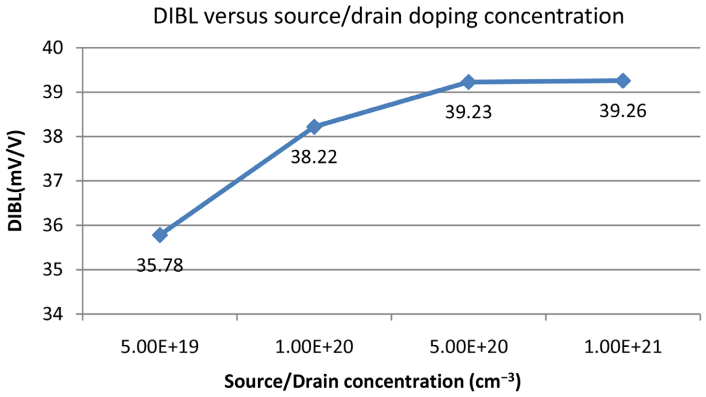

Figure 14. Graph of DIBL versus source/drain doping concentration.

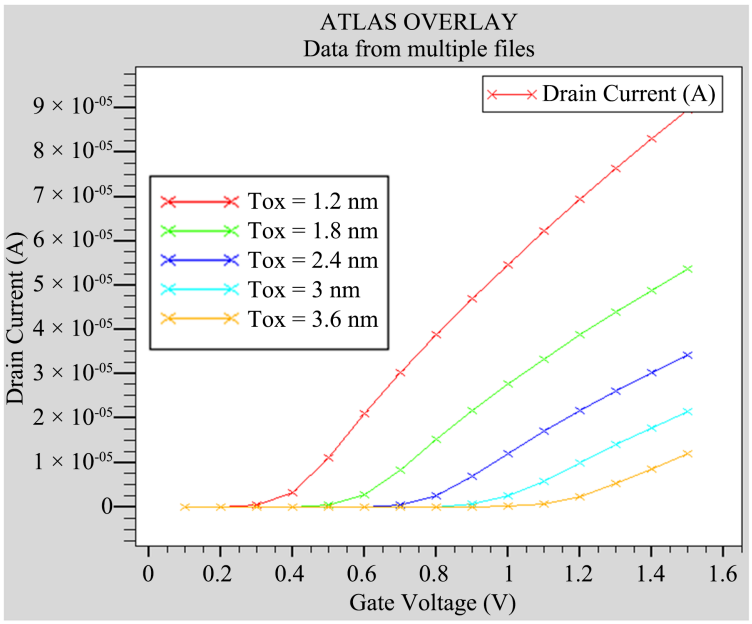

Figure 15. Ids/Vgs characteristics of NMOS at various gate oxide thickness.

The graph of subthreshold slope versus gate oxide thickness is shown Figure 17. As gate oxide thickness decreases, the steeper subthreshold slope becomes as from Figure 17 which strongly increases the device speed.

The graph I_{on} versus gate oxide thickness is shown in Figure 18. From Figure 18, it can be said that the thinner the gate oxide thickness, the higher the on-state current.

Table 3. Electrical characteristics of NMOS at different gate oxide thickness with channel doping is 5×10^{18} cm^{-3}, the doping of the source and drain regions is 10^{20} cm^{-3}.

Gate oxide thickness, T_{ox} (nm)	Threshold voltage, Vth (V)	Subthreshold slope (mV/dec)	On-state current, I_{on} (μA)	Leakage current, I_{off} (pA)	DIBL (mV/V)
1.2	0.33957	75.64	805.71	1776.31	38.22
1.8	0.52932	83.06	394.26	58.06	55.08
2.4	0.71897	90.40	187.41	3.81	71.47
3	0.90891	98.04	82.42	0.42	97.94
3.6	1.09925	106.03	31.93	0.07	120.30

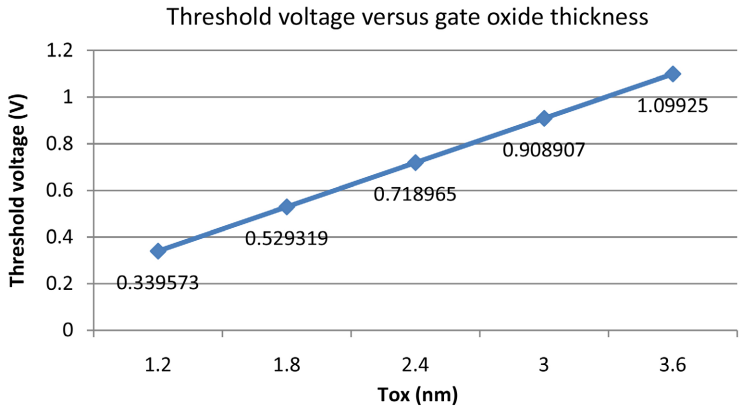

Figure 16. Graph of threshold voltage versus gate oxide thickness.

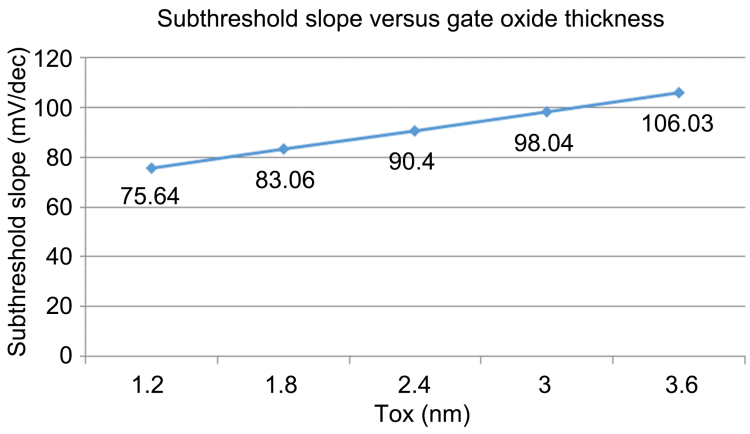

Figure 17. Graph of subthreshold slope versus gate oxide thickness.

The graph of leakage current (I_{off}) versus gate oxide thickness is shown in Figure 19. From Figure 19, it can be said that the higher the gate oxide thickness, the lower the leakage current.

The graph of drain induced barrier lowering (DIBL) versus gate oxide thickness is shown in Figure 20. From Figure 20, it is evident that as gate oxide thickness decreases, DIBL improves.

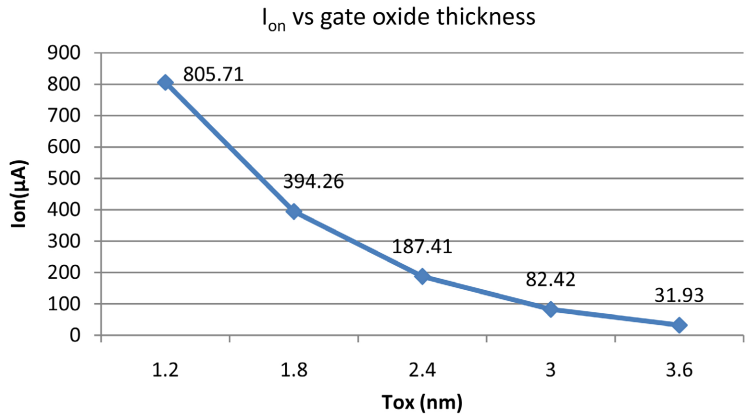

Figure 18. Graph of I_{on} versus gate oxide thickness.

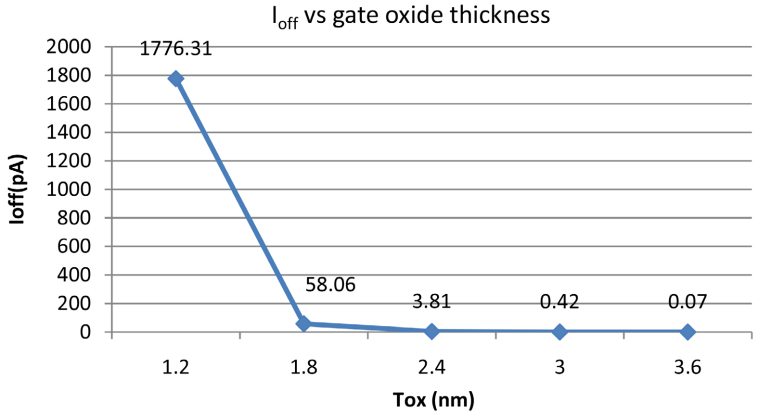

Figure 19. Graph of I_{off} versus gate oxide thickness.

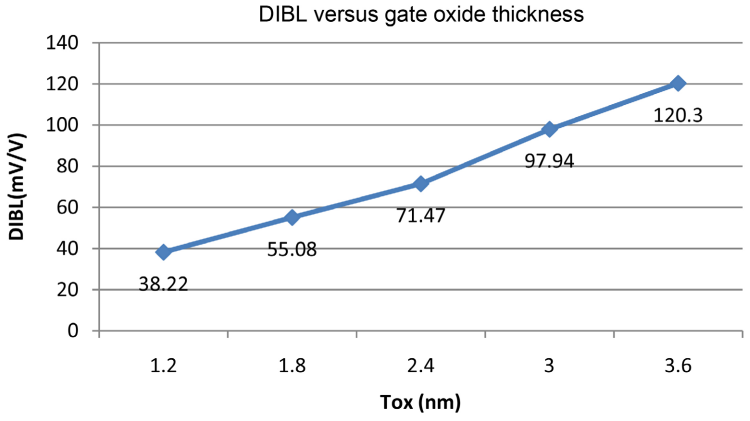

Figure 20. Graph of DIBL versus gate oxide thickness.

4. Conclusions

MOSFET has been investigated in terms of electrical characteristics using Silvaco TCAD simulator by varying channel doping concentration, drain and source doping concentration and gate oxide thickness. It is found that the thinner gate oxide thickness of 1.2 nm gives the best performance in terms of electrical parameter results. Although the leakage current increases, when the channel doping concentration is decreased while keeping the source, drain doping concentration and gate oxide thickness fixed, the threshold voltage decreases, subthreshold slope improves, on-state current increases, leakage current increases and DIBL degrades. When the source, drain doping concentration is increased while keeping the channel doping concentration and gate oxide thickness fixed, the threshold voltage increases, subthreshold slope improves, on-state current increases, leakage current increases and DIBL degrades.

So the doping concentration of channel, drain and source of MOSFET has to be chosen depending on application requirement.

Conflicts of Interest

The author declares that there is no conflict of interest.

References

[1] Rahou, F.Z., Guen-Bouazza, A. and Rahou, M. (2013) Electrical Characteristics Comparison between Fully-Depleted SOI MOSFET and Partially-Depleted SOI MOSFET Using Silvaco Software. *Global Journal of Researches in Engineering Electrical and Electronics Engineering*, **13**, 1-6.

[2] Husaini, Y., Ismail, M.H., Zoolfakar, A.S. and Khairudin, N. (2010) Electrical Characteristics Comparison between Partially-Depleted SOI and N-MOS Devices Investigation using Silvaco. 2010 *IEEE Symposium on Industrial Electronics and Applications*, Penang, 3-5 October 2005, 532-536. https://doi.org/10.1109/ISIEA.2010.5679408

[3] Bowden, M.J. (2004) Moore' s Law and the Technology S-Curve. SATM.

[4] Moore, G.E. (1965) Cramming More Components onto Integrated Circuits. *Electronics*, **38**, 114-117.

[5] Sze, S.M. (2008) Semiconductor Devices: Physics and Technology. 2nd Edition, Wiley-India.

[6] Bohr, M. (2007) A 30 Year Retrospective on Dennard's MOSFET Scaling Paper. *IEEE Solid-State Circuits* Society Newsletter, **12**, 11-13. https://doi.org/10.1109/N-SSC.2007.4785534

[7] Razavi, B. (2001) Design of Analog CMOS Integrated Circuits. McGraw-Hill, Boston, MA.

[8] Anderson, B.L and Anderson, R.L. (2005) Fundamentals of Semiconductor Devices. McGraw-Hill Higher Education, Boston.

[9] Silvaco International (2004) ATLAS User's Manual Device Simulation Software. Santa Clara, Calif.

[10] Verma, A., Mishra, A., Singh, A. and Agrawal, A. (2014) Effect of Threshold Voltage on Various CMOS Performance Parameter. *International Journal of Engineer-*

ing Research and Applications, **4**, 21-28.

[11] Vandana, B. (2013) Study of Floating Body Effect in SOI Technology. *International Journal of Modern Engineering Research*, **3**, 1817-1824.

[12] Cristoloveanu, S. and Li, S. (2014) Electrical Characterization of Silicon-on-Insulator Materials and Devices. Springer US.

[13] Singh, S.K., Kaushik, B.K., Chauhan, D.S. and Kumar, S. (2013) Reduction of Subthreshold Leakage Current in MOS. Transistors. *World Applied Sciences Journal*, **25**, 446-450.