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Effect of Defects at the Buffer Layer CdS/Absorber CIGS Interface on CIGS Solar Cell Performance

Boureima Traoré, Soumaïla Ouédraogo, Marcel Bawindsom Kébré, Daouda Oubda, Issiaka Sankara, Adama Zongo, François Zougmoré

Laboratoire de Matériaux et Environnement (LA.M.E)-UFR/SEA, Département de Physique, Université Joseph Ki-ZERBO, Ouagadougou, Burkina Faso
Email: traoreboureim@gmail.com

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Abstract

This scientific paper presents a study investigating the effects of defects at the CdS/CIGS and CdS/SDL interfaces on the performance of CIGS solar cells. The objective of this study is to analyze the influence of defects at the interface between the CdS buffer layer and the CIGS absorber, as well as the surface defect layer (SDL), on CIGS solar cell performance. The study explores three key aspects: the impact of the conduction band offset (CBO) at the CdS/CIGS interface, the effects of interface defects and defect density on performance, and the combined influence of CBO and defect density at the CdS/SDL and SDL/CIGS interfaces. For interface defects not exceeding 10^{13} cm^{-2}, we obtained a good efficiency of 22.9% when −0.1 eV < CBO < 0.1 eV. By analyzing the quality of CdS/SDL and SDL/CIGS junctions, it appears that defects at the SDL/CIGS interface have very little impact on the performances of the CIGS solar cell. By optimizing the electrical parameters of the CdS/SDL interface defects, we achieved a conversion efficiency of 23.1% when −0.05 eV < CBO < 0.05 eV.

Keywords

Numerical Simulation, CdS/CIGS Interface, Interface Defects, Conduction Band Offset (CBO), Surface Defect Layer (SDL)

1. Introduction

Today, thin films occupy a prominent place in the field of photovoltaic solar cells due to their low production cost and excellent conversion efficiency of up to 23.35% [1]. All these record efficiencies are closely linked to the quality of the buffer layer/absorber interface. The CdS/CIGS interface plays an important role in the separation of electron-hole pairs [2]. The CdS/CIGS interface is a region where the atomic arrangement is strongly disturbed, thus creating atomic inter-diffusion phenomena [3]. Annealing conditions [2] and post-deposition treatments, which require high temperatures, can modify the properties of the CdS/CIGS interface. This change in interface properties can lead to interface defects [4]. The difference in optical and electrical properties between the buffer layer and the absorber leads to detuning at the band level, resulting in a band offset at the CdS/CIGS interface [5]. Several studies performed with X-ray photoelectron spectrometry (XPS) have shown the presence of very thin In-rich n-type layers $(CuIn_3Se_5)$ on the surface of the CIGS absorber [2] [4]. This thin layer, identified as a surface defect layer is commonly referred to as (SDL). These studies have also shown that the composition of the absorber surface is different from that of the CIGS absorber volume [6] [7] [8]. The impact of defects at the CdS/CIGS interface on the operation of the CIGS-based solar cell is not yet well understood, and is the subject of several theoretical and experimental studies. Consequently, can the presence of this layer of surface defects at the CdS/CIGS interface significantly impact solar cell performance? After highlighting the three types of defects that limit cell performance at the CdS/CIGS interface, a detailed study of interface defects and conduction band offset at the CdS/CIGS interface will be carried out. Taking into account the surface defect layer (SDL), a study will also be carried out on the CdS/SDL and SDL/CIGS interfaces. Our aim is to study the impact of these defects at the CdS/CIGS and CdS/SDL and SDL/CIGS interfaces on the performance of the CIGS-based solar cell.

2. Device Model and Simulation Details

Numerical simulation is used to study the influence of solar cell parameters on these electrical characteristics without performing the experiment. In this work, we will use the SCAPS-1D software [9] [10] to perform our numerical simulations. SCAPS-1D uses the finite-difference method with well-defined boundary conditions to solve the basic equations: the Poisson equation, the continuity equations and transports equation of electrons respectively of holes. SCAPS is used to replicate and investigate all the available research-level CIGS solar cells with various buffer layers. From the solution provided by SCAPS simulation, output such as current voltage characteristics in the dark and under illumination can be obtained as a function of temperature.

The structure of the CIGS-based thin-film solar cell comprises a mechanical substrate, a molybdenum (Mo) back contact, a p-type CIGS absorber that forms the P-N heterojunction with the n-type CdS buffer layer, a transparent conductive oxide (OTC) window layer and an aluminum-nickel metal grid front contact. Its structure (ZnO:i)/(CdS/(CIGS/Mo)) is shown in **Figure 1(a)**. The second structure (ZnO:i)/(CdS/(SDL/CIGS)/Mo) studied with SDL is shown in **Figure 1(b)**.

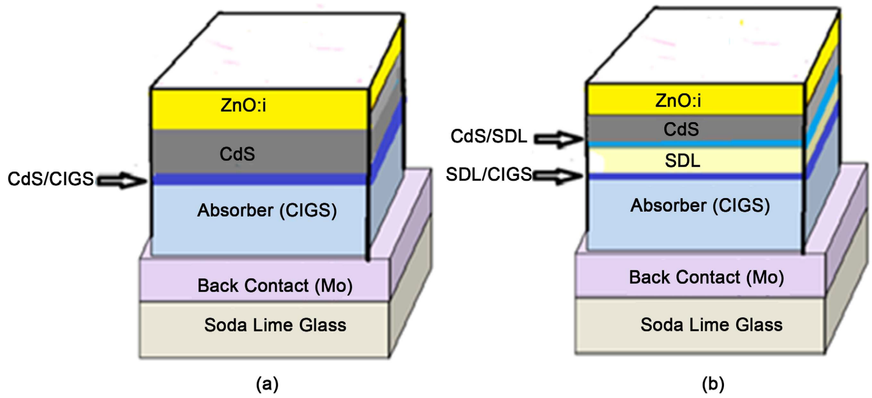

Figure 1. Structure of the CIGS solar cell with SDL (a) and without SDL (b).

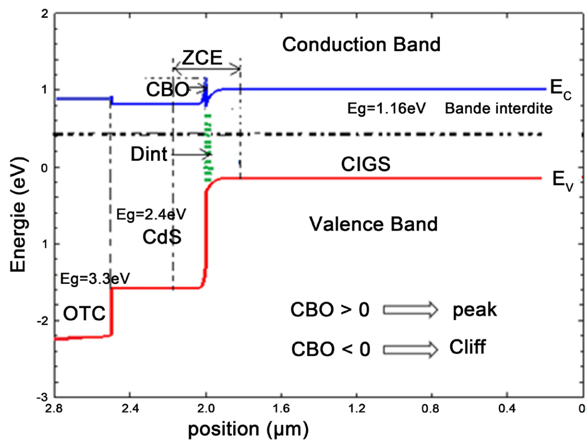

Figure 2. Energy band diagram of the cell when the conduction band of CIGS is above (CBO > 0) (a) and below (CBO < 0) (b) that of CdS.

At the interface between the CdS buffer layer and the CIGS absorber, Schmid et al have shown the presence of a thin surface defect layer (SDL) rich in n-type indium (**Figure 1(b)**). This thin layer is identified as a defect and formed by atomic inter diffusion between the CdS buffer layer and the CIGS absorber [11]. With a gap wider than that of the CIGS at volume [2] [12] this layer is formed on the surface of the CIGS. **Figure 2** shows the energy band diagram of the solar cell of the i-ZnO/(CdS/(CIGS/Mo)) structure. In **Figure 2(a)**, the conduction band of the CdS buffer layer is above that of the CIGS absorber, resulting in a peak (CBO > 0) at the CdS/CIGS interface. As for **Figure 2(b)**, the conduction band of CdS is below that of the CIGS absorber, resulting in a cliff (CBO < 0) at the CdS/CIGS interface.

The properties of the different layers and interfaces used for the numerical simulation are summarized in **Table 1**. These properties were obtained from theoretical and experimental results [11] [13] [14] [15].

The solar cell temperature is maintained at 300 K and is illuminated under standard conditions by an AM 1.5 G spectrum that accounts for both direct and diffuse radiation. In order to validate our results, we compared the J-V characteristic curves of our numerical simulation with that performed experimentally by

Table 1. Parameters used to simulate the CIGS solar cell CIGS.

Layers properties				
	i-Zno	CdS	SDL	CIGS
Thickness (nm)	300	50	15	2500
Band gap (eV)	3.3	2.4	1.3	1.25
Electron Affinity (eV)	4.55	Variable	Variable	Variable
Diélectric relative Permittivity	9.00	10	13.6	13.6
Effective densité of state in BC (cm^{-3})	$3.1*10^{18}$	$3.1*10^{18}$	$2*10^{18}$	$2*10^{18}$
Effective densité of state in BV (cm^{-3})	$1.8*10^{19}$	$3.1*10^{18}$	$1.5*10^{19}$	$1.5*10^{19}$
Electrons thermal velocity (cm/s)	$2.4*10^{7}$	$3.1*10^{7}$	$3.9*10^{7}$	$3.9*10^{7}$
Holes thermal velocity (cm/s)	$1.3*10^{7}$	$1.6*10^{7}$	$1.4*10^{7}$	$1.4*10^{7}$
Electrons Mobility (cm^2/Vs)	100	72	10	100
Holes Mobility (cm^2/Vs)	31	20	1.25	12.5
Doping concentration (cm^{-3})	$1*10^{17}(D)$	$5*10^{17}(D)$	$1*10^{13}(D)$	$1*10^{16}(A)$
Bulk defect properties				
Bulk defect Density (cm^{-3})	$1*10^{16}$	$5*10^{16}$	$1*10^{14}$	$1*10^{14}$
Capture cross-section electrons (cm^2)	$1*10^{-15}$	$1*10^{-15}$	$5*10^{-13}$	Variable
Capture cross-section holes (cm^2)	$5*10^{-13}$	$5*10^{-13}$	$5*10^{-15}$	$5*10^{-15}$
Interface Properties				
	CdS/SDL		SDL/CIGS	
Interface defect density (cm^{-2})	Variable		Variable	
Capture cross-section electrons (cm^2)	$1*10^{-15}$		$1*10^{-15}$	
Capture cross-section holes (cm^2)	$1*10^{-15}$		$1*10^{-15}$	

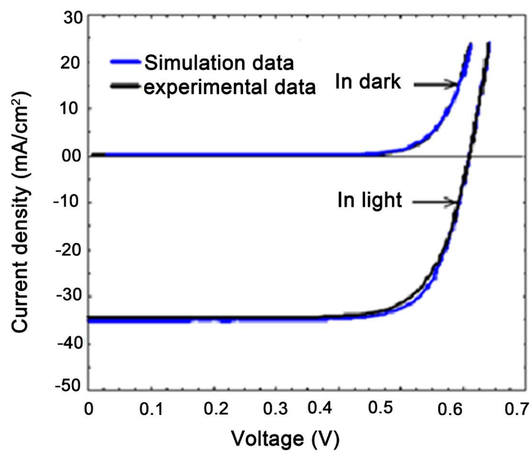

Figure 3. J-V characteristic curves compared compared with experimental results by Pettersson *et al.* [11].

Pettersson. A good agreement is found between these two results, as shown in **Figure 3**.

3. Result and Discussion

3.1. CdS/CIGS Interface

In the absence of the surface defect layer (SDL), the predominant defects at the buffer layer/absorber interface are interface defects and band offset. These defects are due to inter-diffusion phenomena and band alignment at the buffer layer/absorber interface. To this end, we will study the impact of interface defects on solar cell performance as a function of minority carrier lifetime in the CIGS absorber. The same will apply to the conduction band offset on solar cell performance.

3.1.1. Band Offset at the CdS/CIGS Interface and Minority Carrier Lifetime in the Absorber

The conduction band offset at the CIGS/CdS interface and the minority carrier lifetime (τ_n) in the absorber are two very important parameters affecting the performance of the CIGS-based solar cell CBO is represented by the difference in electronic affinity between the absorber (CIGS) and the buffer layer (CdS). To carry out our simulations, we will keep the electronic affinity of the absorber constant $\chi_{CIGS} = 4.5\text{ eV}$ by varying that of the buffer layer χ_{CdS} from (4 eV to 5 eV) thus resulting in a variation of the conduction band offset from −0.5 eV to 0.5 eV. The lifetime of the minority carriers in the absorber will vary from 10^{-2} ns to 10^{1} ns with a step of 10 ns. Since the absorber in this cell is p-doped, the minority charge carriers are electrons. **Figure 4** shows the influence of the conduction band offset at the CdS/CIGS interface on the electrical parameters $\left(J_{SC}, V_{OC}, FF, \eta\right)$ as a function of the minority carrier lifetime in the absorber. Generally speaking, all electrical characteristics increase as the electron lifetime in the absorber increases. When CBO < −0.2 eV, all electrical parameters of the solar cell decrease. Open-circuit voltage (V_{OC}) and conversion efficiency (η) are the characteristics most affected (**Figure 4(a)**, **Figure 4(d)**). This decrease can be explained by a high cliff depth (**Figure 3(b)**). The cliff decreases the potential difference across the ZCE, thus increasing the probability of recombination at the CdS/CIGS interface, leading to a decrease in (V_{OC}). Above −0.2 eV, (V_{OC}) is almost constant. When CBO > 0.4 eV (**Figure 4**), solar cell performance decreases sharply through short-circuit current density (J_{SC}), efficiency η and form factor (FF).

This decrease may be due to the high peak shown in (**Figure 3(a)**). This peak acts as a barrier against photo-generated electrons in the absorber. If the peak height exceeds 0.4 eV, the photo-generated electrons cannot cross the barrier, so they recombine with the holes. These results are in good agreement with numerical simulations carried out on the CdS/CIGS interface by Minemoto *et al.* and Gloeckler *et al.* [16] [17]. They concluded that photogenerated carrier transport is blocked if CBO > 0.4 eV, resulting in a reduction in short-circuit current

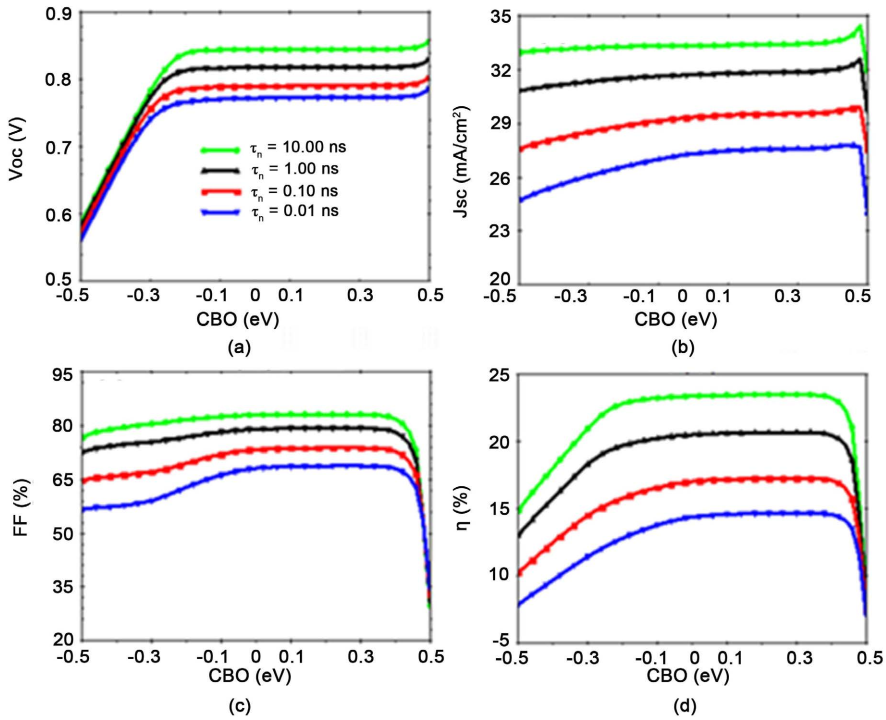

Figure 4. Effect of conduction band offset at the CdS/CIGS interface on electrical parameters as a function of electron lifetime in the absorber.

density (J_{SC}), form factor (FF) and device efficiency. When −0.1 eV < CBO < 0.1 eV, better performance is achieved with efficiency reaching 22.8%. This performance can be explained by a favorable conduction band alignment at the CdS/CIGS interface. This interval corresponds to very low values of peak height and cliff depth. However, adjustment of the conduction band discontinuity is necessary to improve solar cell performance.

3.1.2. Defects at the CdS/CIGS Interface and Minority Carrier Lifetime in Absorber

In CIGS-based solar cells, the CdS/CIGS interface is susceptible to have defects called interface defects (Dint) due to the different optoelectronic properties of CdS and CIGS. This interface is considered to be a zone of high recombination due to defects linked to dangling bonds. To quantify the impact that these interface defects play on the operation of the CIGS solar cell, simulations are carried out by varying the density of interface defects from 10^{10} cm^{-2} to 10^{18} cm^{-2}. **Figure 5** shows us the influence of defects at the CdS/CIGS interface on the electrical parameters as a function of the minority carrier lifetime in the absorber.

In general, all electrical characteristics increase with increasing electron lifetime in the absorber. When defects at the CdS/CIGS interface are less than 10^{13} cm^{-2}, very good performances are obtained through the electrical parameters as shown in **Figure 5**. However, interface defects greater than 10^{13} cm^{-2} leads to a decrease of all the electrical parameters of the cell as shown in **Figure 5**. This is

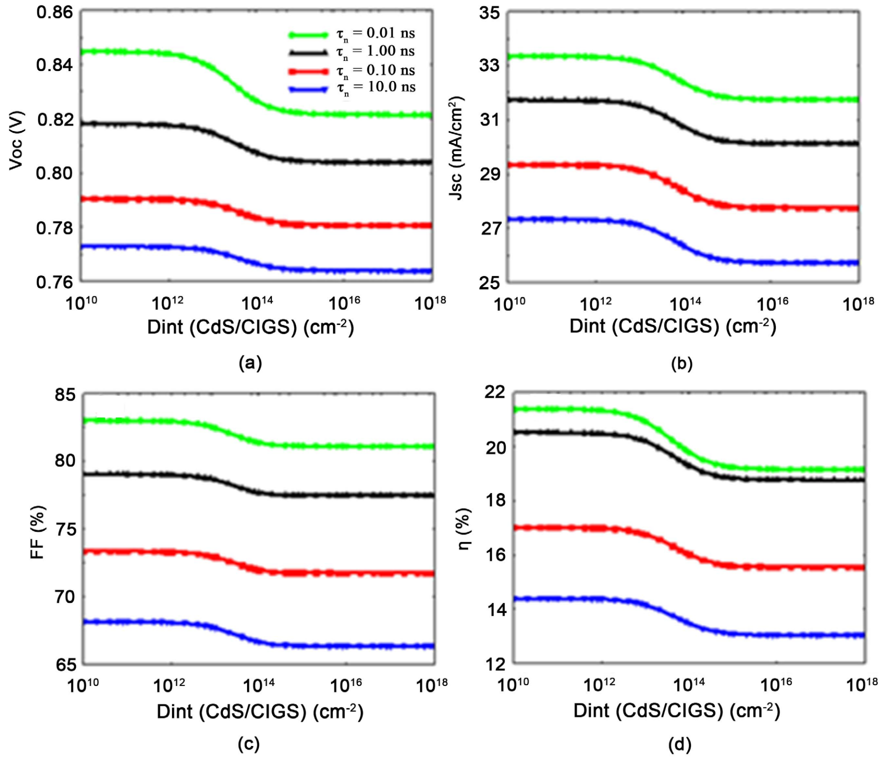

Figure 5. Effect of defect at the CdS/CIGS interface on electrical parameters as a function of electron lifetime in the absorber.

probably due to a Fermi level not very an favourable anchor level at this interface [15]. When defects at the CdS/CIGS interface are very large (Dint > 10^{13} cm^{-2}), the device's band structure exhibits weak band curvature in the space charge zone (SCZ), resulting in very poor cell performance.

3.1.3. Band Offset and Defect Density at the CdS/CIGS Interface

In Sections 3.1.1 and 3.1.2, we see that all electrical parameters increase as the electron lifetime in the absorber increases, and good performance is achieved for an electron lifetime in the absorber of 10 ns. For a deeper understanding, we will study the influence of the conduction band offset as a function of defects at the CdS/CIGS interface on the electrical parameters as represented in Figure 6.

For low values of the conduction band offset, very poor performances are obtained through the short-circuit current density (J_{SC}), form factor (FF) and device efficiency η for high values of defects at the CdS/CIGS interface *i.e.* exceeding 10^{15} cm^{-2} as shown in Figure 6(a), Figure 6(b), Figure 6(d). This study confirms the results obtained in Section 3.1.1. and 3.1.2. This poor performance can be explained by a high cliff that acts as a barrier against photogenerated electrons, favoring recombination phenomena via excessively high interface defects. When CBO > 0.4 eV, the efficiency η and the form factor decrease sharply as shown in Figure 6(c), Figure 6(d). This decrease in solar cell performance may be due to a very high peak as shown in Figure 3(a) As for the short-circuit

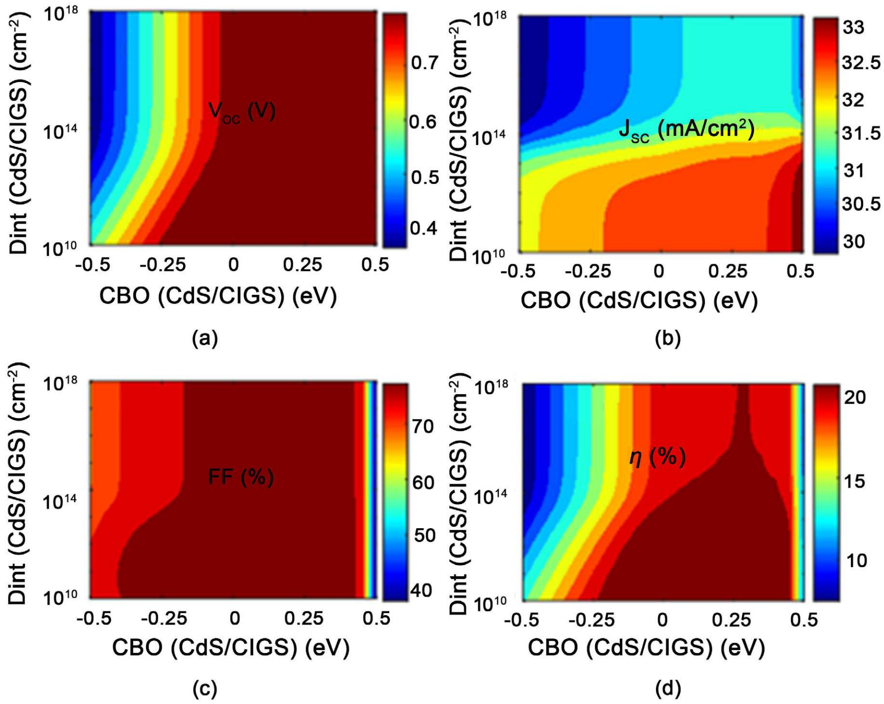

Figure 6. Effect of conduction band offset at the CdS/CIGS on electrical parameters as a function of electron lifetime in the absorber.

current density, it decreases when the interface defects exceed 10^{15} cm^{-2}. This can be explained by the combined effect of the high peak and fermi level anchoring due to the very high interface defects. At the end of this study dedicated to the CdS/CIGS interface, it emerges that better performances are obtained with −0.1 eV < CBO < 0.1 eV and interface defects lower than 10^{13} cm^{-2}.

3.2. CdS/SDL and SDL/CIGS Interfaces

3.2.1. Band Offset at the CdS/SDL and SDL/CIGS Interface and Minority Carrier Lifetime in the Absorber

Figure 7 shows us the influence of the conduction band discontinuity at the CdS/SDL and SDL/CIGS interfaces on the electrical characteristics as a function of electron lifetime in the absorber. In general, all electrical parameters increase with increasing electron lifetime in the absorber. When CBO < −0.1 eV, the open-circuit voltage (V_{OC}) decreases at the CdS/SDL and SDL/CIGS interfaces compared with the CdS/CIGS interface, where (V_{OC}) decreases when CBO < −0.3 eV. This decrease may be due to the double cliff at both interfaces. The cliff decreases the potential difference across the space charge zone (ZCS), thus increasing the probability of recombination at both interfaces. When CBO > 0.3 eV, the open-circuit voltage (V_{OC}) remains relatively constant at the CdS/SDL interface (Figure 7(a)) and decreases sharply at the SDL/CIGS interface (Figure 7(b)). As for the short-circuit current density (J_{SC}), it grows linearly with the CBO at the CdS/SDL interface Figure 7(c). When CBO < −0.4 eV and CBO > 0.1 eV, (J_{SC}), decreases at the SDL/CIGS interface Figure 7(d).

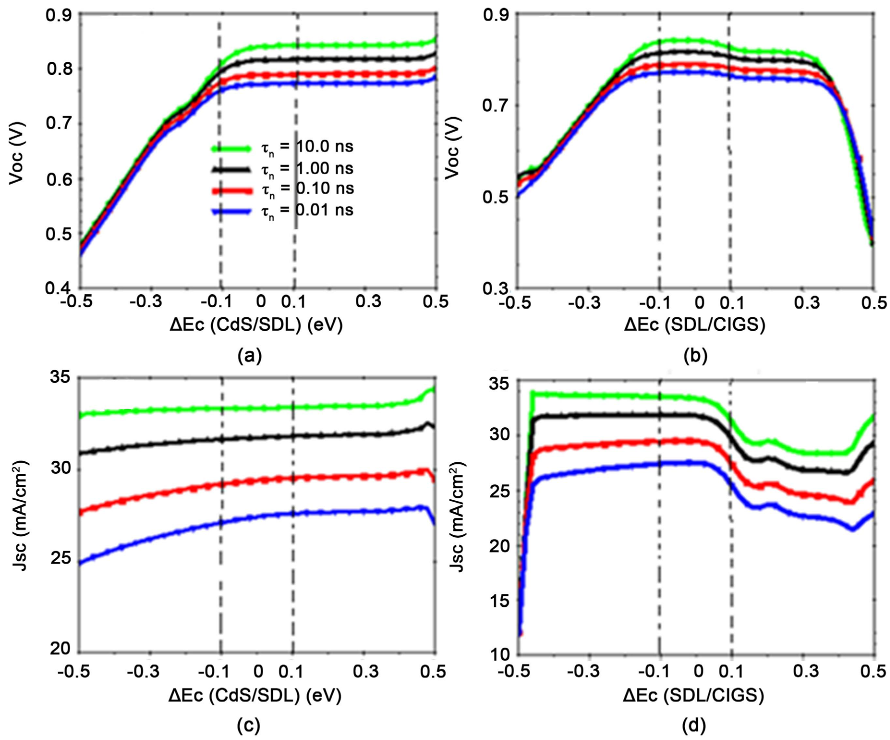

Figure 7. Effect of conduction band offset at the CdS/SDL and SDL/CIGS interface on electrical parameters (J_{SC} and V_{OC}) as a function of electron lifetime in the absorber.

In the previous section, we showed that better performance is achieved when −0.1 eV < CBO (CdS/CIGS) < 0.1 eV. Next, we will compare the conversion efficiency (η) when the conduction band offset at the CdS/SDL and SDL/CIGS interfaces is between −0.1 eV and 0.1 eV. At the CdS/SDL interface, the conversion efficiency increases slightly, reaching a value of 22.9% as shown **Figure 8(c)**. For the SDL/CIGS interface, the conversion efficiency increases to 23.1%, *i.e.* an efficiency gain of 0.2% (**Figure 8(d)**). In view of the above, we can say that an improvement in solar cell performance is observed when −0.1 eV < CBO (SDL/CIGS) < 0.1 eV. This implies that defects at the SDL/CIGS interface have less impact on solar cell performance. This may be due to the fact that the surface defect layer has almost the same composition as the absorber volume and that the p-n junction is formed between p-CIGS and n-SDL, not between p-CIGS and n-CdS [6] [8].

3.2.2. Defects at the CdS/SDL and SDL/CIGS Interfaces

To quantify the impact that interface defects play on the operation of the CIGS solar cell, we will simultaneously study the impact of defects at the CdS/SDL and SDL/CIGS interfaces on electrical performance as illustrated in the figure (**Figure 9**). Generally speaking, very good performance is observed when defects at the CdS/SDL and SDL/CIGS interfaces are less than 10^{13} cm^{-2}. At the CdS/SDL interface, performance decreases drastically when $\mathrm{Dint}(\mathrm{CdS/SDL}) > 10^{13}$ cm^{-2}. At the SDL/CIGS interface, performance decreases slightly when $\mathrm{Dint}(\mathrm{SDL/CIGS}) > 10^{13}$ cm^{-2}. This decrease may probably be due to an unfavorable Fermi level

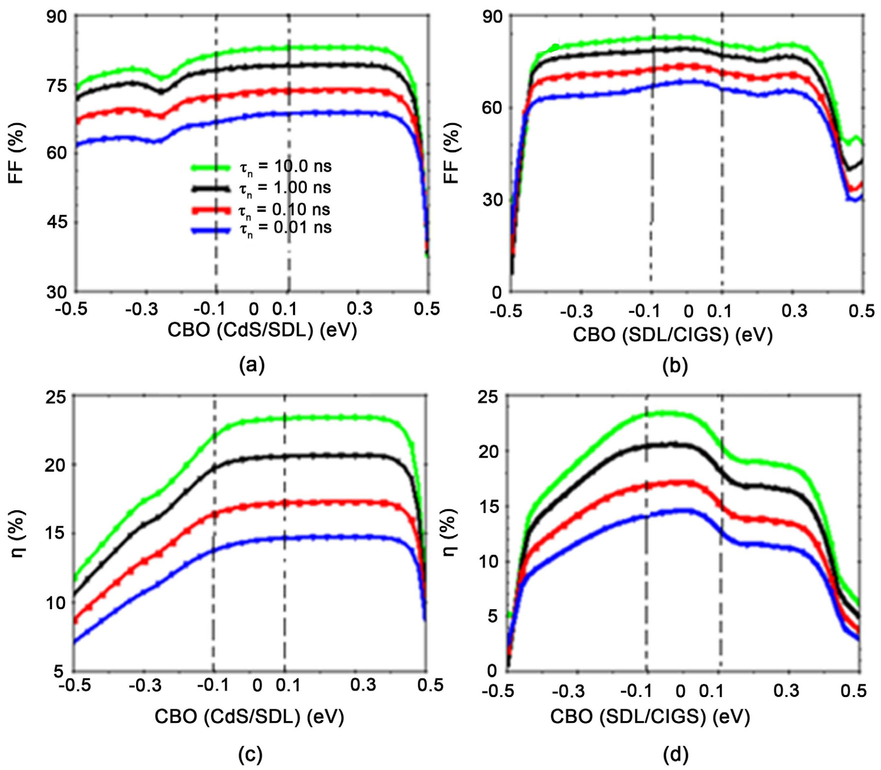

Figure 8. Effect of conduction band offset at the CdS/SDL and SDL/CIGS interface on electrical parameters (η and *FF*) as a function of electron lifetime in the absorber.

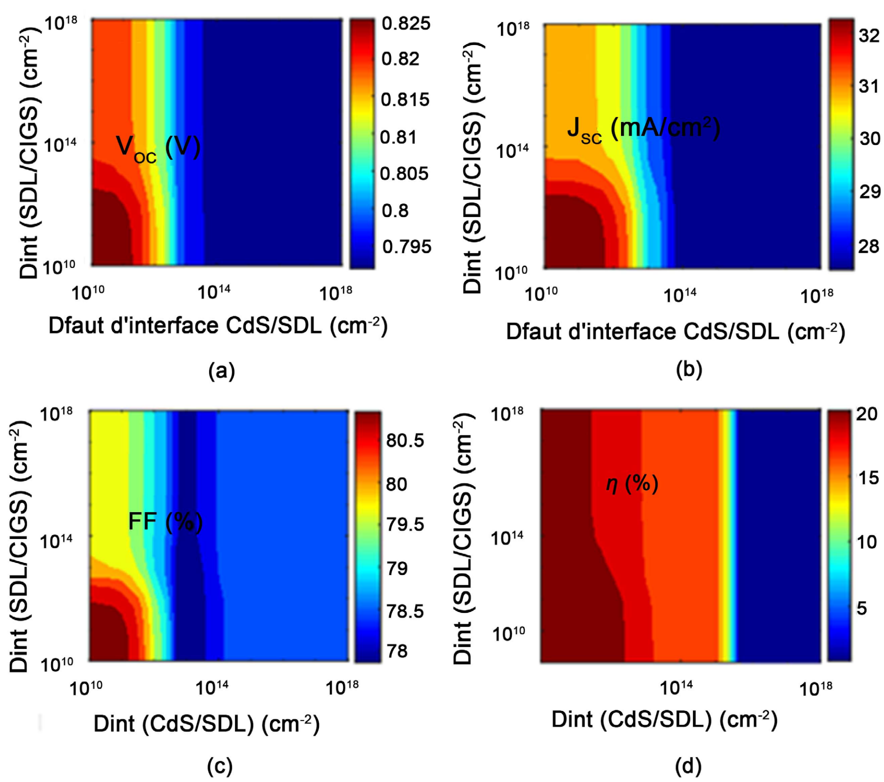

Figure 9. Effect of defect at the CdS/SDL and SDL/CIGS interface on electrical parameters.

anchoring at these interfaces [18]. At the end of our analysis, we can therefore say that defects at the SDL/CIGS interface have less impact on solar cell performance.

4. Conclusion

In this paper, based on numerical simulation, the SCAPS-1D software was used to study the impact of some interface defects on solar cell performance. In the first part of this work, a detailed study of the CdS/CIGS interface was carried out. This study consisted in determining the impact of the conduction band offset and defects at the CdS/CIGS interface as a function of the minority carrier lifetime in the absorber. It was found that very good performances are obtained when -0.1 eV < CBO < 0.1 eV and interface defects are less than 10^{-13} cm^2. The second part of our study was based exclusively on CdS/SDL and SDL/CIGS interfaces. A comparative study of conduction band offset as a function of minority carrier lifetime in the absorber was carried out. Subsequently, a simultaneous study of defects at the CdS/SDL and SDL/CIGS interfaces was also carried out. By comparing these two interfaces, it appears from this work that defects at the SDL/CIGS interface have less impact on solar cell performance. This work can be beneficial to the development of solar cells with good conversion efficiency. These results show the importance of interface defects in the architecture of new high-efficiency solar cells. These results may provide a basis for improving the performance of CIGS-based solar cells.

Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

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