

New Method for Diagnostics of Ion Implantation Induced Charge Carrier Traps in Micro- and Nanoelectronic Devices

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ABSTRACT

An important problem of defect charging in electron-hole plasma in a semiconductor electronic device is investigated using the analogy of dust charging in dusty plasmas. This investigation yielded physical picture of the problem along with the mathematical model. Charging and discharging mechanism of charge carrier traps in a semiconductor electronic device is also given. Potential applications of the study in semiconductor device technology are discussed. It would be interesting to find out how dust acoustic waves in electron-hole plasma in micro and nanoelectronic devices can be useful in finding out charge carrier trap properties of impurities or defects which serve as dust particles in electron-hole (*e-h*) plasma. A new method based on an established technique “deep level transient spectroscopy” (DLTS) is described here suggesting the determination of properties of charge carrier traps in present and future semiconductor devices by measuring the frequency of dust acoustic waves (DAW). Relationship between frequency of DAW and properties of traps is described mathematically proposing the basis of a technique, called here, dust mode frequency deep level transient spectroscopy (DMF-DLTS).

Keywords: Semiconductors; Ion Implantation; Defects; Dust Acoustic Waves; Deep Level Transient Spectroscopy; Electron-Hole Plasma; Nanoelectronics

1. Introduction

During the fabrication, defect or particulate contamination of microelectronic device structures is a serious concern. It can be due to unwanted growth on growth reactor walls or impurities in supply of atomic species in the reactor. Extended defect structures are also formed in different semiconductors used in electronic devices during ion implantation. Extended structures in ion implanted Sb doped Ge (Ge: Sb) form extended defect structures which show high thermal stability and also transform to other defect phases rather than repair. These defects have fatal effects on transport of charge carriers in semiconductor thin films used in electronic devices, which makes knowledge about them important [1-4]. Due to limitation of carrier mobility in Si, Ge has emerged as a key ingredient material for fabrication of a new generation of ultrafast devices in the regime of tens of gigahertz. Ion implantation can be used to write a network of devices on a semiconductor wafer due to possibility of controlled implantation beam size and energy, and masking of the target wafer.

Elemental implantation defects, especially charge car-

rier traps, and their electronic implications in Ge and similar materials have not been understood with sufficient details, so a comprehensive understanding of properties of defects (vacancies and self-interstitials) in Ge and related materials, and their interactions with impurity atoms is still required [4-7]. These elemental defects join impurities in implanted/doped semiconductors to form defect clusters which act as charge carrier traps. A generalized model for charging and discharging of defects in semiconductor electronic devices is presented here along with its perspective applications.

2. A Model of Defect/Impurity Charging

2.1. Physical Picture

In a perfect crystal of, say, Ge or Si, all the atoms are at their lattice sites and do not have ability to trap additional charge carriers. If impurities are introduced in a perfect crystal, they get ability to trap charge carriers. It may be noted that self interstitial and vacancies are also defects and can trap charge carriers. In real crystalline structure grown for use in devices, contain a variety of defects and

sometimes form defect clusters. These clusters are normally composed of vacancy-dopant or interstitial-dopant clusters. These extended clusters can trap a considerable fraction of electrons or holes present in the active volume of a device.

It is thought that these types of extended defect clusters are present in N-type Ge and prevent the feasibility of high speed electronic devices. Depending upon crystal and dopant, preset defect clusters can trap electrons or holes depending on the coulomb potential around defect, impurities or a defect cluster. Electron-hole plasmas are found in electronic devices crystals exposed to optical excitations etc. Defect clusters are exposed to electron and hole currents due to which they are charged. Defect charging in semiconductors is quite complex. After charging processes end, charged defects start discharging naturally. Charging/discharging of defect clusters in semiconductor devices are important and affect performance of devices. Charging and discharging of defects can be used for characterization of charge carrier traps in micro and nanoelectronic devices. Behaviour of deep level traps, which forms the basis for DLTS technique, is described by a schematic in **Figure 1** showing electron and hole traps in a semiconductor. Capture & emission by deep-level traps in a semiconductor. DLTS makes use of the measurement of the depletion region of a simple semiconductor electronic device, normally, a Schottky diode. In such a measurement, the regular reverse polarization of the diode is modified by the probing voltage pulse, resulting in the flow of carriers from the bulk to the measurement region, charging the defects or traps. After the pulse ends, thermal emission of carriers from the traps produces the capacitance transient in the device, called the DLTS signal.

2.2. Mathematical Model

Suppose an electron-hole plasma is generated in an electronic device with electron density as n_e and hole density n_h . For simplicity, we assume here extended defect clusters capable of trapping a considerable number of electrons. We consider a case of net electron trapping or negatively charged defects in a semiconductor device. The model situation resembles the typical case of ion implanted Ge:Sb. For the simplicity, we assume that at the time of generation of electron-hole plasma, $n_e - n_h$. In implanted Ge:Sb, highly stable vacancy-antimony-Ge clusters ($V_iSb_mGe_n$) are present which are thought to be electron traps in this n -type Ge. These extended defect clusters get charged like dust particles and grains in electron-ion plasma. Let the density of defect cluster or dust grain in $e-h$ plasma, generated in the above mentioned device, is n_d .

We further assume here that densities of electrons and holes are below the limit at which inter particle distance

becomes lower than de Broglie wavelength of any specific specie which assures that the case $e-h$ plasma being discussed here is of classical nature. If we take charge of electron as $-e$, hole as $+e$ and defect or dust grain $s - Z_d \cdot e$, the well-known condition of charge neutrality can be written as below:

$$-n_e e + n_h e - n_d Z_d e = 0 \quad (1)$$

Using simple algebra,

$$\frac{n_e}{n_h} = 1 - \frac{n_d}{n_h} Z_d \quad (2)$$

For any practical device, defect grain density is much lower than densities of electrons and holes, so the number

$$\frac{n_d}{n_h} Z_d \ll 1$$

which is the case of isolated dust or defect grains [8-11]. It may also be noted that in present devices defect grains can be only up to a few nanometer size. Maximum charge on defect depends upon defect structure and its size. A isolated defect or dust grain in $e-h$ plasma attains a floating potential ϕ_p which is determined by electron repulsion and hole collection in case of net negative charging of defects. The electron current responsible for depositing electrons on the defect is given by,

$$I_e = -4\pi a^2 e n_e \left(\frac{k_B T_e}{2\pi m_e} \right)^{1/2} \exp\left(\frac{e\phi_p}{k_B T_e} \right) \quad (3)$$

where m_e and T_e are electron effective mass and temperature, and a is the radius of the equivalent sphere of defect grain. The hole current compensating electron charging of a defect is given by,

$$I_h = -4\pi a^2 e n_h \left(\frac{k_B T_h}{2\pi m_h} \right)^{1/2} \exp\left(\frac{e\phi_p}{k_B T_h} \right) \quad (4)$$

where m_h and T_h are hole effective mass and temperature. For further details of Equations (3), (4), please see Refs. [8-12]. The charging equation of a negatively charged grain can be written as below, [8-10].

$$\frac{dZ_d}{dt} = -\frac{I_e + I_h}{e} \quad (5)$$

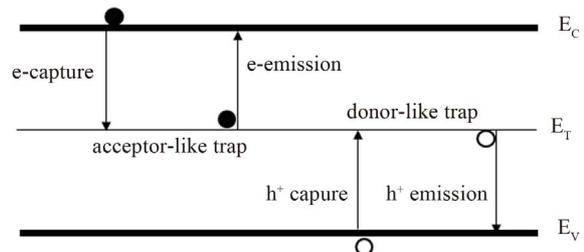


Figure 1. Energy band diagram for a semiconductor with deep-level traps. E_C is lower edge of the conduction band while E_V is the upper edge of the valence band.

Case of hole or positive charging of defects can be described using a simple analogy and comparison between electrons and holes.

2.3. Mechanism of Charging and Discharging of Electron Traps in an Electronic Device

Electron traps are centers in a semiconductor capable of trapping electrons with a certain binding energy. Traps cause power dissipation and reduce conductivity of the device. When electrons and holes are present in the form of a plasma in an electronic device, dust or defect grains are exposed to both electron (T_e) and hole (T_h) currents. These currents simultaneously charge and discharge defect grains. When $e-h$ plasma is first generated ($t = 0$) in an electronic device, a charging transient is produced after which charging and discharging perturbation continues until the device operation ends (end of $e-h$ pair generation). After this, a discharging transient is produced in which electrons are released due to thermal agitation and thermally generated holes. UV light can also produce discharging through photoelectron emission.

3. New Method for the Diagnostics of Charge Carrier Traps in a Micro- and a Nanoelectronic Device

The frequency ω of dust acoustic mode in electron ion plasma, with dust charged as negative, is given by [8-10],

$$\omega = kZ_d \left(\frac{n_{d0}}{n_{i0}} \right)^{1/2} \left(\frac{k_B T_i}{m_d} \right)^{1/2} \left[1 + \frac{T_i}{T_e} \left(1 - \frac{Z_d n_{d0}}{n_{i0}} \right) \right]^{-1/2} \quad (6)$$

where k is the wavenumber, k_B is the Boltzman constan, Z_d is charge on the dust, n_{d0} and n_{i0} are, respectively, equilibrium dust and ion densities, m_i and m_d are, respectively, ion and dust masses, T_e and T_i are electron and ion temperatures respectively and e is the electronic charge. With take the case of semiconductor device working at room temperature and having low electron and hole densities (due to low doping level) so that plasma behavior is classical. With charge traps or dust in the device, the above equation the following form by replacing ion parameters with hole parameters,

$$\omega = kZ_d \left(\frac{n_{d0}}{n_{h0}} \right)^{1/2} \left(\frac{k_B T_h}{m_d} \right)^{1/2} \left[1 + \frac{T_h}{T_e} \left(1 - \frac{Z_d n_{d0}}{n_{h0}} \right) \right]^{-1/2} \quad (7)$$

Now, m_h and n_{h0} are, respectively, hole mass and equilibrium density. Dust particles in $e-h$ plasma are impurities or defect clusters which can be positively charged, negatively charged or neutral. Dust particles in $e-h$ plasma can have a range of mass and mobility coefficient as they can be free or loosely or strongly bound to the host lattice structure. So, dust model in $e-h$ plasma in electronic devices can be of quite complex nature.

Here, following questions about $e-h$ -dust plasma in semiconductor devices are investigated. What can be the nature of dust modes in $e-h$ -dust plasma in semiconductor devices? Can these dust modes be useful in diagnostics of present or future micro or nanoelectronic devices? What can be the practical method of utilizing dust modes in diagnostics of semiconductor devices?

Dust particles (impurities or defects) in a semiconductor device act as electron or hole traps depending upon its electronic structure. If a pulse of electrons or holes is injected into a semiconductor device, as in a charge carrier trap characterization technique DLTS [13-15], these dust particles will be charged with electrons are holes. After the charge carrier feeding pulse ends, charged defects or dust particles will start discharging and it will continue until dust particles or defects reach their equilibrium charge. Dust mode frequency will also change as dust charge changes with time. This changing mode frequency with time is given by the following,

$$\omega(t) = kZ_d(t) \left(\frac{n_{d0}}{n_{h0}} \right)^{1/2} \left(\frac{k_B T_h}{m_d} \right)^{1/2} \left[1 + \frac{T_h}{T_e} \left(1 - \frac{Z_d(t) n_{d0}}{n_{h0}} \right) \right]^{-1/2} \quad (8)$$

In DLTS technique, the device is biased at a reverse bias V_R at which the bias is pulsed by a trap filling pulse V_P for a time t_p . Filled defect states start emptying, when bias returns back to V_R , and that results in a capacitance transient. Filling pulse is applied in a series and the varying capacitance of the diode $C(t, T)$ is given by [16],

$$C(t, T) = C_\infty - \Delta C_0 \exp(-e_p t) \quad (9)$$

where C_∞ is the equilibrium capacitance value at reverse voltage, ΔC_0 is the lowering of C_∞ at $t = 0$ and e_p is the hole emission coefficient. The above equation will be valid for electron traps with e_p replaced with e_n (the electron emission coefficient) and ΔC_0 is the rise of C_∞ at $t = 0$. DLTS spectrum is generated by applying a sine-function correlation with period P to $C(t, T)$ as,

$$S(T) = -\frac{1}{P} \int_0^P \sin\left(\frac{2\pi t}{P}\right) \cdot C(t, T) dt \quad (10)$$

The above procedure is applied to determine fundamental Fourier component of the transient, $C(t, T)$. For exponential transients, the period P , the emission coefficient e_p and T_{max} for which $S(T)$ shows a maximum, are related as [17]

$$1/e_p(T_{max}) = 0.42435 \times P \quad (11)$$

By choosing different appropriate values of period P , corresponding values of e_p and T_{max} can be determined for a specific transient $C(t, T)$ corresponding to a particular hole trap.

As clear from Equation (3), the frequency of dust

would depend on varying charge Z_d of dust particles in the same way as $C(t, T)$ during dust or trap discharge after the application of the filling pulse. So, dust mode frequency transient $\omega(t, T)$ for the same hole trap as in Equation (4), an analogue to capacitance transient $C(t, T)$, can be defined as,

$$\omega(t, T) = \omega_\infty - \Delta\omega_0 \exp(-e_p t) \quad (12)$$

where ω_∞ and $\Delta\omega_0$ are, respectively, equilibrium dust mode frequency and full magnitude of the frequency transient at $t = 0$. In the same way as in Equation (5), dust mode frequency DLTS or DMF-DLTS signal, $S_\omega(T)$, can be generated by applying the correlation sine-function as in Equation (5),

$$S_\omega(T) = -\frac{1}{P} \int_0^P \sin\left(\frac{2\pi t}{P}\right) \cdot \omega(t, T) dt \quad (13)$$

DMF-DLTS will show a set of peaks of $S_\omega(T)$ signal, each corresponding to a particular dust specie. This spectrum of peaks will be similar to a DLTS spectrum (**Figure 2**) with different DLTS peaks, with peak parameters carrying finger prints of dust species. Once dust mode frequency ω_∞ and change $\Delta\omega_0$ are measured, further details of experimental and analysis aspects of implementation of this new DLTS can be seen by a selected studies available in the common literature [13-19].

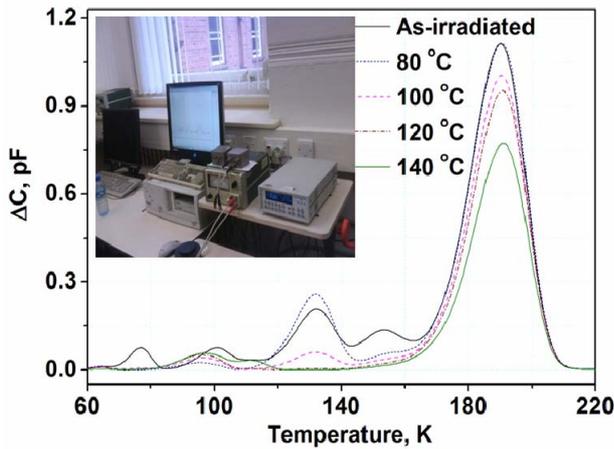


Figure 2. DLTS signal showing traps caused by the electron irradiation induced in Sb-doped ($\rho \approx 20 \Omega\text{-cm}$) Ge sample for the filling pulse of -0.5 V. Reverse bias -5 V and filling pulse duration of 10ms were used. As a simple rule, each peak represents an electronically active trap. Measurements of the same sample annealed for 30 m at temperatures of $100^\circ\text{C} - 220^\circ\text{C}$ are also shown which reduction or evolution of traps due to thermal treatment. The inset shows the measurement system at Microelectronics & Nanostructures Group, Electrical and Electronic Engineering, UMIST, University of Manchester, Manchester M60 1QD, UK University of Manchester, UK. These results were collected with the help of A. R. Peaker, V. P. Markevich and I. D. Hawkins.

4. Potential Applications and Discussion

The present investigation provides the essential information for understanding charging/discharging of defects in semiconductor electronic devices using transient and steady state conditions of operation. It is well known that switching on and off of a range of electronic devices affects their life. Charging and discharging currents produced, respectively, in switching on and off of an electronic devices affect its quality life.

Deep level transient spectroscopy [13-15] makes use of charging and discharging capacitance transients for characterization of charge carrier traps in a semiconductor electronic device. According to this study small scale charging and discharging perturbations continue even during steady state operation of devices. These perturbations would have higher magnitude and intensity if an electronic devices operation different operational stages. These perturbations produce a fluctuating field in the device. Fluctuating fields can have more deleterious effects on the operating device, especially if the fluctuation frequency is high.

Here, we classify defects in a semiconductor electronic device into three classes which are electronically inactive defects, electronically static defects and electronically dynamic defects. Electronically dynamic defects continue producing charging and discharging transients in an operating device and are most undesirable. Electronically inactive defects only decrease active volume of the device and have minimum undesirable effects whereas electronically static defects trap charge carriers but do not produce negligible charging and discharging transients after getting charged at start up of the device. The work presented here in conjunction with the fundamental plasma work [20,21] may lead to applications in the field of Nanotechnology [22,23] and nuclear instruments and methods [24-27].

Figure 3 is a pictorial view of findings of the paper. Physical significance of charge carrier traps in a semiconductor is shown graphically at the right bottom of the figure. Immediately above it shown is a physical process of bending of a crystal (as a pictorial view) which can introduce charge carrier traps in a crystal.

5. Conclusion

Defects are charged due to electron and hole currents. Meaningful charging/discharging continues until $I_e + I_h = 0$. Start up of a device and in some conditions the condition $I_e + I_h = 0$ is not fulfilled, so charge fluctuations continue causing energy dissipation which is undesirable due to the problem of decreased efficiency. Energy dissipation also limits life of the device. Using this investigation, defects in semiconductor electronic devices are classified into three groups, electronically inactive defects,

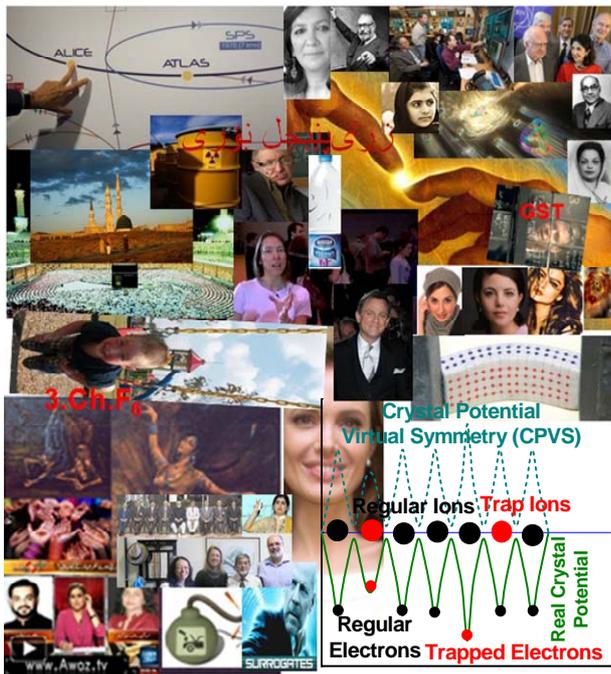


Figure 3. This is a pictorial view of the findings reported in the paper. For the better apprehension of the reader, some aesthetic/geometric Visualization of traps are shown. Right bottom (RB) is geometric visualization of charge carrier traps (here electrons shown) in the form of a plot. These traps have an analogy with massive dust particles in traditional and fullerene plasma [9,10]. Above RB plot, a pictorial view of bending crystal model is shown. Bending of a crystal can possibly create traps in it. Other than RB plot, typical mounts or mounted pictures are taken freely available on the web. Leading sources of the pictures are webpages of FermiLab Today (US), CERN (Switzerland), Dawn News (Pakistan), OGRA (Pakistan), PINSTECH/SID Library (PAEC, Islamabad, Pakistan).

electronically static defects and electronically dynamic defects. Electronically dynamic defects are most harmful for semiconductor electronic devices. A new technique DMF-DLTS is proposed here by describing measurement principle of the technique. This new technique combined with conventional and Laplace DLTS techniques can serve as a combination of carrier trap characterization techniques capable of extracting further advanced information about carrier traps in semiconductor devices.

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