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Study of Two One-Dimensional Multi Tunnel Junctions Arrays Structures by SIMON

Amine Touati, Samir Chatbouri, Nabil Sghaier, Adel Kalboussi

Laboratory of Microelectronics and Instrumentation, Faculty of Sciences of Monastir, University of Monastir, Monastir, Tunisia
Email: Amine.Touati@istls.rnu.tn

ABSTRACT

Multi Tunnel Junctions (MTJs) have attracted much attention recently in the fields of Single-Electron Transistor (SET) and Single-Electron Memory (SEM). In this paper, we investigate a nano-device structure using a two one dimensional array MTJs connected to the basic Single Electron Circuits, in order to analyze the impact of physical parameters on the performances and application of this structure. The device generates can operate at room temperature. The simulation of single-electron circuit demonstrates with Monte Carlo simulator, SIMON.

Keywords: Multi Tunnel Junctions (MTJs); Coulomb Blockade Effect; Effective Capacitances; SIMON Simulator

1. Introduction

As the semiconductor device feature size enters the sub-50-nm range, two new effects come into play. One is the quantum effect, which is rooted in the wave nature of the charge carriers, and gives rise to non classical transport effects such as resonant tunneling and quantum interference. The other is related to the quantized nature of the electronic charge, often manifested in the so-called single-electron effect: Charging each electron to a small confined region requires a certain amount of energy in order to overcome the Coulomb repulsion; if this charging energy is greater than the thermal energy, $k_B T$ (k_B: Boltzmann constant, T: temperature), a single electron added to the region could have a significant effect on other electrons entering the confined region.

Single-Electron Transistors (SETs) operate using a Coulomb blockade, which occurs in tiny structures made of conductive material due to electrostatic interactions between confined electrons. There are basically two types of SET application: memory devices [1] and logic functions have been proposed [2]. The small size is especially important for memory devices; memory cells have to be small to achieve a greater degree of integration.

Since the very early demonstration of the single-electron charging effect [3] a number of advances has been made. Low temperature experiments on the single-electron turnstile [4] have established and proven their working principle. Single-electron devices have also been applied to metrology, where a Coulomb blockade thermometry has been proposed [5].

For the future ultimate application of SETs, we must first succeed in the manipulation and the detection of a single electron. Basic demonstrations of single-electron transfer devices have been achieved at low temperatures, and some have even been realized at room temperature [6,7].

Raising the operating temperature as high as room temperature means that we have to reduce the island size of the order of a few nanometers. Although this is a challenging issue, some devices have been demonstrated that clearly and conclusively operate at room temperature through the use of recent rapidly developing nanotechnologies. The results provide excellent prospects for the future practical application of SETs.

The Multiple-Tunnel Junction (MTJ) consists of a one chain of nanoscale islands and tunnel junctions. In such a system, the single-electron charging of each island, and the effect of excess electrons on the polarization of neighboring tunnel junctions, modifies the Coulomb blockade region, and the *I-V* characteristics of the system. Furthermore, the single-electron charging energy of an island embedded within a chain of islands and tunnel barriers is also increased somewhat. The effective total capacitance of the system can be decreased and hence the charging energy EC and operating temperature T_{max} increased within the same fabrication technology by replacing the single junction of the transistor with short one-dimensional (1D) arrays. This raises the maximum temperature where single-electron effects are observed, in comparison with a simple double tunnel junction of similar island capacitance.

In this paper, we will concentrate on the *I-V* characteristics of one 1D-MTJs and tow 1D-MTJs.

2. Theory

2.1. Cell Design and Description

Figure 1 shows the circuit diagram for a two 1D MTJ with $(M - 1)$ islands, and M tunnel junctions in first line, and $(P - 1)$ islands, and P tunnel junctions on the second line. The islands are separated from each other and from the source and drain regions at the ends, by tunnel junctions with capacitance C. The remaining capacitance of each island is represented by C, and a bias V is used to inject electrons into the MTJ. The source is connected to the ground. Thus will reduce the error to the order $1/MP$, where M and P are the number of junctions in parallel and in series respectively. For numerical calculations, we used our universal single-electronics simulation program SIMON [8,9] based on a Monte Carlo approach.

The oxide layer separating the two MTJs is shown in **Figure 1** by a capacitor C_{ox}. Such as approximate expression of the capacity of oxide:

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_r S}{d} \tag{1}$$

The dynamics of the system are governed by the following equation which gives the tunneling rate of an electron in each one of tunnel junctions by using the "orthodox theory" [10] of single electron tunnelling:

$$\Gamma_{i \to j} = \frac{1}{e^2 R_T} \frac{\Delta F_{ij}}{1 - \exp\left(\Delta F_{ij}/k_B T\right)} \tag{2}$$

where $\Delta F_{ij} = \Delta F_i - \Delta F_j = -eV_{ds}$ is the difference between the free energy of the initial and final states, where V_{ds} is the source voltage, and R_T is the tunneling resistance of the junction. The tunneling rate of global system it is:

$$\Gamma = \sum_M \Gamma^1_{i \to j} \sum_P \Gamma^2_{i' \to j'} \tag{3}$$

where $\Gamma^{1,2}$ denote the first and second arrays respectively. The sum is made on the M and P MTJs. The theory of uniform one 1D arrays of tunnel junctions is well developed for the case of low temperatures, $k_B T << E_{ch} = e^2/C_\Sigma$ [11,12]. When the temperature becomes so high that the energy scale of thermal fluctuations $k_B T$ exceeds of the single-electron addition energy Ec, these fluctuations smear the Coulomb blockade, making the operation of the transistor impossible. The Monte Carlo simulations show that the tunnel junction capacitance C which is used in the equations for one 1D array should be replaced in the two 1D case by an effective capacitance C_{eff} which is higher than the real capacitance.

Experimentally, MTJs with constant values of C and C_{ox} have been fabricated mainly using metal islands [13]. An important property of the two 1D array is that it can be fabricated with lower resistance than a one 1D array, even if it contains many junctions in series. For a good functioning of the structure and to avoid degradation of the system we must choose a high number of junctions

The charging energy of the island creates an energy barrier which blocks the entrance of electrons into the MTJ so that multistable states of different numbers of electrons can be formed. The MTJ is also important in suppressing co-tunneling effects; that is, electron tunneling simultaneously across more than one junction.

2.2. Physicals Parameters

The tunneling occurs through one tunnel junction and the simultaneous tunneling of electrons across the other junctions is neglected. When the tunneling through $2M$ ($M = P$) junctions is considered, the other junctions behave simply as capacitors. The effective capacitance C_{eff} at island is given by:

$$C_{eff} = C_i + C_{ox} \tag{4}$$

where

$$C_i = \left[\frac{2M}{2M - 1}\right] C \tag{5}$$

In an infinite 1-D array, the capacitance between two neighboring islands is exactly twice the capacitance of the tunnel junctions, and this is the reason that the offset voltage is a factor of 2 lower in a two 1-D array compared to a one 1D array.

For the kth island, the potential is given by:

$$V_k = -\frac{e}{C_{eff}} \tag{6}$$

This may be used to write the potential at the $(k - 1)^{th}$ island.

The effective charging energy, $E_{c,MTJ}$ is defined similarly to the usual charging energy, except the physical capacitance is replaced with the effective capacitance:

$$E_{ch,eff} = \frac{e^2}{2C_{eff}} \tag{7}$$

R$_{T,1}$, C$_1$ R$_{T,2}$, C$_2$ R$_{T,i}$, C$_i$ R$_{T,i+1}$, C$_{i+1}$ R$_{T,M-1}$, C$_{M-1}$ R$_{T,M}$, C$_M$

C$_{ox,1}$ C$_{ox,i}$ C$_{ox,N-1}$

R$_{T,1}$, C$_1$ R$_{T,2}$, C$_2$ R$_{T,i}$, C$_i$ R$_{T,i+1}$, C$_{i+1}$ R$_{T,P-1}$, C$_{P-1}$ R$_{T,P}$, C$_P$
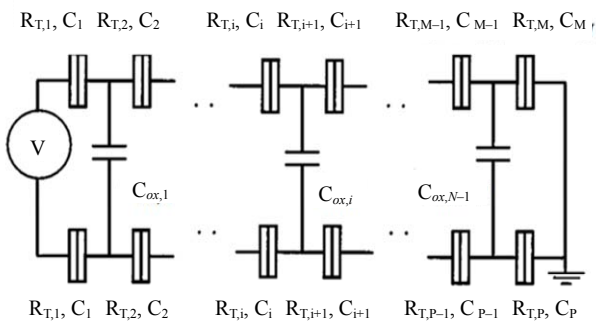
Figure 1. A circuit diagram of tow one-dimensional array of tunnel junctions. Junction *i* is characterized by its tunnel resistance R$_{T,i}$ and capacitance C$_i$ in parallel and islands have a oxide capacitance C$_{ox,i}$.

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Applying a large enough voltage V will inject a electron into the MTJ, and a current begins to flow. The threshold voltage when this occurs is given by:

$$V_{th} = \frac{e}{C_{eff}} \tag{8}$$

The value of the threshold voltage is low compared to the voltage corresponding to the sum of the individual charging energies of the islands. This is because the applied voltage drops more across the first junction, closest to the voltage source, due to the presence of the stray capacitance C_{ox} at the first island. We have further-more assumed that the offset voltage of a two one dimensional arrays of tunnel junctions is:

$$V_{off} = \frac{Ne}{4C} \tag{9}$$

3. Simulation Results

3.1. *I-V* Characteristic

We will now consider the *I-V* characteristics of the two 1-D MTJs. As the bias V increases, the number of transitions in the MTJs increases (**Figure 2(b)**). We consider a simple two island MTJ, where the electron numbers on the islands are n_1 and n_2 respectively. The charge state of the MTJ without any extra electrons may be expressed as $(n_1, n_2) = (0, 0)$ [14]. When a bias $V > V_{th}$ is applied, an electron tunnels onto the first island, creating the state (1, 0). This electron can then move through the MTJ, through the states (0, 1) to (0, 0) as it leaves the MTJ. However, as the applied voltage is increased, other transitions become possible, e.g. one may transition from the state (0, 1) either to the state (0, 0) or to the state (1, 1). These additional transitions lead to an increase in the current. For a longer MTJ, larger numbers of transitions are possible.

The theoretical results presented give that $C_{eff} = 0.52$ aF; C_{eff} is lower than the total capacitance attached to an island $2C_T + C_{ox} = 0.8$ aF; and $E_{ch,eff} = 0.15$ eV = 6 k_BT (k_BT = 0.025 eV at 300 K), this proves that the charging energy is much higher than the thermal energy. Therefore increase the number of tunnel junctions network can overcome the effect of low capacity and temperature operating. The staircase is typically irregular, with variation in the step heights and widths. The blocking region is more important, also when the number of junctions increases for 2 × 7 MTJs. The threshold voltage is 0.3 V from (Equation (8)), and from the curve it is ~0.4 V. The current I it changes from ~1 nA (7 MTJs in parallel) to ~ 5.2 nA for 3 MTJs.

For the effects of bias voltage V_{ds}, we find that it has a more effect on the electron tunneling than that of the one single electron tunneling, *i.e.* Single-Electron Transistor (SET), at some favored value more than of the Coulomb

blockade voltage.

Also, the tunneling rate of global system has a new factor so that: $\Gamma' = \alpha \times \Gamma$ where α is factor which depend on the effect of stray capacitor; with stray capacitances, the change of the Gibbs free energy due to the cotunneling process.

A typical result (**Figure 3**) has shown that the main effect of the stray capacitances is to reduce the threshold
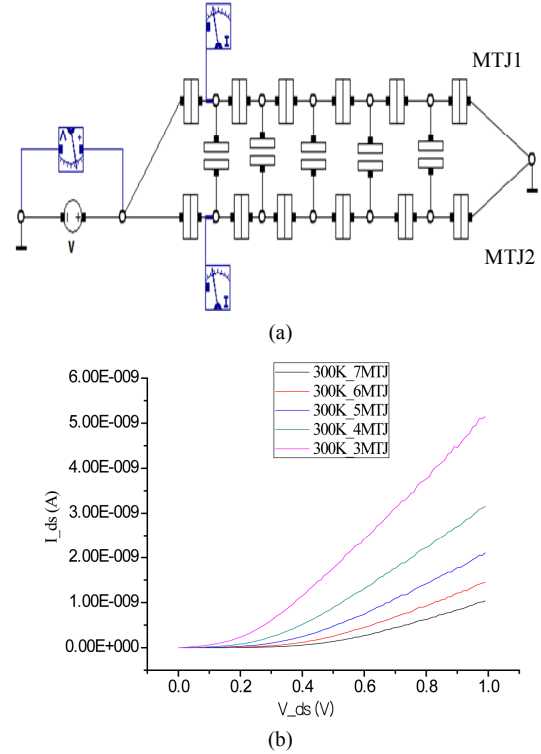

(a)

(b)

Figure 2. A SIMON (a) equivalent circuit of a device with two 1-D MTJs consisting of 10 islands and 11 MTJs with $C = 3 \times 10^{-19}$ F, $C_{ox} = 2 \times 10^{-19}$ F and $R_T = 40$ MΩ. C, C_{ox}, and R_T represent the tunnel junctions capacitance, oxide capacitance, and tunnel resistances, respectively; (b) Drain current vs. source-drain voltage characteristics at $T = 300$ K. 3, 4, 5, 6 and 7 MTJ denote the number of tunnel junctions in each array.
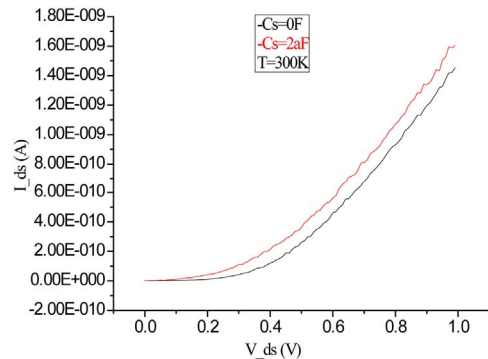

Figure 3. Stray capacitor (Cs) effect on the drain current of two 1-D device at 300 K.

voltages, whereas it has very little effect on the magnitude of the tunneling current [15,16]. In general, when the stray capacitances increase, the *I-V* curve of the single-electron device is shifted towards the low-voltage side.

3.2. Temperature Effect on Device

Figure 4(a) show the behavior of *I-V* at 4.2 K and 300 K for one dimensional and two dimensional arrays respectively. At low temperature the curve exhibited no current in the range of applied voltage from 0 to 0.3 V for two 1-D arrays; the Coulomb blockade (CB) region but for one 1D we do not observe clearly the CB zone. However, at room temperature for one dimensional device showed a linear increase even in the zero bias regions, on the other hand, for two one dimensional structures we can perceiving the transistor performance. This means that electron tunneling was suppressed because the charging energy of the nanoparticle was sufficiently larger than the thermal fluctuation energy at 300 K.

Then we have tried to see the effect of temperature on the two 1-D device **Figure 4(b)**, the CB zone is contracted when the temperature increase. The conduction current is activated at higher temperatures even at low temperature, and the *I-V* curve is not looks ohmic attitude. Also the increase in the temperature increase the conductivity and this due to excited states of the array that are thermally populated, which contribute to the current.

The clear Coulomb staircase suggests a strong asymmetry in the junctions along the MTJ, and this may be modeled by means of a random variation in the tunnel junction resistances R_T, associated with the observed variation in nanocrystal separation.

3.3. Device Function with Two Gate Voltages

For the applications of that structure, such as the multiple value logic (MVL) circuits [17], logic memory circuit [18] and hybrid SET-MOS [19], we need to have a gate or multi-gates allows more than two levels of logic. So we have added to the circuit in the **Figure 2(a)**, two gates for each array; generally the two gates, one gate is used as voltage input port and the other gate is used as threshold voltage adjusting port. Single-electron current oscillations are observed in the I_{ds}-V_{gs} characteristics **Figure 5** without degradation like we have a simple SET, the oscillations persist up to 300 K with an unchanged period. The oscillation periods increase when the temperature
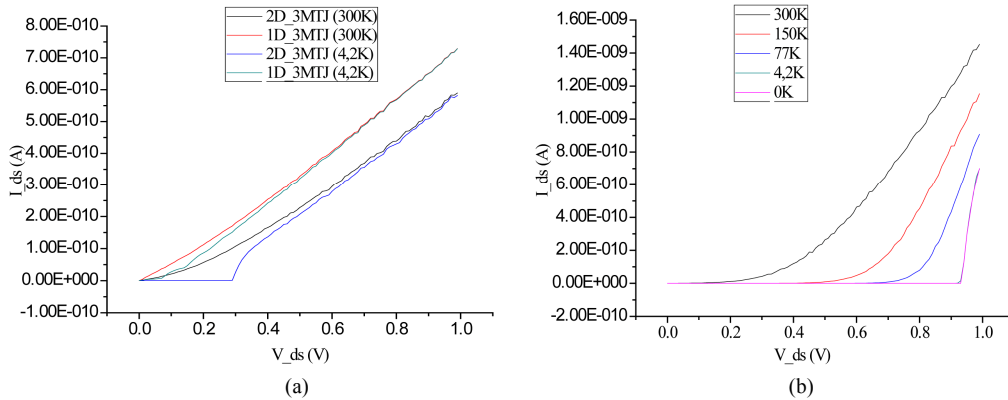

Figure 4. Monte Carlo simulation of the I_{ds}-V_{ds} characteristics (a) of one and two 1D-MTJs at 4.2 K and 300 K; (b) Temperature effect on two 1D with 7 MTJs in parallel.
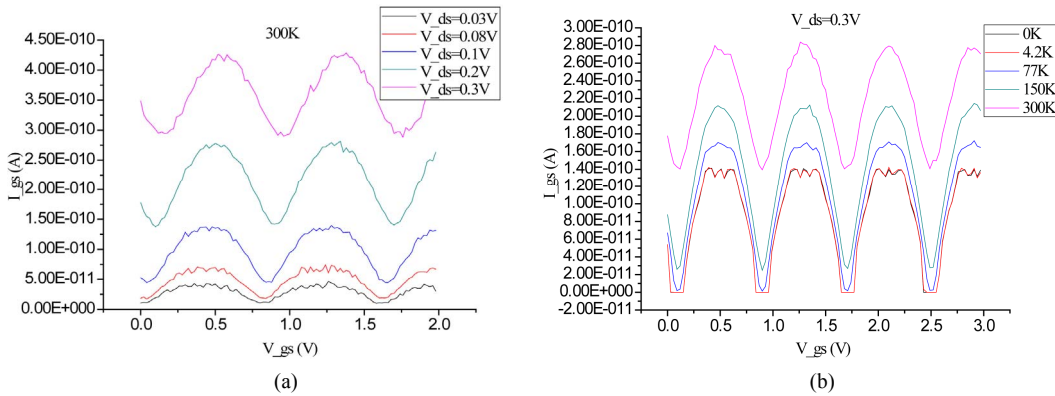

Figure 5. Periodic single-electron oscillations in the I_{ds}-V_{gs} characteristics of two one dimensional arrays with *M = P* = 6, (a) At a constant value of *T* = 300 K as temperature is varied; (b) At a constant value of V_{ds} = 0.3 V as temperature is varied.

and drain-source voltage are increased, and decrease when the T and V_{ds} are decreased.

The decrease in the oscillation period with increasing width implies an increase in the island capacitance. This is because the gate-islands capacitances (C_s) now are associated with the part of the electric field between the gates and island which passes through the oxide. The effect of the quantum dot size can be observed directly in the single-electron characteristics, as this is proportional to the island capacitance and therefore determines the Coulomb gap and the current oscillation period.

4. Conclusion

We have studied the temperature influence on one of promising single electron system that consists of two parallel 1D arrays. A Monte Carlo simulation showed that the stray capacitor C_0 the coupling capacitor C_{ox}, and the bias voltage V_{ds} play important roles to determine the electron transport on the system. On the other hand the tunneling rate of the system, the charging energy, and the temperature has a direct influence on the C_{eff} values. Finally, the obtained results are very interesting which give insight into the behavior of the tow one-dimensional with both arrays ($2M$) should provide guideposts for future implementation of logical memory circuits.

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