World Journal of Nano Science and Engineering, **2011, 1, 84-88**
doi:10.4236/wjnse.2011.13013 Published Online September 2011 (http://www.SciRP.org/journal/wjnse)

Scientific Research

Preparation and Characterization of TiO_2 and SiO_2 Thin Films

Davinder Rathee[1], Sandeep K. Arya[1], Mukesh Kumar[2]
[1]*Department of Electronics and Communication Engineering*, *Guru Jambheshwar University of Science and Technology*, *Hisar*, *India*
[2]*Department of Electronics Science*, *Kurukshetra University*, *Kurukshetra*, *India*
E-mail: *jerry_2c@yahoo.com*
Received June 25, 2011; *revised July* 25, 2011; *accepted August* 10, 2011

Abstract

Although scaling will continue for couple of decades but device geometries reaches to atomic size and limitation of quantum mechanical physical boundaries. To address these problems there is need of innovation in material science & engineering, device structure, and new nano devices based on different principle of physics. So TiO_2 thin films have been grown on well clean N-type silicon substrates via a sol–gel spin coating method. MOS capacitor were fabricated and characterized with SiO_2 and TiO_2 as dielectric material on N-type silicon wafer. The thickness was measured by stylus profiler and found to be 510 Å and 528 Å for SiO_2 and TiO_2 respectively. Some of the material parameters were found from the measured Capacitance -Voltage (C-V) curve obtained by SUPREM-III (Stanford University Process Engineering Model Version 0-83) for SiO_2 and C-V Keithly 590 analyzer for TiO_2 thin films. The result shows that obtained TiO_2 film present a dielectric constant of approximately 80. The refractive index was found to be 2.4 and optical constant was 5.43 obtained from Ellipsometry. Band gap 3.6 eV of TiO_2 was calculated by spectrophotometer and Surface morphology was obtained using Scanning Electron Microscope (SEM-JEOL) micrograph. The aluminum (Al) metal was deposited by the thermal evaporation system on the back side of the sample for the ohmic contact. Analysis shows that TiO_2 may be acceptable as a viable substitute for high k dielectric in order to prevent the tunneling current problems.

Keywords: Thin Films, Sol-Gel, Capacitance-Voltage Curve, TiO_2, Flat Band Voltage

1. Introduction

The silicon industry has been scaling SiO_2 aggressively for low power, high performance CMOS logic applications. The tunneling current increases exponentially as the thickness of the dielectric decreases. Now a day's TiO_2 oxide layers are being studied intensively as one of the promising high K dielectric for high density DRAM applications [1]. According to International Technology Roadmap for Semiconductor (ITRS) a dielectric constant higher than 25 is needed to meet the scaling goal and at the same time to keep the gate leakage current within tolerable limit (10 A/cm^2) [2]. There are various challenges with new high K dielectric i.e must have large band gap, nature must be amorphous, thermodynamically stability, and good interface quality with Si [3,4]. Several high K materials are considered to replace SiO_2 gate dielectric among them metal oxides having value high than 25 are of interest [4]. Here we present the study of Titanium dioxide (TiO_2) as a gate dielectric layer.

2. Experimental

The films were deposited on N-type <100> silicon substrate in the 2-10 Ω cm resistivity range. The silicon wafer was chemically cleaned by RCA standard cleaning procedure to remove insoluble metallic and organic contaminants.

2.1. Nanocrystalline Dielectric Film Deposition

TiO_2 thin films were deposited on Silicon <100> substrate using Sol-Gel method. Titanium isoproxide (TIP) was used as the Titania precursor. The matrix sol was

Copyright © 2011 SciRes.

prepared by mixing TIP with absolute ethanol and acetic acid in the molar ratio of 0.1:8:0.1. The substrate was placed on spinner and drops of above mentioned solution were placed on substrate. The substrate was then allowed to spin for 2 minutes with spinning rate 1500 rpm. Then sample was baked for 20 minutes at 95˚C. The film was than annealed in dynamic air at 550˚C for 30 minutes to treat the adsorbed film. While SiO_2 film was grown on silicon substrate using dry oxidation process at 650˚C for 60 minutes with a pre ramp of 5˚C per minute so that we reach reached to 950˚C and than flat temp of 950˚C for the 110 minutes at last post-ramp of 5˚C per minutes for 60 minutes with N_2(12) and O_2(32).

2.2. MOS Capacitor Fabrication

MOS capacitors were fabricated on a 4 inch diameter & 800 micron thick N-type silicon wafer. The dielectric layer of 510 Å was grown on silicon wafer by dry oxidation at 950˚C for 2 hours. About 3000 Å of aluminum was then deposited over oxide layers using the sputtering technique. The 10^{-2} cm^2 capacitor contact was defined by physical mask. The contacts were annealed in gas atmosphere H_2, & N_2 at 350˚C for 25 minutes. The fabricated capacitors electrically tested to characterize the material and to inspect the device performance. The variation of capacitance (C) with voltage V_G ranging –5 Volts to +5 Volts is shown in **Figure 2**.

In this work MOS capacitor were fabricated utilizing TiO_2 film deposited by Sol Gel spin coating method and SiO_2 films were thermally grown on <100> silicon substrate. The C-V measurement for TiO_2 was obtained using C-V analyzer [5,6], while SUPREM-III tool was used for SiO_2 layer. SUPREM- III is a computer program that allows the user to simulate the various processing steps used in manufacturing of the Silicon integrated or discrete devices [7]. The characterization of the samples was carried out at room temperature. Two dimensional SEM images of the TiO_2 film of thickness 52 nm (average film thickness for three sol-gel immersion cycles) were obtained (using JEOL-JM-6510 model shown in **Figure 1**), the accelerating voltage was kept at 5 kV. The optical properties were studied using UV-Visible spectrophotometer.

3. Results and Discussion

3.1. Film Characetrization

The porous nature of the film is clearly visible. The refractive index (n) of the TiO_2 film measured by Ellipsometer and was found to be 2.33. The optical dielectric constant can be determined from the refractive index of TiO_2 $\varepsilon_{opt} = n^2 = 2.33^2 = 5.4389$. The band gap was calculated 3.6 eV by using equation $\varepsilon = c/\lambda$, ε is photon energy, c speed of light and λ cut of wavelength by the help of Spectrophotometer as shown in **Figure 1(b)**.

3.2. MOS Capacitor Results

The variation of the capacitance (C) with gate voltage (VG) ranging from –5.0 V to +5.0 V with frequency 10 KHz was obtained using SUPREM -III for SiO_2 di electric and by Keithley 590 CV analyzer for TiO_2 layer as shown in **Figure 2**. The oxide capacitance (C_{ox}) is the high frequency capacitance when the device is biased for strong accumulation as shown in **Figure 2**. In case of SiO_2 dielectric it was found to be 5.202 pF, and 41.4 pF for TiO_2 as shown in **Figures 2(a)** and **2(b)** respectively.

The dielectric constant of TiO_2 (high-k) 80 was observed by calculation from the knowledge of the capacitance (C_{ox}), film thickness (d), the free space charge permittivity (ε_o) and the area of the capacitor (A) using the relation $K = Cd/\varepsilon_o A$. Thickness was measured by using stylus profiler and found to be 528 A for TiO_2 and 510 A in case of SiO_2 **Figure 3(a)**.

While in the inversion region, where the total capacitance per unit area ($C_{a,\min}$) is the series combination of the oxide capacitance and the steady minimum depletion capacitance.

The inversion capacitance per unit area was calculated

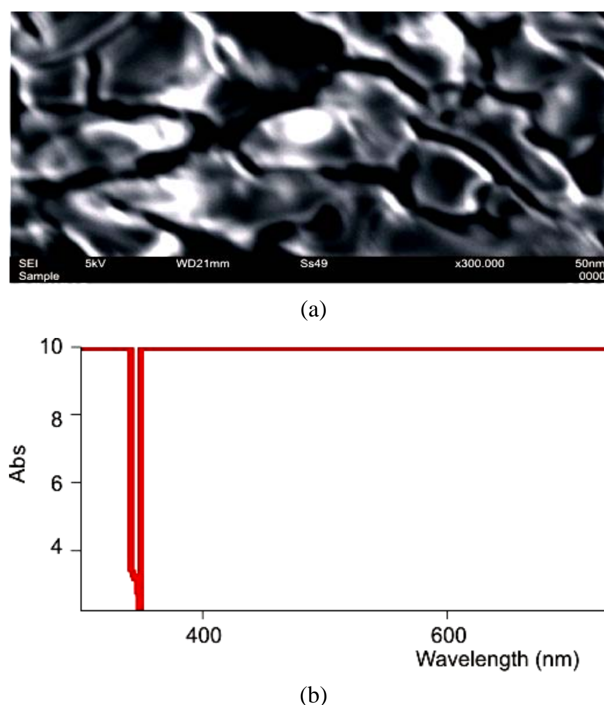


Figure 1. (a) SEM images of TiO_2 deposited on silicon wafer annealed at 550 C; (b) The absorption spectra of TiO_2 thin film.

Copyright © 2011 SciRes.

46.17 pF for TiO_2 by equation

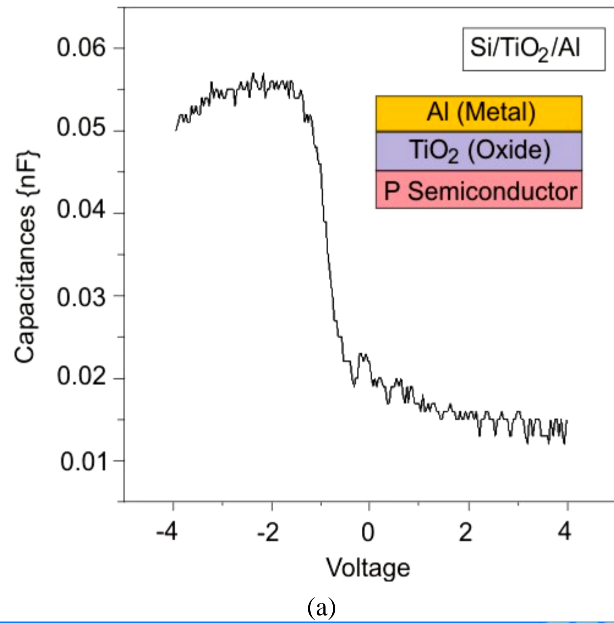
$$C_{a,\min} = \left[\frac{1}{C_{ox}} + \left(\sqrt{\frac{q\varepsilon_{Si}N_d}{2(2\varphi)}}\right)^{-1}\right]^{-1} \quad (1)$$

where C_{ox} oxide capacitance, electronic charge, ε_{Si} is the permittivity of the substrate = 11.7 × 8.85 × 10^{-14}, N_d is density of carrier concentration in the doped substrate, ni is carrier concentration in intrinsic semiconductor.

While in the inversion region, where the total capacitance per unit area ($C_{a,\min}$) is the series combination of the oxide capacitance and the steady minimum depletion capacitance.

The inversion capacitance per unit area was calculated 46.17 pF for TiO_2 by equation

$$C_{a,\min} = \left[\frac{1}{C_{ox}} + \left(\sqrt{\frac{q\varepsilon_{Si}N_d}{2(2\varphi)}}\right)^{-1}\right] \quad (2)$$



(a)

(b)

Figure 2. (a) C-V Characteristics of MOS capacitors at room temperature (Si/TiO_2/Al) (b) Si/SiO_2/Al C-V Characteristics of MOS capacitors at room temperature.

Copyright © 2011 SciRes.

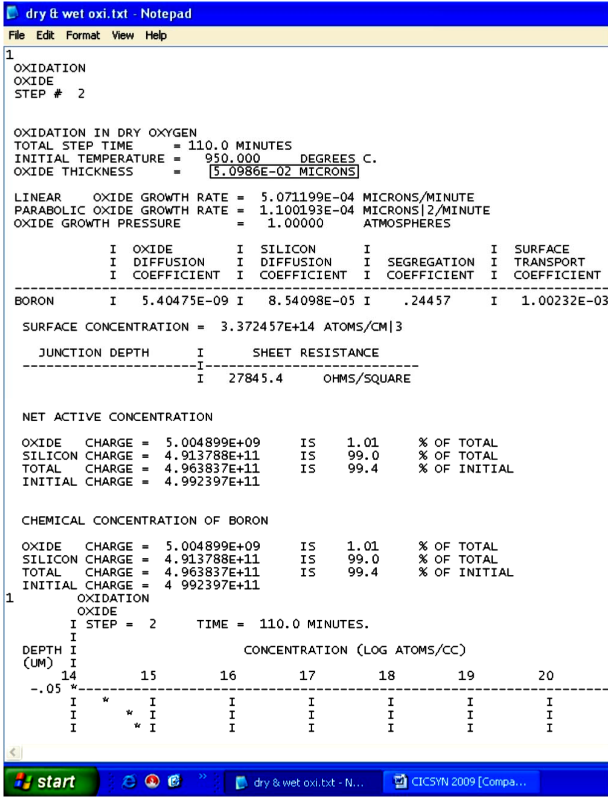


Figure 3. Oxide thickness measurements.

where C_{ox} oxide capacitance, electronic charge, ε_{Si} is the permittivity of the substrate = 11.7 × 8.85 × 10^{-14}, N_d is density of carrier concentration in the doped substrate, ni is carrier concentration in intrinsic semiconductor. Now the flat band capacitance given as

$$C_{FB} = \frac{C_{ox}\varepsilon_S A/\left(1\times10^{-4}\right)(\lambda)}{\left(1\times10^{-12}\right)\left(C_{ox}\right)\left(\varepsilon_S A\right)/\left(1\times10^{-4}\right)(\lambda)} = 39.7\text{ pF} \quad (3)$$

where λ is the extrinsic Debye length, as calculated

$$\lambda_D = \sqrt{\left(\frac{\varepsilon_S kT}{q^2 N_X}\right)} = 1.279\times10^{-5} \quad (4)$$

where kT is thermal energy at room temperature. Debye length indicates that how far an Electrical event can be sensed with in the semiconductor. The flat band capacitance C_{FB} = 39.7 pF, C_{ox} is the oxide capacitance = 41.4 pF and A is gate area = 3.13 × 10^{-6} m^2. This C_{FB} is less than the $C_{a,\min} = 46.5$ pF.

By the C-V characteristics of the capacitor the flat band voltage V_{FB} of the capacitor can be estimated. Now the threshold voltage V_{TH} for MOS-C from a C-V curve as follows.

$$V_{TH} = \left[\frac{A}{C_{ox}}\sqrt{4E_S q\left|N_{BULK}\right|\left|\varphi_B\right|} + 2\left|\varphi_b\right|\right] + V_{FB} \quad (5)$$

$= V_{TH}$ Calculated was 2V

By comparing the C-V characteristics of the capacitor with the ideal simulated C-V curves, the flat band voltage of the capacitors was calculated 2V. The oxide charge density of capacitor was calculated by

$$Q_i = C_{ox}\cdot(W_{MS} - V_{FB})/A \quad (6)$$

where C_{ox}, W_{MS}, V_{FB} and A are oxide capacitance, metal semiconductor work function difference, flat band voltage, and electrode area A. The value of oxide charge density for structure Si/TiO_2/Al (Q_{it}) 7.48 × 10^{12} and interface trap density (D_{it}) 4.32 × 10^{13} $eV^{-1}\cdot cm^{-2}$ were slightly higher than the values reported in literature [5].

The deposited TiO_2 thin presented a dielectric constant value of approximately 80, an order of magnitude higher than the obtained for SiO_2 (3.9). MOS capacitors were fabricated and it presented a leakage current density of 10 mA/cm^2, acceptable for high performance logic circuits (maximum of 100 A/cm^2) and low power circuits (10 mA/cm^2) device [8]. The leakage current density value is higher than thermally grown SiO_2 film with approximately same thickness as shown in **Figure 4**. These results indicate that TiO_2 deposited on silicon with right recipe may be strong candidate to substitute the current dielectric in CMOS fabrication.

4. Conclusions

MOS capacitors were fabricated successfully by using TiO_2 and SiO_2 as gate dielectric. The capacitor uses Si substrate with Al as another terminal. The C-V and I-V results shows that the as deposited TiO_2 Nanocrystalline films present a dielectric constant of approximately 73, with good interface quality with silicon and with leakage current density, for 1V of 10 mA/cm^2, which may be acceptable for fabricating high performance and low power logic circuits. Also the measured band gap of

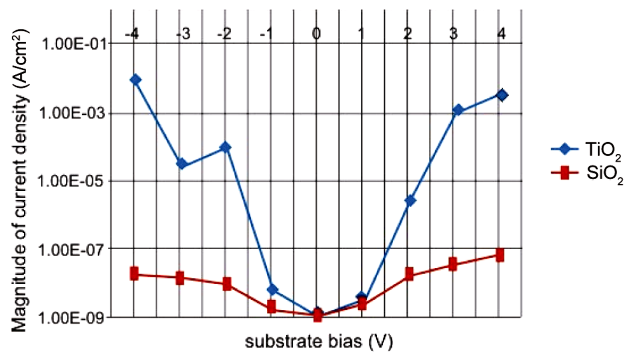


Figure 4. Gate leakage current density vs. electric field.

TiO_2 thin film was 3.6 eV may be applied in microelec tronics applications. The higher value of leakage current density and interface trap density of MOS capacitors requires further improvement in the deposition process. The measured results shows that thermally grown oxide has desirable properties in terms of leakage current and interface trap density but another obtained parameter like higher dielectric constant and small band gap are also considerable. More research is needed in case of TiO_2 to solve leakage current problem without decreasing in effective dielectric constant.

5. Acknowledgements

The author would like to thank Prof. G. Singh and Mr Virenjay M Shrivastava, both from Deaprtment of Electronics and Communication Engineering, Jaypee University of Information Technology, Solan, India, who permit to take the reference of their work related to Silicon Technology. The author also wants to thank Dr. K. S. Yadav, Sr. Scientist, CEERI, Pilani, India for many insightful discussions.

6. References

[1] S. A. Campbell, D. C. Glimer, X. C. Wang, M. Hsieh, H. S. Kim, *et al.*, "MOSFET Transistor Fabricated with High Permittivity TiO_2 Dielectric," *IEEE Transactions Electron Devices*, Vol. 44, No. 1, 1997, pp. 104-109. doi:10.1109/16.554800

[2] S. K. Samanta, S. Chatterjee, L. K. Bera and H. D. Banerjee, "Temperature Dependence of Electrical Properties of $N_2O/O_2/N_2O$ Grown Oxide on Strained SiGe," *Applied Physics Letters*, Vol. 80, No. 14, 2002, pp. 2547-2549. doi:10.1063/1.1469221

[3] S. K. Ray, D. W. Mc Neil, D. L. Gay, C. K. Marti, G. A. Armstrong and B. M. Armstrong, "Composition of $Si_{1-y}C_y$ Films Produced by Solid-Phase Epitaxy and Rapid Thermal Vapour Deposition," *Thin Solid Films*, Vol. 294, No. 1-2, 1997, pp. 149-152. doi:10.1016/S0040-6090(96)09389-3

[4] H. Iwai and H. Wong, "On the Scaling Issues and High-J Replacement of Ultrathin Gate Dielectrics for Nanoscale MOS Transistors," *Microelectronic Engineering*, Vol. 83, 2006, pp. 1867-1904.

[5] E. H. Nicollian and J. R. Brew, MOS Physics and Technology, John Wiley& Sons, New York, 1982.

[6] S. M. Sze, Physics of Semiconductor Devices, 2nd Edition, Wiley, New York, 1985.

[7] A. I. Akinwande, "IC Lab Testing," unpublished.

[8] B. G. Streetman, Solid State Electronics Devices, 1995.

[9] V. M. Srivastava, G. Singh and K. S. Yadav, "Measurement of Oxide Thickness for MOS Devices, Using Simulation of SUPREM Simulator," *International Journal of Recent Trends in Engineering*, Vol. 1, No. 4, 2009.

[10] M. Kumar and D. Kumar, "The Deposition of Nanocrystalline TiO_2 Thin Film on Silicon Using Sol-Gel Technique and its Characterization," *Microelectronic Engineering*, Vol. 87, No. 3, 2010, pp. 447-450. doi:10.1016/j.mee.2009.08.025

Copyright © 2011 SciRes.