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A Proposed Exercise to Reinforce Abstract Thinking for Upper-Division Computer and Electrical Engineering Students: Modeling a High-Speed Inverter Using Cognitive Representations and Abstract Algebra

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Abstract

In mathematics, physics, and engineering, abstract concepts are an indispensable foundation for the study and comprehension of concrete models. As concepts within these fields become increasingly detached from physical entities and more associated with mental events, thinking shifts from analytical to conceptual-abstract. Fundamental topics taken from the abstract algebra (aka: modern algebra) are unquestionably abstract. Historically, fundamental concepts taught from the abstract algebra are detached from physical reality with one exception: Boolean operations. Even so, many abstract algebra texts present Boolean operations from a purely mathematical operator perspective that is detached from physical entities. Some texts on the abstract algebra introduce logic gate circuits, but treat them as perceptual symbols. For majors of pure or applied mathematics, detachments from physical entities is not relevant. For students of Computer and Electrical Engineering (CpE/EE), mental associations of Boolean operations are essential, and one might argue that studying pure Boolean axioms are unnecessary mental abstractions. But by its nature, the CpE/EE field tends to be more mentally abstract than the other engineering disciplines. The depth of the mathematical abstractions that we teach to upper-division CpE/EE majors is certainly up for questioning.

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Keywords

Abstract Thinking, Sensorimotor Reenactment, Neurocognition, Microelectronics, Boolean Algebra

1. Introduction

In traditional computer and electrical engineering curricula, juniors must complete a course sequence in microelectronic devices and circuits (often referred to as microelectronics or electronic circuits). Depending on the academic institution, this sequence is typically two semesters or three trimesters in duration. Classic textbooks may include [1]-[4].

One of the successions of topics covered in this sequence is digital circuits, which includes a meticulous study of the dynamic switching characteristics of a basic metal-oxide semiconductor field-effect transistor (MOSFET) inverter. Prior to this juncture, students have to spend several weeks learning about the comprehensive physical structure and current-voltage characteristics of these devices, followed by how MOSFETs are biased to operate as linear amplifiers. Preceding the microelectronics sequence, CpE/EE majors traditionally complete a course in digital logic design. This is where the student learns about fundamental binary and hexadecimal arithmetic operations, the basic logic gates as mathematical operators, the various transistor-transistor logic (TTL) gate IC families, their combinational and sequential switching architectures, hardware reduction techniques, and hardware description language (e.g., VHDL, [5]).

When CpE/EE juniors are ready to study digital circuit configurations in microelectronics, they first should learn how an inverter circuit is formed using discrete components. This is initially introduced as resistor-transistor logic (RTL), followed by the complementary MOS (CMOS) configuration. It's here where students' knowledge of 1) transistor *i-v* characteristic curves; 2) TTL logic gates, gets unified. Students learn that a MOSFET must be operated in either the cutoff or triode regions if it's to function as a logic inverter. Rather than using theoretical "1 s" and "0 s" to represent logic states, students acknowledge that these binary representations are distinctive [6] objects: dc voltages measured at the gate and drain terminals of a CMOS pair. Concurrently, students establish that these voltages are restricted to the extreme and ideal limits of zero (e.g., V_{OL}) or some "full" amount (e.g., V_{OH}), and that these voltages represent MOSFET operation in the cutoff and triode regions, respectively. What's more, the student learns that the switching transition from V_{OL} to V_{OH} (and vice versa) is not instantaneous, and that there are tangible energy consequences for such an ideality. It's at this critical juncture that the student experiences sensorimotor reenactment [7] [8] and an elaboration of abstract concepts [9] [10].

Simultaneously, students learn that familiar MOSFET parameters (e.g., electron mobility μ_n and SiO_2 capacitance C_{ox}) factor into the modeling of lumped drain-source dynamic resistance and inverter switching speed. Hence, it's here where the CpE/EE begins to understand the very real switching characteristics of a discrete transistor and particularly, switching time and power dissipation consequences. These distinctives [6] are in stark contrast with what students previously assumed to be a logic-function building block embedded in an integrated circuit.

If the CpE/EE student chooses to pursue more advanced courses in the areas of digital electronic circuits or digital logic operations, they have a variety of advanced-undergraduate courses to choose from [11]-[17]. Traditionally, these courses are structured to teach 1) the analysis and design of CMOS integrated circuits; 2) architectures and implementations of data converters; 3) energy-efficient VLSI design; 4) the development of hardware for embedded microcontroller systems. As practical as these courses are to the development of computing architectures, rigorous and abstract mathematical concepts relating to the explicit physical switching dynamics of digital circuits are not covered.

Hence, the CpE/EE intent on establishing a rigorous, mathematical description of switched electronic systems might consider courses in Switching Systems and Automata, Switching Theory and Logic Design, or just Switching Theory. Texts examined on these topics tend to be presented from a rigorous, algebraic treatment [18]-[22] or from a CpE/EE or a computer science context with an introductory chapter on pure algebraic fundamentals [23]-[26]. Some exceptions are [27]-[29]. Those authors present a fairly rigorous mathematical treatment of Boolean operations and switching devices in early chapters, followed by classic and practical applications of the theory to the design of combinational and sequential architectures in later chapters.

Regardless of the presentation, the texts examined are traditionally presented to advanced graduate-level students in computer engineering, computer science, pure, or applied mathematics. It's not characteristic for *un-*

dergraduate CpE/EE's to learn how to take pure or abstract mathematical concepts and conceptualize these abstractions into something tangible (e.g., a physical digital circuit). Consequently, undergraduate CpE/EE's are not likely to cross-correlate Boolean switching abstractions with the physical properties of a transistor. The author sees the benefit of such a unified exposure at a level that is appropriate for junior CpE/EE's.

2. Conceptual Framework

Conceptual-abstract thinking consists of one's ability to effectively find connections or patterns between abstract ideas. The subsequent task is to then piece ideas together to form a coherent picture [30]. The latter portion of this sentence "… piece ideas together to form a coherent picture" inherently involves other forms of thinking (e.g., analytical and inductive thinking). Thus, when presented with generalized non-physical mathematical concepts, how effectively would a traditional CpE/EE junior form a conceptual discernment of such abstractions in the context of familiar logic structures and transistor devices?

From a classical cognitive viewpoint [31] mental abstractions are represented by a set of defining features. For instance, how does a junior CpE/EE learn to differentiate between a MOSFET and a bipolar-junction transistor (BJT)? From a black-box perspective (the abstract), both are three-terminal semiconductor devices and both can be biased to operate as a linear amplifier or as a digital switch (less abstract). In cognition research, mental perceptions of this type (e.g., digital switch) are referred to as structured representations. Without a comprehensive understanding of specific defining features like 1) device physical operation; 2) device *i*-*v* characteristics, the MOSFET and BJT would remain pure abstractions.

The MOSFET has many very specific defining features such as enhancement of a current flow channel via the application of an electric field $\mathscr{E}$, a threshold voltage V_t, an oxide capacitance C_{ox}, and an aspect ratio W/L. These features are essential for describing the concept of "MOSFET" and distinguishing it as a unique three-terminal device. The feature of a new abstract stimulus [32]-[34]—for instance, introduction to the BJT—is assessed by the student against the features of the concreteness of the MOSFET in order to determine if the BJT is an example of that category. When being introduced to the abstraction "BJT", the student might ask a series of questions, for instance: "Does the BJT have a *pn*-structure similar to that of a MOSFET? Does the BJT operate on the same principle as the MOSFET? Are BJT *i*-*v* characteristics similar to those of a MOSFET? Can the BJT be biased to operate linearly like a MOSFET?"—and so forth. The student might conclude subsequently that the BJT can be made to function like a MOSFET in amplifying signals. However, students learn that the BJT doesn't operate on the same principle as a MOSFET. Hence, the latter might come to be understood as a *characteristic* feature of *a MOSFET* but not necessarily a *defining* feature of *a transistor*. In other words, students come to understand the MOSFET is uniquely characteristic in its operation, but that it's not necessary for a transistor to operate on this principle for it to function as a linear amplifier or a digital inverter.

What about a case where there are no defining features of a device abstraction but characteristic features only? For instance, a truth table might have the characteristic features of a three-input NAND gate. But in the absence of defining features, how can one make a concrete determination that it's data from a 74LVC1G10 [35]? It could very well be three discrete CMOS inverters being fed into a 74LVC1G332three input OR gate [36]. Hence, one can conclude that abstractions may either be represented by a set of features which are characteristic, or probable of familiar examples [32]—for instance, the truth table is probably that of a three-input NAND gate. This viewpoint can be extended to mathematical abstractions. For instance, mathematical abstractions are generally presented with precise definitions, corollaries, or lemmas.

3. Purpose

An exercise is proposed to promote the association of the physical characteristics of dynamic switching in a CMOS inverter with concepts taken from the abstract algebra. The objective is to present the CpE/EE junior with a basic algebraic abstraction and through a series of fundamental steps, engage the students' abstract and inductive thinking into realizing the abstraction into the physical switching characteristics of a CMOS inverter. CMOS technology was chosen because inverter switching-speeds and steady-state response times approximate a hypothetical switch.

4. The Proposed Exercise

Consider the algebraic symbol x as being a number of the set S, such that $x \in S$. The task is to manipulate the

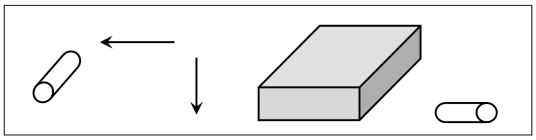
symbol x of the set S using a *binary operation*.

DEFINITION I: A binary operation on a set S is a rule that associates with each ordered pair of elements in S a unique element of S. It's a mapping which sends elements of the Cartesian product $S \times S \rightarrow S$. Because the result of performing the operation on a pair of elements of S is again an element of S, the operation is called a closed binary operation on S.

DEFINITION II: Given an element x in S, if there exists and element $y \in S$ such that $x \vee y = 1$ and $x \wedge y = 0$, then y is called a complement of x.

From these definitions perform the following tasks:

a) Arrange the following objects into a representation of the operation f: $S \rightarrow \overline{S}$, labeling which object is f. The arrows along with the other scattered shapes ought to be nicely arranged. Label the input(s) and output(s) using a variable of your choice.



b) Construct a complete truth table for the operation in *a*.

c) Use the following Boolean theorems to prove complementation: $\overline{0} = 1$; $\overline{1} = 0$

Theorem 1: $0 \wedge x = 0$; $1 \vee x = 1$

Theorem 2: $x \wedge (x \vee y) = x = x \vee (x \wedge y)$

Having completed tasks *a.* through *c.* you've focused on the Boolean complementation function f: $S \rightarrow \overline{S}$. In doing so, the operations $\overline{0} = 1$ and $\overline{1} = 0$ were treated as an *instantaneous mapping*.

As a CpE/EE major you're aware that real-life electronic circuits can perform complementation (e.g., a TTL 7404 NOT gate). Likewise, you're aware that TTL circuitry doesn't act alone; the output of one logic gate ultimately feeds into the input of another. Consequently, there are parasitic capacitances that realistically affect the speed of the complementation operation. As a result of this capacitance, V_{in} is not complemented instantaneously but involves a propagation delay t_p as illustrated in **Figure 1**. For instance, the operation $\overline{1} = 0$ involves the delay t_{pHL}, where the subscript "*pHL*" represents the propagation time it takes a complementation circuit to switch (map) a 1 (HIGH) to a 0 (LOW).

Consider now the complementation model (**Figure 2**), representing one of two possible states of the CMOS inverter of **Figure 1**:

Where $R_{P(ON)}$ is the drain-to-source resistance of Q_P during its ON state, and C represents the lumped-loading parasitic capacitance.

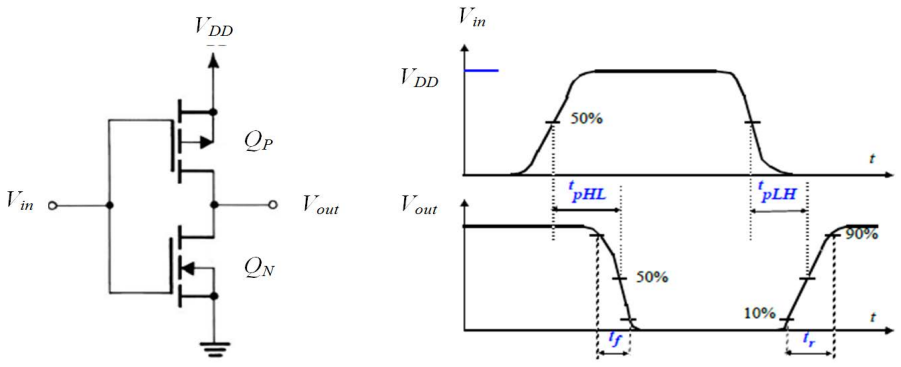


Figure 1. CMOS inverter performing the Boolean operation $\overline{0} = 1$ and $\overline{1} = 0$ (where 1 = V_{DD}). The time delays t_{pHL} and t_{pLH} brings about the notion that the switching is not instantaneous.

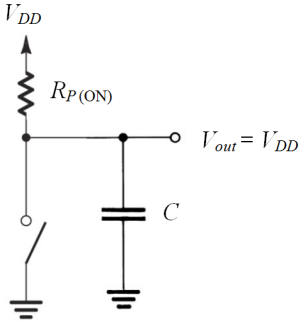


Figure 2. One possibe state of **Figure 1.**

d) Use Kirchhoff's voltage law and the initial condition $V_{out} = 0$ when $t = 0$ to show that:

$$V_{\text{out}}(t) = V_{DD}\left(1 - e^{-\frac{t}{CR_{P(\text{ON})}}}\right)$$

e) Discuss under what condition this seemingly continuous-time solution in *d.* approximates the Boolean abstraction $S \rightarrow \bar{S}$.

PAUSE

Having completed tasks *d.* and *e.* you've focused on the fact that a realistic continuous-time relationship models digital signal complementation and hence, the Boolean complementation function f: $S \rightarrow \bar{S}$. In doing so, the operations $\bar{0} = 1$ and $\bar{1} = 0$ are not considered to be an *instantaneous mapping*.

f) Consider the intrinsic drain-to-source resistance $R_{P(\text{ON})}$:

$$R_{P(\text{ON})} = \frac{1}{\left[\mu_P C_{ox}\left(\frac{W}{L}\right)\left(V_{DD} - |V_t|\right)\right]}$$

where V_t is the threshold voltage of transistor Q_P. Discuss in detail how hole mobility μ_p ($cm^2/V{\cdot}s$) and the SiO_2 capacitance C_{ox} (Farads/meter^2 or Amp-second/Volt·meter^2) affect the speed of complementation and therefore, how these two parameters limit the instantaneous complementation of the abstraction $S \rightarrow \bar{S}$.

Stop: you have completed this exercise. Wait for further instructions from the researcher.

5. Conclusions

An exercise has been proposed for the purpose of engaging students' thinking into realizing an algebraic abstraction into the physical switching characteristics of a basic CMOS inverter circuit. This exercise is meant to be used in a clinical setting with advanced-junior CpE/EE majors.

The intellectual merit of this exercise is that it promotes conceptual-abstract and deductive thinking in the CpE/EE junior via a non-traditional presentation of complementation, where mental abstractions that are nor-

mally presented in a pure and theoretical manner are represented by a set of defining features congruent with a CpE/EE's assumed knowledge level in microelectronics.

The broader impact is that of advancing the clinician's understanding of how a small and unique group of undergraduates practice abstract and deductive thinking in the process of making familiar mental associations (*i.e.*, structured representations) when presented with a pure mathematical abstraction. This work bridges cognitive theories of object concepts [6], concept elaboration [9] [10] and [31], abstract stimuli [33], and sensorimotor reenactment [7] [8] and [34] with upper-level computer and electrical engineering education.

The subsequent research ambitions of the author are to establish the validity and reliability of this exercise as an abstract reasoning assessment in a clinical setting. The objective is to dispense this exercise between the pre- and post-test administration of an established abstract and/or intelligence test battery, e.g., [37]-[40].

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