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Cost-Benefit Analysis of Computer-Aided Technology Customization Projects

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Abstract

This paper presents a methodology to assess the quantitative benefit of a computer-aided technology customization project in wafer foundries. As the dedicated semiconductor foundries transition to complete integrated circuit (IC) product development solution providers, offering customer-centric IC fabrication technology to fables customers has become crucial for foundry business model. In order to support customers' niche product-line, computer-aided design (CAD) tools are used for a rapid and cost-effective customization of foundry's core IC fabrication technology. In this paper, the efficiency and effectiveness of CAD in IC fabrication technology customization projects are evaluated by an analytical model. The data obtained by the model, clearly, shows a significant reduction in technology customization cycle time and cost by using CAD in a technology customization project compared to the conventional practice.

Keywords

Wafer Foundry, Fabless Company, IC Fabrication Technology, Technology Customization, Customer-Centric Technology, Project Management, Cost-Benefit Analysis, Technology CAD, Customer Relationship Management

1. Introduction

One of the recent trends in the microelectronics industry is the transitioning of the "pure-play," manufacturing only, dedicated wafer foundries to complete integrated circuit (IC) product development turn-key solution providers [1]-[6]. In the conventional foundry business model, a foundry develops or acquires a core IC fabrication technology to provide wafer fabrication solutions to fables IC manufacturing companies. With the advancement of mobile computing, social networking, smart-electronic products, and 5G initiatives, it has become mandatory for the IC manufacturers to offer high density products with multiple

circuit functions, what is known today as "System-on-a-Chip (SoC)" [6]. The design and manufacturing of SoCs are extremely complex due to the increased complexities of IC devices and fabrication technology at nano nodes [7] [8] [9] [10] [11]. With the increased complexities of SoC design, it is no longer cost-effective for fabless design companies to acquire and manage head counts and core competencies in-house. Thus, today's fabless companies require wafer fabrication as well as design services for rapid and cost-effective product development [1] [6]. In addition, in order to gain competitive advantage in product offering, some of the fabless companies designing novelty IC-chips require specialized IC fabrication technology. Thus, some of the specialty fabless companies require rapid customization of core foundry technology for their niche product-lines. Therefore, a cost-effective and rapid customization of foundry's core IC fabrication technology node to support the target design specifications of fabless customers is crucial for the success of these fabless companies as well as foundries [12] [13] [14] [15].

Typically, the core IC fabrication technology of a foundry at a node is customized to support a fabless customer's product-line by processing wafers in the production line [16]. Several iterations and a large number of wafers are required to process in the fabrication facility in achieving the final customer-centric IC fabrication technology. And, for a large number of fabless customers, a large number of wafers are used in the conventional technology customization process using trial-and-error experimentation. This iterative fabrication method is time consuming and expensive for customization of a core foundry technology at nano nodes [16]. Besides, processing customization wafers in the production-line causes delay in the fabrication of production wafers incurring potential loss of revenue [16]. Therefore, the foundries must adopt a cost-effective and efficient strategy to provide customer-centric wafer fabrication technology.

In today's foundry business model, a customer support team is organized to offer customer-centric technology customization, design and layout verification, characterization and modeling, packaging, and so on by acquiring relevant core competencies and tools for an efficient customer relationship management [1]-[6]. In a technology customization project, computer-aided design (CAD) tools and simulation methodology can be used for an efficient and effective customization of an IC fabrication technology as well as characterization and modeling of that customer-centric technology [17]-[24]. Though the technology CAD tools have been used in the development of new generation of IC fabrication technology to reduce the development cycle time and cost in comparison to the conventional method [16] [17] [18] [19], a quantitative cost-benefit analysis of CAD-based technology customization projects has not been reported. In this paper, an analytical model [16] [17] is used to estimate the benefit of CAD in a customer-centric IC fabrication technology customization project.

The objective of this paper is to assess the quantitative benefit of a computer-aided IC fabrication technology customization project in wafer foundries. In order to achieve this objective, first of all, an overview of the analytical model

used in this study for reduction in the technology customization cycle time and cost over the conventional method is presented. Then the simulation data obtained by the model showing the benefit of a computer-aided technology customization project is discussed. Finally, the conclusion of the study showing a cycle time reduction of above 25% with a multi-million dollar cost saving in a typical IC fabrication technology customization project compared to the conventional trial-and-error experiment is discussed.

2. Overview of the Analytical Model

Recently, an analytical model for cost-benefit analysis of a computer-aided technology development (TD) project in the semiconductor industry is reported [16]. In a new TD project, the next generation technology is developed by modifying the technology of the previous node, whereas in a technology customization project a customer-centric technology is generated from the core foundry technology at the current node. Therefore, a customer-centric IC fabrication technology customization project can be considered as a computer-aided TD project.

The model to quantify the benefits of computer-aided TD projects compared to the conventional practices is derived based on a set of realistic assumptions observed in the semiconductor industry [16]. The key assumption of the model is that the CAD tools accurately predict the device and process performance of the target fabrication technology [16] [17] [21]. In order to develop a realistic analytical model to compute the benefit of CAD-based projects over the conventional approach, a typical IC fabrication TD project is divided into three phases (ϕ):

- Phase 1, generation of initial guess process recipe;
- Phase 2, process optimization to generate process and device specifications;
- Phase 3, evaluation of process manufacturability.

The detailed model formulation is described in the published report [16] and a brief overview is presented in Section 2.1 and 2.2.

2.1. Expression to Compute Reduction in Technology Customization Cycle Time

If we consider t_{conv} as the conventional development time using only iterative method and F is the development cycle time reduction factor by a CAD-based project, then the reduction in the development cycle time, Δt in a CAD-based project compared to the conventional method is given by [16]

$$\Delta t \cong F t_{conv} . \tag{1}$$

In Equation (1), F is given by

$$F = \left(1 - \tau_{sim} / \tau_{fab}\right), \tag{2}$$

where τ_{sim} is the typical simulation time in a CAD-based virtual fabrication process of a typical customization project and τ_{fab} is the wafer fabrication time of a wafer-lot for the similar project. Typically F = 0.67 and depends on the complexities of IC fabrication technology and simulation time [16]. Equation (1) predicts a typical cycle time reduction in customization of a core foundry IC fa-

brication technology at a node of about 67% [16]. In Section 2.2, (1) is used in modeling the cost-benefit analysis of a CAD-based IC fabrication technology customization project over the conventional methodology.

2.2. Expression to Compute Reduction in Technology Customization Cost

The reduction in the IC fabrication technology customization cost, ΔC in a CAD-based project compared to the conventional method is given by [16]

$$\Delta C \geq C_{wfr}\left[F/(1-\rho)+(1+ROI)\right]\Delta n - C_{cad} \quad (3)$$

where C_{wfr} is the fabrication cost of a wafer-lot, ρ is the fraction of the conventional development wafers used in a CAD-based project, ROI is the return-on-investment from wafer sale, Δn is the reduction in the number of wafer-lots in the fab by using CAD, and C_{cad} is the cost of investment on CAD-infrastructure in the wafer foundry.

In Section 3, the reported values [16] of the model parameters in Equation (3) are used to estimate the cost-benefit analysis in a CAD-based IC fabrication technology customization project compared to the conventional approach.

3. Results and Discussions

Equation (3) is used to estimate the minimum cost saving, ΔC by CAD-based customer-centric IC fabrication technology generation at a node. Equation (3) shows that ΔC can be increased by increasing C_{wfr}, F, ρ, ROI, and Δn and by reducing C_{cad}. However, the values of C_{wfr}, ρ, and ROI are industry dependent standard. Therefore, in this study, only the effect of Δn and F on ΔC is considered. And, the reported values of the parameters used are $C_{wfr} \geq$ \$40 K, F = 0.67, $\rho \geq 0.33$, $ROI \geq 20\%$, and $C_{cad} \leq 500$ K [16] to estimate ΔC for the technology customization projects using a CAD-based methodology. The simulation data are shown in **Figure 1** and **Figure 2**.

Figure 1 shows the estimated minimum cost saving as a function of the reduction in the number, Δn of fabricated-wafers by a CAD-based project over the conventional methodology. The goal of CAD and simulation is to minimize expensive fab-experiments to generate customer-centric IC fabrication technology from the core foundry technology. It is seen from **Figure 1** that ΔC decreases with the increase in C_{cad} and for 100, 250, and 500 K values of C_{cad}, the values of Δn required to breakeven capital expenses are 1.1, 2.8, and 5.7, respectively. Thus, for higher values of capital expenses, the simulation process must reduce a large number of fab-experiment for cost-saving by CAD-based technology customization projects. Typically, C_{cad} < \$300 K [16] for the initial acquisition and implementation of CAD infrastructure which are used in ongoing multiple development projects within the wafer foundry. Therefore, in this study, C_{cad} = \$250 K is considered as the typical cost of CAD infrastructure in the company. Then **Figure 1** shows that to breakeven the capital investment on CAD, only a reduction of at least three wafer-lots ($\Delta n \geq 3$) is required by a CAD-based tech-

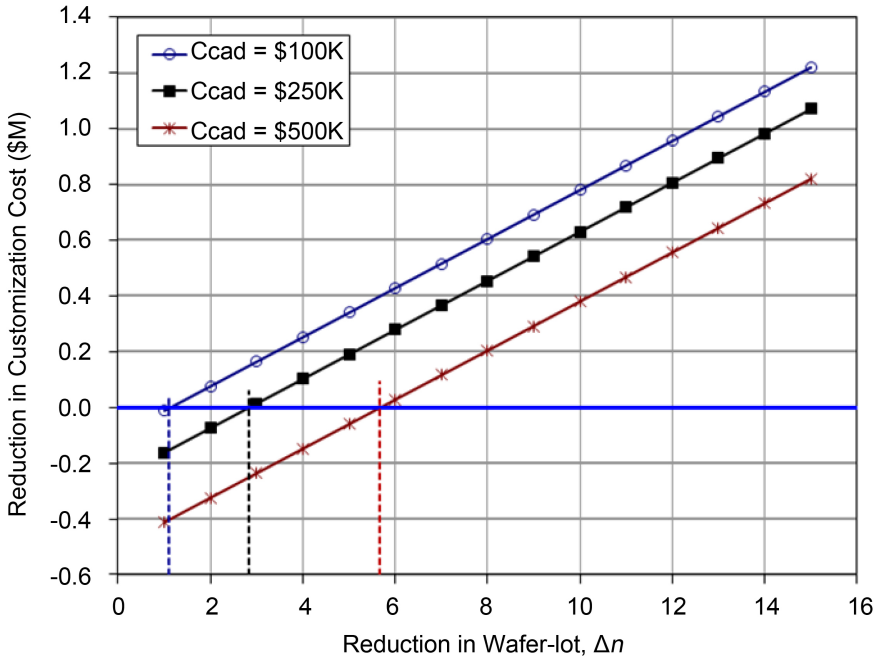

Figure 1. Minimum cost saving, ΔC as a function of the reduction in wafer-lot fabrication, Δn for different CAD-infrastructure expenses, C_{cad}. The data are obtained by (3) using C_{wfr} = \$40 K, $F = 0.67$, $\rho = 0.33$, and $ROI \geq 20\%$.

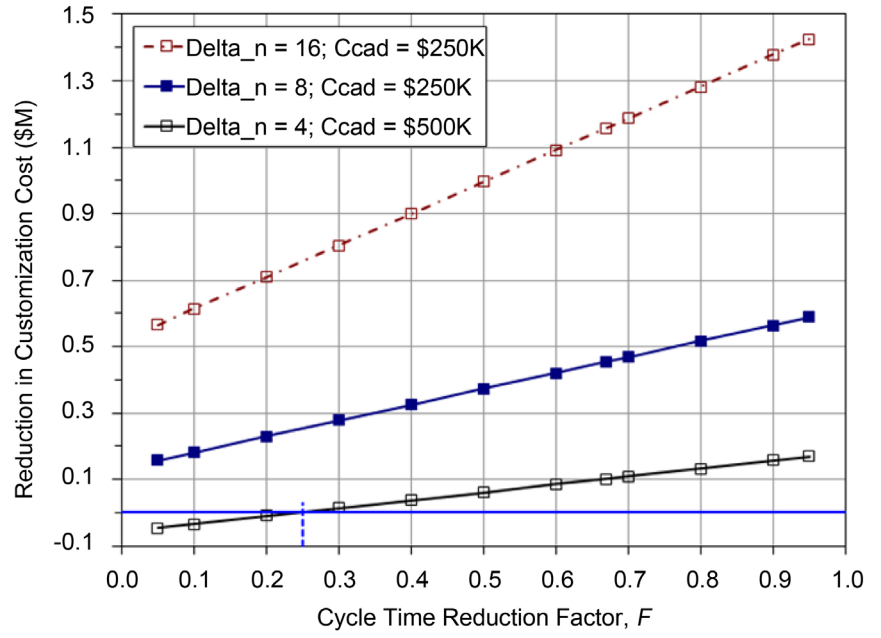

Figure 2. Minimum cost saving, ΔC as a function of cycle-time reduction factor, F with Δn as a third parameter. The data are obtained by (3) using C_{wfr} = \$40 K, $\rho = 0.33$, and $ROI \geq 20\%$ and C_{cad} = 250 K. Plots show that $F \geq 0.25$ for cost saving, $\Delta C > 0$ by a CAD-base technology customization project. In figure legends "Delta-n" represent Δn.

nology customization project. In reality, more than 10 wafer-lots are saved using a simulation project compared to 100% experiment-based project [16]. Therefore, Figure 1 shows that in a CAD-based technology customization project a

cost saving of more than \$600 K can be achieved compared to the same project using the conventional method. And, considering a large number of fabless customers requiring customer-centric technology, over multi-million dolar total cost saving can be achieved by CAD-based technology customization compared to the conventional iterative wafer processing in the fab. Thus, C_{cad} = 250 K is used in assessing the cost-saving as a function of cycle-time reduction factor, F for different values of $\Delta n > 3$ as shown in **Figure 2**.

It is observed from **Figure 2** that for $\Delta C \geq 0$ and $\Delta n = 4$, $F \geq 0.25$. In **Figure 1**, the reported typical value of $F = 0.67$ is used to compute ΔC. **Figure 2** shows that for the typical value of C_{cad} = 250 K, the lower limit of F is about 0.25. Thus, F is valid over a wide range, $0.25 \leq F \leq 0.67$ and therefore, the worst case reduction in technology customization cycle time by a CAD-based project is about 25% compared to that using the conventional method. This implies that any increase in the simulation time, τ_{sim} [Equation (2)] due to a potential increase in the complexities of device and fabrication technology still offers more than 25% cycle-time reduction by a CAD-based project over the conventional iterative fab-experiments. Typically, after the initial investment and implementation of CAD-infrastructure, C_{cad} represents the maintenance cost only which is less than \$100 K annually [16]. Therefore, the range of the values of F is more flexible for τ_{sim} variation than that shown in **Figure 2**. Thus, the analytical model shows a rapid customer-centric IC-fabrication technology generation from a core foundry IC fabrication technology along with multi-million dollar cost-saving using a CAD-based methodology compared to the conventional expensive and time consuming trial-and-error wafer-fabrication.

4. Conclusion

Recently, the semiconductor wafer foundries are transitioning to a complete IC product development turn-key solution providers. In this model, it is extremely critical for foundries to provide customer-centric IC fabrication technology to their fabless customers. For an efficient and effective customization of a foundry's core IC fabrication technology, a CAD-based customization method is crucial. This paper presents a methodology to estimate the cost-benefit of such a CAD-based project management. The data obtained by the analytical model show a reduction in technology customization cycle time over 25% with a multi-million dollar cost-saving in comparison to the conventional practice of wafer fabrication in the foundry production-line. Thus, this paper offers project managers a quantitative methodology for cost-benefit analysis of an IC fabrication technology customization project in a wafer foundry for successful planning and execution of the project.

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