Materials Sciences and Application, **2011, 2, 993-999**
doi:10.4236/msa.2011.28134 Published Online August 2011 (http://www.SciRP.org/journal/msa)

Scientific Research

Investigation of Electrical Transport in PECVD Grown a-SiC$_x$:H Thin Film

Orhan Özdemir*, Kutsal Bozkurt, Kubilay Kutlu

Physics Department, Yildiz Technical University, Esenler/İstanbul, Turkey.
Email: *ozdemir@yildiz.edu.tr

Received April 8th, 2011; revised April 28th, 2011; accepted May 11th, 2011.

ABSTRACT

Dc/ac transport characteristic of PECVD grown hydrogenated amorphous silicon carbide (a-SiC$_x$:H) thin film was investigated in MIS (metal/insulator/semiconductor) structure by dc current/voltage (I/V) at different temperature (T), ac admittance vs. temperature at constant gate bias voltages and deep level transient spectroscopy (DLTS), respectively. According to I-V-T analysis, two main regimes exhibited. At low electric field, apparent Ohm's law dominated with Arrhenius type thermal activation energy (E_A) around 0.4 eV in both forward and reverse directions. At high field, on the contrary, space charge limited (SCL) current mechanism was eventual. The current transport mechanisms and its temperature/frequency dependence were interpreted by a thermally activated hopping processes across the localized states within a-SiC$_x$:H thin film since 0.4 eV as E_A was not high enough for intrinsic band conduction. Instead, transport of charge carriers took place in two steps; first a carrier is thermally excited to an empty energy level from an occupied state then multi-step tunnelling or hopping starts over. Therefore, the two steps mechanisms manifested as single activation energy, differing only through capture cross sections. In turn, two steps in capacitance together with conductance peaks in C-(G)-T while convoluted DLTS signal associated with such events in the measurements.

Keywords: *A-SiC$_x$:H, Dc/Ac Transport, Conduction Mechanisms, Apparent Activation Energy, Admittance, DLTS, Hopping*

1. Introduction

Both tunability of energy band gap from 1.9 - 3.2 eV with different carbon content (*x*) [1] and n-/p- type dopability by appropriate doping gases [1] lead an opportunity of amorphous hydrogenated silicon carbide (a-SiC$_x$:H) films to be used in solar cell technology and light-emitting diodes (LED's). In former, owing to the excellent surface passivation of crystalline silicon (c-Si) and large area deposition capability, a-SiC$_x$:H films are used in silicon solar cell applications. Recent works have shown that Si-rich a-SiC$_x$:H films with low power regime possesses brilliant electronic surface passivation in silicon heterojunction solar cells [2-8]. Improvement in silicon heterojunction solar cells to achieve high conversion efficiency (greater than 22%) [9,10] is possible by electronic surface passivation, *i.e.*, low recombination loss of photo-generated carriers.

Contrary to that LED's applications require bipolar carrier transport and efficient recombination rate of injected electron-hole pairs within the intrinsic layer of a-SiC$_x$:H films. Each phenomena, transport and/or recombination issues, limits the efficiency of LED's in which carriers might flow through either localized or extended states via hopping [11] in a-SiC$_x$:H films. Within this context, since carrier injection issue and nature/amount of localized density of states (DOS) distribution are tightly bound with each other, d.c. and a.c. conductivities seem to be convenient techniques for characterizing electrical features of the a-SiC$_x$:H film within a metal/insulator/semiconductor structure. In other words, d.c. current/voltage (I/V) at different temperatures, a.c. admittance ($Y = G + j\omega C$, G = conductance, C = capacitance, and ω = frequency) versus bias voltage and/or temperature at constant gate bias voltages and deep level transient spectroscopy (DLTS) are proper techniques to employ for investigating electrical features of a-SiC$_x$:H film in MIS structure.

2. Film Fabrication and Experimental Detail

a-SiC$_x$:H film studied in this work was grown, under the mixture of 30 ccm SiH_4 (silane) and 30 ccm C_2H_4 (ethylene), by 13.56 MHz plasma enhanced chemical vapor

Copyright © 2011 SciRes.

deposition (PECVD) technique where the deposition parameters were held at 0.1 Torr pressure, 250˚C substrate temperature, 60 mW/cm^2 ac RF power. p- type silicon wafer with resistivity of 10 Ω cm, and corning 7059 glass plates were used as substrates for electrical and optical analyses.

A profiler (Ambios XP-2) was used to measure the film thickness as 125 nm. UV- VIS spectroscopy (Perkin Elmer Lambda 2S) supplied the optical energy gap and refractive index as 2.67 eV and 2.15, respectively, d.c and ac electrical measurements were performed by an electrometer (Keithley 6517), an impedance analyser (HP 4192 A), and DLTS (Semilab DLS 82 E), respectively.

3. Results and Discussions

3.1. d.c. Properties Through Resistivity Measurements

Electrical resistivity of the film has been obtained in sandwich configuration from the ohmic region of the dc current (I) vs d.c voltage (V) and depicted in **Figure 1 (a)**. Apart from the existence of the ohmic region in forward current, another conduction mechanisms, depending on the magnitude of bias voltage, are eventual. Along the I-V curve, ohmic region, is followed by a superlinear region. Forward current is proportional to power of bias voltage; *i.e.*, $I \propto V^p$ where p inversely varies with temperature. It is located between 2.2 and 3.4 for the exploited temperature interval of 295 - 370 K. This power law dependence of the current on the applied voltage beyond a critical value indicates a space charge limitation.

Conductivity, evaluated from the ohmic region

$$\left(\sigma \approx \exp\left[-\frac{E_A}{kT}\right]\right),$$

follows an Arrhenius behavior with a single activation energy (E_A) of about 0.4 eV within the studied temperature interval (see **Figure 1(b)**). Typically, the ohmic region is attributed to an intrinsic thermal excitation of free carriers. However, for a wide energy gap insulator at moderate temperatures as in this case, it is doubtful. Rather, a hopping type conduction through the localized states is reasonable owing to the presence of large amount of distributed localized states on either side of the Fermi level (E_F). In other words, the electrical conduction take place in two steps; in first, thermal excitation of carrier from E_F to the relevant edge of the extended state band, and then hopping across the localized states whose density strongly increases (exponential or Gauss like) away from E_F towards the band edges. That is, the thermal excitation allows carriers to populate the states at energies distant from E_F and thus strongly increases the number of neighboring states accessible for hopping (lower hopping distance and higher hopping rate) [12-16].

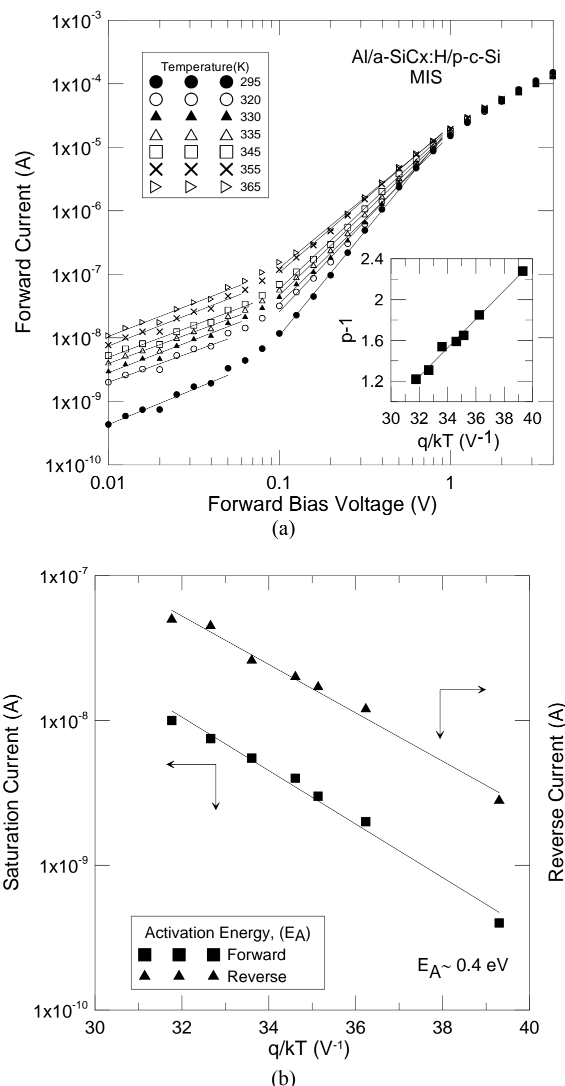


Figure 1. (a) Forward current- forward bias voltage characteristics of a Al/a-SiC$_x$:H/p-c-Si MIS structure at studied temperature interval of 295 - 365 K. Two main conduction regimes, ohmic and space-charge-limited (SCL), are clearly observed. The inset of the figure reinforces the existence of SCL mechanism, (b) Temperature dependence of saturation current in forward direction and reverse current at a bias of 0.1 V. The activation energy, determined via the slope of the variation, was determined at the proximity of 0.4 eV in both directions.

Within this context, the large majority of transport occurs within a relatively thin energy interval whose median value is defined as the so called average transport energy E_t: $\Delta E_t = E_t - E_F$ (or $E_F - E_t$) appears as the measured activation energy (E_A) from the Arrhenius plot (**Figure 1-b**). The medium activation energy value of 0.4

eV for dc conductivity is neither high enough for intrinsic band conduction nor low enough for hopping transport across the uniformly distributed deep states.

3.2. a.c. Properties Through Admittance Measurements

Admittance measurements on the MIS structure (Al/a-SiC$_x$:H film/p-Si/Al) were performed as a function of dc gate voltage (V_G), temperature (T) and frequency (ω) of the gate voltage modulation to carry out the dielectric behavior of the a-SiC$_x$:H film.

3.2.1. Capacitance (Conductance)- Bias Voltage Variation

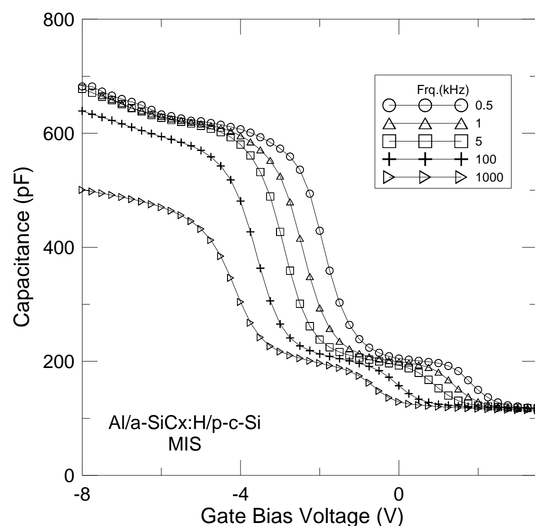
Figure 2 exhibits the strong ω dispersion of both measured parallel capacitance (C_m) and conductance (G_m/ω) as a function of V_G. Apart from the frequency dependence, C_m converges to a voltage independent value of about 500 pF at the negative side of V_G under high frequency. This is relevant to strong accumulation in the silicon interface and corresponds to the film geometrical capacitance

$$C_f = \frac{\varepsilon_{a-SiC_x:H} A}{d_I}$$

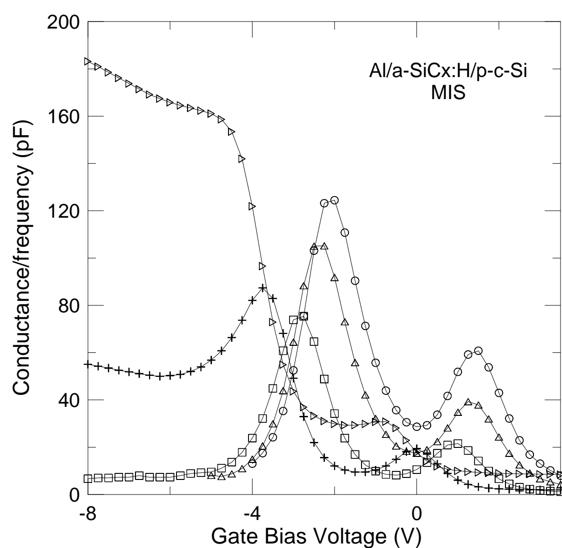
where film thickness d_I was measured separately as 125 nm by both mechanical profiler and UV-Visible transmittance within mutual checking [16]. C_f value of 500 pF supplies the film dielectric constant as $\varepsilon_{a-SiCx:H} \approx 4.6$ for an electrode area A of 1.54×10^{-2} cm^{-2}.

The frequency dependence of the admittance along the accumulation bias voltage is originated from the modulation of injected charges, Q_t, residing interior of the a-SiC$_x$:H film. Because, under an accumulating type V_G, the stored holes at the a-SiC$_x$:H/p-c-Si interface are injected by multi-tunneling (or hopping) through localized states due to the direction of applied electric field. Therefore, a charge modulation δQ_G on the front metal electrode induces equal but opposite amount of charge modulation δQ_s, constitituing by injected charge modulation, δQ_t, interface state charges, δQ_{ss}, and accumulated charges, δQ_A, respectively. Both δQ_{ss} and δQ_A are away a distance of d_I from the interface, whereas δQ_t is located at an average distance $d_I - x_t$ with x_t being the average distance of interior injected charges from the p-c-Si side. Hence, the measured capacitance is "build" by these charges due to the moment arm (centroid of charges) as:

$$C = \frac{\varepsilon A}{\langle d \rangle}, \quad \langle d \rangle = \frac{(d_I - x_t)\delta Q_t + (\delta Q_{ss} + \delta Q_A) d_I}{\delta Q_t + \delta Q_{ss} + \delta Q_A} \qquad (1)$$



(a)



(b)

Figure 2. Capacitance (a), conductance/frequency (b) variations as a function of gate bias voltage at room temperature under various modulation frequencies for Al/a-SiC$_x$: H/p-c-Si MIS structure.

Increase in ac modulation causes reduction in Q_t, in turn $\langle d \rangle$ enlarges, leading to a reduction in capacitance from geometric value to the first minimum; forming a first step in C-V curve (see **Figure 2(a)**). The following section is devoted to figure out a second step in the measurement.

The amount of injected charges within the a-SiC$_x$:H film bend the silicon energy bands, ψ_s. Equality of ψ_s to zero $(\psi_s = 0)$ corresponds to compensation of injected charges and marks the boundary between end of accumulation regime and onset in depletion regime. In other words, conventional MOS analysis predicts the depletion regime subsequently after the accumulation

Copyright © 2011 SciRes.

one as V_G is swept towards more positive side. Additionally, the involvement of charges, either in a-SiC$_x$:H or a-SiC$_x$:H/p-c-Si interface, modify the shape of C-V curve. Manifestation of this issue in C-V curves appears as steps with frequency dependent manners. The first step is interpreted as the modulation of injected charges over the geometric film capacitance under a condition of $\psi_s \le 0$. For $\psi_s \ge 0$, on the other side, δQ_G comprises of δQ_{ss} and δQ_D where δQ_D is depletion charges, located a distance of d_I+d_D with

$$d_D = \sqrt{\frac{2\varepsilon_{si}\psi_s}{qN_A}}$$

q is elementary charge and N_A denotes doping concentration of c-Si. Consequently, $\langle d \rangle$ in this case would be expressed by

$$\langle d \rangle = \frac{\delta Q_{ss} d + \delta Q_D \left(d + d_D\right)}{\delta Q_{ss} + \delta Q_D}. \quad (2)$$

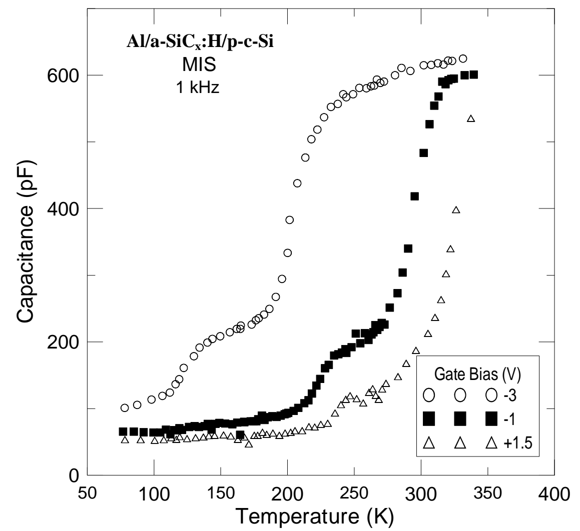
At low frequency, δQ_{ss} is much more smaller than δQ_D and hence $\langle d \rangle \approx d_I$. Therefore, moment arm shifts from $d_I - x_t$ to d_I. For high frequency where $\delta Q_{ss} \ll \delta Q_D$, the ac modulation exclusively occurs at the silicon depletion edge so d_I moves to $d_I + d_D$. Consequently, two steps in capacitance are formed in C-V analysis.

3.2.2. Capacitance (Conductance)- Temperature Variation

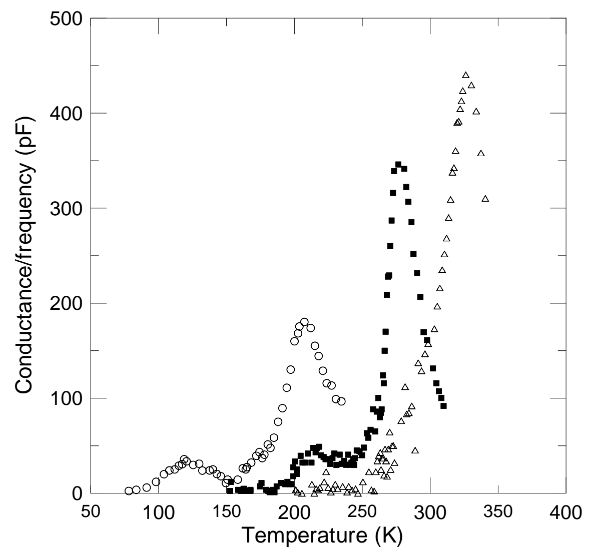
Temperature dependence of admittance measurements (C_m and G_m/ω) under predetermined dc gate biases and small amplitude ac excitation frequency of 1 kHz for a-SiC$_x$:H film in MIS structure is illustrated in **Figures 3 a-b** and **4 a-b**, respectively. The mechanisms behind the capacitance steps are investigated through frequency dependence; examples for a-SiC$_x$:H film is given in **Figure 4(a-b)** at the gate bias of −1 V corresponding to depletion/weak inversion regime. Frequency dependent capacitance steps of C_m as well as G_m/ω peaks are distinguished within 200 - 280 K and 280-340 K temperature intervals. These temperature activated processes are Arrhenius type (see **Figure 5**). It is worth to note that determined E_A from the steps in capacitance remains at the same energy values but appear at different temperature interval in C-T scans, as shown in **Figure 4**. Moreover, at a temperature range following the second step, frequency dependent capacitance plateau arises for a-SiC$_x$:H film and designates the film geometric capacitances at high frequency as in C-V curve.

Variation of capacitance as a function of bias/temperature could be interpreted equivalently with capture/emission time,

$$\tau \left(= e^{\frac{q\psi_s}{kT}} \right):$$



(a)

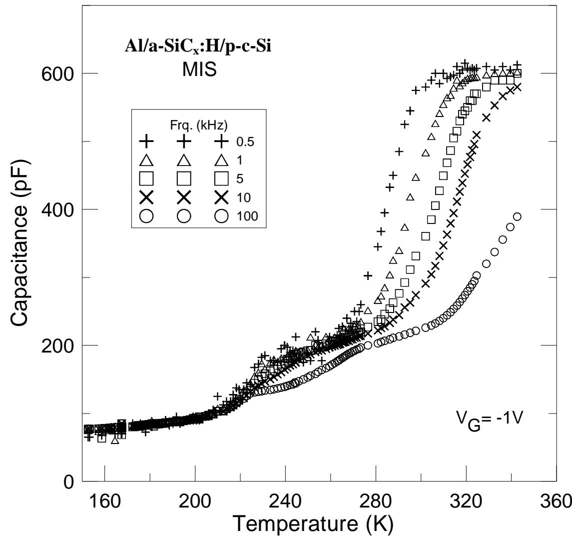


(b)

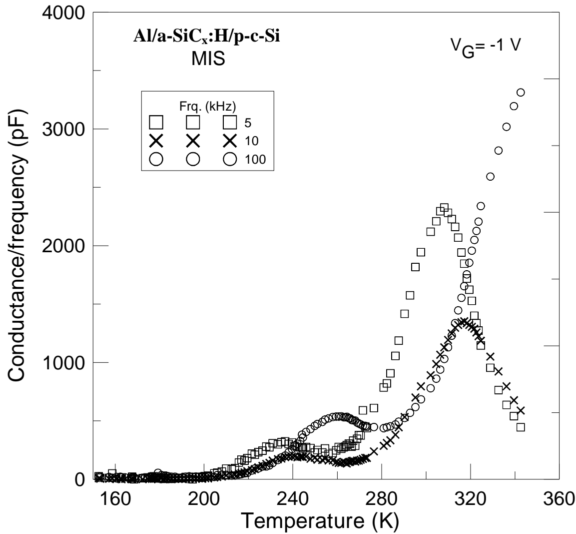
Figure 3. Capacitance (a), conductance/frequency (b) vs. temperature scans at various gate bias voltages (-3, -1 and +1.5 V) at 1 kHz meauring frequency.

changing gate bias (temperature) towards accumulating bias regime (high temperature zone) leads to a decrease in ψ_s, hence only fast states could follow the ac modulation. Increasing the gate bias values towards positive side, the flat band voltage $\left(\psi_s \approx 0\right)$ is first reached and then the depleting gate bias regime starts. Further increase in gate bias causes the increase of ψ_s (>0) in turn widening the depletion width. This phenomenon appears as steps in C_m and peaks in G_m/ω. These steps might be correlated as follows: first, the trapped holes in a-SiC$_x$:H film hop or multi-tunnel toward interface states, then emitted from the interface states to the valance band edge of c-Si substrate. Hence, two characteristic times

Copyright © 2011 SciRes.



(a)



(b)

Figure 4. Capacitance (a), conductance/frequency (b) vs. temperature curves at V_G = –1 V for various measuring frequency.

τ_α and τ_β are associated with such events: a release time τ_α of trapped charges from the interface states to the valance band edge by the well known Shockley-Read-Hall statistics (that is a single mechanism) and τ_β release time of trapped charges within the film to the valance band edge via interface states (that is, a two step mechanism) [18];

$$\tau_\alpha = \left(\sigma_p v_{th} p_e\right)^{-1} \exp\left(q\psi_s \big/ kT \right),$$

$$\tau_\beta = \left(\sigma_p v_{th} p_e \exp\left[-\frac{2x_t}{\lambda} \right] \right)^{-1} \exp\left(q\psi_s / kT \right) \quad (3)$$

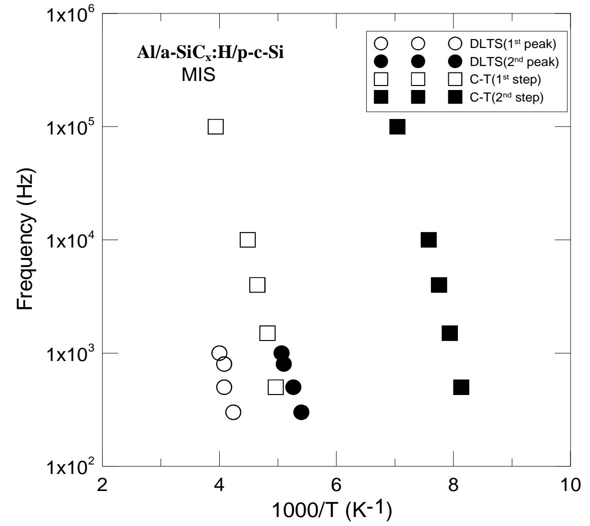


Figure 5. Activation energies obtained from the frequency of conductance/DLTS peak vs. temperature curves at V_G = –1 V (black/filled rectangle) and –3 V (open/filled circle), respectively.

where p_e = the free carrier concentration in c-Si, v_{th} = thermal velocity of carriers, σ_p = capture cross section of trap and λ = localization length.

3.3. DLTS Measurement

A small signal (or energy resolved) DLTS measurement is performed and depicted in **Figure 6** for a-SiC$_x$:H film in MIS structure at hand. In the measurement, a small injection pulse is superimposed on a quiscent voltage ($U_{quiscent}$) which defines the position of the Fermi level at the surface of p-c-Si. Moreover, the measurement involves the periodic application of small filling voltage (U_{fill}) of width t_p to charge/discharge the interface traps around E_F with majority carriers in depletion regime. The capacitance transient of DLTS signal of the present system is expressed as [19]

$$S = \delta C(0) \frac{1 - \exp\left[-\frac{T_p}{2\tau} \right]}{T_p} \left\{ \tau \exp\left(-\frac{t_d}{\tau} \right) - \left(\tau - t_g \right) \exp\left(-\frac{T_p - 2t_p}{2\tau} \right) \right\} \quad (4)$$

where T_p is the period of applied trap filling pulse, $t_g = t_p + t_d$ with $t_d = T_p/20$ and τ is the relaxation time.

As shown in **Figure 6**, convoluted DLTS signal of peaks become to separate as V_G increases. Remarkably, from the peak of the temperature position, Arrhenius plot is drawn to determine E_A while height of the signal serves to evaluate the interface state density. Similar to C-T scans, two series of peaks lead to same E_A (see **Figure 5**), differing through only capture cross sections. Also, movement of peaks as bias changes are the signature of interface traps rather than bulk nature, reinforcing the above analysis.

Copyright © 2011 SciRes.

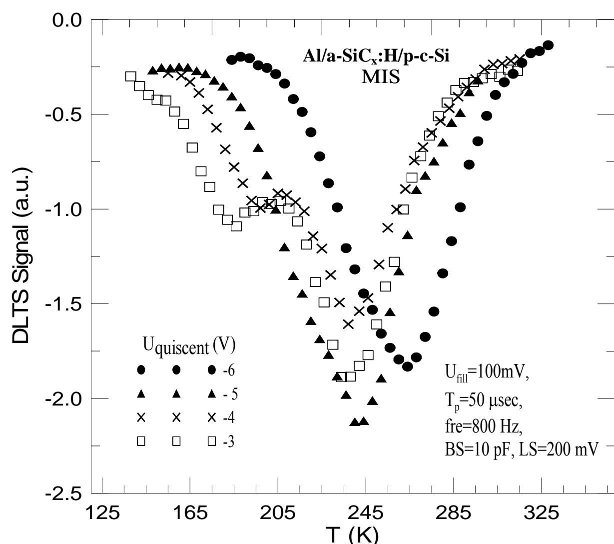


Figure 6. DLTS spectra of Al/a-SiCx:H/p-c-Si MIS strcuture at predetermined gate bias voltages.

4. Conclusions

Apart from I-V-T analysis, C-T-ω/DLTS measurements have stated that the obtained E_A was the same for the first and second steps/peaks, respectively. This was interpreted as the traps lying on the same energy value at the interface around the Fermi level leading to the same activation energy and appearing at shifted along the 1/T axis.

REFERENCES

[1] J. Kanicki, "Amorphous and Microcrystalline Semiconductor Devices," Materials and Device Physics, Vol. 2, Artech House, London, 1992.

[2] M. Vetter, C. Voz, R. Ferre, I. Martı´n, A. Orpella, J. Puigdollers, J. Andreu and R. Alcubilla, "Electronic Properties of Intrinsic and Doped Amorphous Silicon Carbide Films," *Thin Solid Films*, Vol. 511-512, 26 July 2006, pp. 290-294.

[3] S. Ogawa, M. Okabe, Y. Ikeda, T. Itoh, N. Yoshida and S. Nonomura, "Applications of Microcrystalline Hydrogenated Cubic Silicon Carbide for Amorphous Silicon Thin Film Solar Cells," *Thin Solid Films*, Vol. 516, No. 5, 2008, pp. 740-742 doi:10.1016/j.tsf.2007.06.047

[4] S. J. Lee, S. H. Kim, D. W. Kim, K. H. Kim, B. K. Kim and J. Jang, "Effect of Hydrogen Plasma Passivation on Performance of HIT Solar Cells," *Solar Energy Materials & Solar Cells*, Vol. 95, No. 1, January 2011, pp. 81-83. doi:10.1016/j.solmat.2010.05.015

[5] M. Vetter, I. Martı´n, R. Ferre, M. Garı´n and R. Alcubilla, "Crystalline Silicon Surface Passivation by Amorphous Silicon Carbide Films," *Solar Energy Materials & Solar Cells*, Vol. 91, No. 2-3, 23 January 2007, pp. 174-179. doi:10.1016/j.solmat.2006.08.004

[6] Z. Hu, X. B. Liao, H. W. Diao, Y. Cai, S. B. Zhang, E. Fortunato and R. Martins, "Hydrogenated P-Type Nanocrystalline Silicon in Amorphous Silicon Solar Cells," *Journal of Non-Crystalline Solids*, Vol. 352, No. 9-20, 15 June 2006, pp. 1900-1903. doi:10.1016/j.jnoncrysol.2006.02.010

[7] S. Y. Myong, S. S. Kim and K. S. Lim, "Improvement of Pin-type Amorphous Silicon Solar Cell Performance by Employing Double Silicon-Carbide Player Structure," *Journal of Applied Physics*, Vol. 95, No. 3, 1 February 2004, pp. 1525-1530. doi:10.1063/1.1639140

[8] R. Ferre, I. Martín, M. Vetter, M. Garín and R. Alcubilla, "Effect of Amorphous Silicon Carbide Layer Thickness on the Passivation Quality of Crystalline Silicon Surface," *Applied Physics Letters*, Vol. 87, No. 20, November 2005, pp. 109-202. doi:10.1063/1.2130530

[9] H. Fujiwara and M. Kondo, "Effects of A-Si:H Layer Thicknesses on the Performance of A-Si:H/c-Si Heterojunction Solar Cells," *Journal of Applied Physics*, Vol. 101, No. 5, 2007, pp. 054516-054525. doi:10.1063/1.2559975

[10] H. Fujiwara and M. Kondo, "Impact of Epitaxial Growth at the Heterointerface of A-Si:H/c-Si Solar Cells," *Applied Physics Letters*, Vol. 90, No. 1, January 2007, pp. 013503-013506. doi:10.1063/1.2426900

[11] K. Sel, B. Akaoğlu, İ. Atilgan and B. Katircioğlu, "Effects of Tail States on the Conduction Mechanisms in Silicon Carbide Thin Films with High Carbon Content," *Solid-State Electronics*, Vol. 57, No. 1, March 2011, pp 1-8. doi:10.1016/j.sse.2010.12.010

[12] M. Grünewald, P. Thomas and D. Würtz," Simple Calculation of the Hopping Conductivity for an Exponential Band Tail," *Physics States Solid* (*B*), Vol. 94, No.1, July 79, pp. K1-K4.

[13] S. Nespurer, O. Zmeskal and F. Schauer, "An Ohmic contact Test Using the Activation Energy of Steady-State Space-Charge-Limited Current," *Physica Status Solidi (B)*, Vol. 85, No. 2, 1984, pp. 619-625. doi:10.1002/pssa.2210850238

[14] A. Bozhko, M. Shupegin and T. Takagi, "Space-charge-limited Current in Hydrogenated Amorphous Carbon Films Containing Silicon and Oxygen," *Diamond and Related. Materials*, Vol. 11, No. 10, October 2002, pp. 1753-1759. doi:10.1016/S0925-9635(02)00156-5

[15] C. Godet, "Hopping Model for Charge Transport in Amorphous Carbon," *Philosophical Magazine Part B*, Vol. 81, No. 2, February 2001, pp. 205-222. doi:10.1080/13642810108216536

[16] O. Özdemir, M. Anutgan, T. Aliyeva-Anutgan, İ. Atılgan and B. Katırcıoğlu, "Electrical Transport Mechanism in Boron Nitride Thin Film," *Journal of Non-Crystalline Solids*, Vol. 355, No. 14-15, 1 June 2009, pp. 851-859. doi:10.1016/j.jnoncrysol.2009.04.034

[17] O. Özdemir, İ. Atılgan, B. Akaoğlu, K. Sel and B. Katırcıoğlu, "Frequency Dependence of Conductivity in Intrinsic Amorphous Silicon Carbide Film, Assessed Through Admittance Measurement of Metal Insulator Semiconductor Structure," *Thin Solid Films*, Vol. 497, No. 1-2, 21 February 2006, pp. 149-156. doi:10.1016/j.tsf.2005.10.065

[18] O. Özdemir, S. Özder, İ. Atılgan and B. Katırcıoğlu, "Admittance Analyis of an MIS Structure Made with PECVD Deposited A-SiN_x:H Films," *Journal of Non-Crystalline Solids*, Vol. 249, No. 2-3, 2 July 1999, pp. 131-144

[19] S. Özder, "Investigation of SiO2/p-Si Structure by DLTS and Various Admittance Techniques," Ph.D. Dissertation, Middle East Technical University, Ankara, 1994.

Copyright © 2011 SciRes.