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The Charge Storage of Doubly Stacked Nanocrystalline-Si based Metal Insulator Semiconductor Memory Structure

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ABSTRACT

Doubly stacked nanocrystalline-Si (nc-Si) based metal insulator semiconductor memory structure was fabricated by plasma enhanced chemical vapor deposition. Capacitance-Voltage (C-V) and capacitance-time (C-t) measurements were used to investigate electron tunnel, storage and discharging characteristic. The C-V results show that the flatband voltage increases at first, then decreases and finally increases, exhibiting a clear deep at gate voltage of 9 V. The decreasing of flatband voltage at moderate programming bias is attributed to the transfer of electrons from the lower nc-Si layer to the upper nc-Si layer. The C-t measurement results show that the charges transfer in the structure strongly depends on the hold time and the flatband voltage decreases markedly with increasing the hold time.

Keywords: nc-Si dots; Capacitance-Voltage Measurement; Storage

1. Introduction

In recent years, silicon nanostructures have attracted enormous attentions.[1-5] Particularly, metal-insulator-semiconductor (MIS) structures based on silicon quantum dots are widely studied for their new physical phenomena as well as their potential applications in future memory device. The first nanocrystals based MIS memory structure was put forward by Tiwari et al., where Si nanocrystals were used as storage nodes.[1] Compared to the conventional nonvolatile memories with polycrystalline silicon or silicon nitride floating gate as the charge storage layer, a nanocrystal based memory has been suggested as one of the key items for increasing flash memory stability and decreasing the node size for higher information density. In such memory device, the Si nanocrystals are sufficiently isolated from each other by insulator. Hence, the electrons are localized in the nanocrystals and a local leakage path would not discharge all of the nanocrystals, which means a nanocrystal based memory should have a better reliability than conventional nonvolatile memories.[2-3] However, nanocrystal based memories have a rather low charge density which might be a drawback of this approach. In addition, the charge retention time in single-layer nanocrystal based memory device is also limited by the fast direct tunneling process through the ultrathin tunneling layer. To solve these problems, there are have some approaches, suchas the introduction of certain tunneling dielcctric materials and a doubly stacked dot structure. For instance, multilayer nc-Si structure in SiO2 matrix was investigated by some research groups,[6-8] where electrons were injected into the multilayer structure via a FN tunneling process at high programming voltages. An ultrahigh stored charge density is demonstrated in the multilayer nc-Si structure. A self-aligned stacked double-layer nc-Si structure in SiN_x matrix with enhanced retention time has been reported.[9,10]

In this work, we have prepared the stacked nc-Si memory structure where double layers of nc-Si dots embedded within triple SiNx barriers. We investigated the charge storage mechanism in stacked nc-Si memory structure by using capacitance voltage (C-V) measurement and capacitance-time (C-t) measurements.

2. Experimental Details

The stack nc-Si dots based memory structures were fabricated on n-type crystalline Si substrates (6-8 Ω cm) in plasma enhanced chemical vapor deposition system. The doubly stacked layers of nc-Si with the thickness of about 5 nm were fabricated by the layer-by-layer deposition technique[11] with silane and hydrogen mixture gas. SiNx barrier were deposited by a gas mixture of silane and ammonia with the ratio of 1:5. The thickness of both lower and upper tunneling SiN_x barrier was about 4 nm and the thickness of control SiN_x barrier was about 20 nm. For comparison the sample with single nc-Si dots layer was also prepared with the same deposition process. The thickness of nc-Si layer, tunneling layer and the bar-

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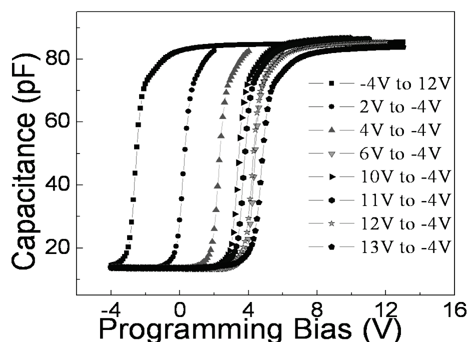

Figure 1. The Capacitance-voltage characteristics of the doubly stacked nc-Si structure.

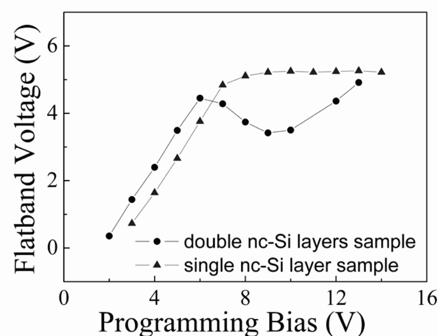

Figure 2. The dependence of the flatband voltage on programming bias.

rier layer was 5nm, 4nm and 20nm, respectively. The samples were annealed in nitrogen ambient at 900 ^{o}C for 30 minute to improve the quality of the nc-Si and to reduce the density of interface states and defects in the structure. The C-V and C-t measurements were performed using Agilent 4284A LCR meter. All measurements were performed at air ambient and at room temperature inside a shield box.

3. Results and discussions

Figure 1 shows the C-V characteristics of the doubly stacked nc-Si memory structure. The bias was sweeping from the accumulation to the inversion region for the MIS device based on the n-type substrates. In order to obtain saturation of charge storage, before each sweep the structure was held at a positive gate bias for 120 s. After each sweep, electrons trapped in the structure were erased by negative bias of -4 V for 120 s to bring the structure to the neutral stage. As can seen in figure 1, at low programming bias, a higher programming bias applied at the gate results in a bigger shift of the flatband voltage, which is caused by more and more electrons trapping in the structure. At moderate programming bias (6 V to 9 V), the flatband voltage decreases with increasing the bias. At high programming bias (10 V to 13 V), the flatband voltage increases with the bias. Under fixed erasing bias and varied programming bias, the relationship between programming bias and flatband voltage is of special interest.

Figure 2 shows the programming bias dependence of the flatband voltage. With increasing the gate voltage, the flatband voltage of the sample with double nc-Si layers is found to first increase, then decrease, and finally increase, exhibiting a clear deep at bias of 9 V. When the programming bias increases from 2 V to 6 V, the flatband voltage is shift from 0.34 V to 4.47 V. With further increasing the programming bias from 6 V to 9 V, the flatband voltage decrease from 4.47 V to 3.44 V. As the bias changes from 9 V to 13 V, the flatband voltage increases to 4.92 V. The flatband voltage of the sample with single nc-Si layer increases from 0.73V to 3.35V when the bias changes from 3V to 5V. Then the flatband voltage keeps invariably with the increasing the bias. we think that the decreasing of flatband voltage at moderate programming bias is attributed to the transfer of electrons from the lower nc-Si layer to the upper nc-Si layer.

Figure 3 shows the relationship of programming bias and the flatband voltage under different hold time. Each sweep measurement was performed after a positive gate bias was held at the gate for different hold time of 120 s, 50 s and 20 s, respectively. From the figure 4, we can see that the flatband voltage strongly depends on the hold time. When the structure was held at a positive gate bias for 120 s, we can see clear at moderate programming bias (9 V). With varying the hold time to 50 s, the flatband-voltage curve also exhibits a deep, but the deep is smaller than that of the hold time of 120 s. It demonstrates that the charge transfer is not sufficient for the hold time of 50 s, resulting that the amount of transfer charges is less than that of the hold time of 120 s. Hence, the decrease of flatband voltage and the deep is smaller than that of the hold time of 120 s. In the case of the hold time of 20 s, we can notice that the flatband voltage keeps unchanged nearly, which demonstrates that few charges exist can transfer from the lower nc-Si layer to the upper nc-Si layer. Based on the above experimental result, we conclude that the charges transfer in the structure strongly depends on the hold time and the flatband voltage decreases markedly with increasing the hold time.

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4. Conclusions

In summary, doubly stacked nc-Si based MIS memory structure was fabricated by plasma enhanced chemical vapor deposition. C-V and C-t measurement was used to investigate electron storage and discharging in the structure. The C-V experiment results show that the flatband voltage first increases, then decreases and finally increases, exhibiting a claer deep at gate voltage of 9 V. The decreasing of flatband voltage at moderate programming bias is attributed to the transfer of electrons from the lower nc-Si layer to the upper nc-Si layer. The C-t measurement results show that the charges transfer in the structure strongly depends on the hold time.

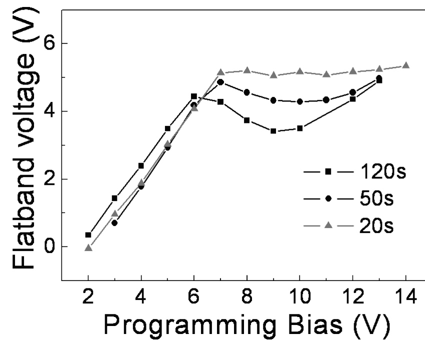

Figure 3. The programming bias dependence of flatband voltage under different hold times.

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