

A Novel Topology of Single-Phase AC-DC Integrated Boost-SEPIC (IBS) Converter Using Common Part Sharing Method (CPSM) for High Step-Up Applications

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Abstract

A novel topology of Integrated Boost-SEPIC (IBS) AC-DC converter using common part sharing method (CPSM) has been proposed in this paper. Conventional boost converters with bridge rectifier configuration are inefficient due to limited voltage step-up ratio which may not be applicable for high step-up applications as in the case of micro generators. The proposed IBS topology is based on the common part sharing method capable of operating both for positive and negative half cycle of the input signal. Result and simulation were conducted using PSIM environment. The proposed AC-DC IBS topology eliminates the requirement of bridge rectifier achieving high efficiency (about 99%), improved power factor (0.75, leading) and lower THD (about 38.8%) which is within IEEE standard.

Keywords

Integrated Boost-SEPIC (IBS), Bridgeless AC-DC Converter, Voltage Gain, THD Minimization, Efficiency Improvement, Power Factor Correction

1. Introduction

Continuous advancement in power electronics has led to the development of self-powered devices requiring low power, mainly analog and digital circuits. Self-powered devices harvest the ambient energies from micro generators and can perform their operation without the requirement of continuous external power supply [1] [2] [3]. The output of micro generators is AC having a low

voltage level in the range of few hundred millivolts but the electronic load requires much higher DC voltage [4] [5]. Hence, power electronic converters govern the output of micro generators to provide the required DC bus to the loads [6] [7].

However, it is very difficult to satisfy the requirement of high voltage conversion ratio and high efficiency at once [3] [4] [5]. This is primarily due to the parasitic resistances, which cause serious degradation in the step-up ratio and efficiency as the duty cycle increases. Moreover, in case of high output voltage applications, severe reverse recovery problem is caused by high voltage rating diode and therefore requires a subber [8] [9] [10] [11] [12]. As a result conventional boost converter would not be acceptable for high step-up applications. To mitigate the problems associated with high voltage output, various types of step-up converters, utilizing the voltage conversion ability have been proposed achieving high performance [12]-[20]. Conventional power converters for energy conversion, mostly consist of two stages: a diode bridge rectifier for AC-DC conversion followed by a standard Buck or Boost DC-DC converter [21] [22] [23] [24]. However, there are major disadvantages in using the two-stage power converters to condition the outputs of the electromagnetic micro generators. Firstly, rectification is not feasible by the use of conventional diodes for very low voltage electromagnetic micro generators. Secondly, even if the diode bridge rectification is feasible, the forward voltage drops in the diodes will cause a large amount of losses and make the power conversion very inefficient. Moreover, bridge rectifier configuration of AC-DC converter suffers from distorted input current at low power factor. Therefore, several techniques have been developed and proposed to solve the harmonic distortions in the input current as well as to improve the power factor [25] [26] [27].

In this paper, a novel topology of Integrated Boost-SEPIC (IBS) converter has been proposed which combines the Boost converter with an isolated SEPIC converter as a series output module in order to obtain high step-up ratio and to overcome the above mentioned drawbacks. A common part sharing method (CPSM) as shown in **Figure 1**, avoiding bridge rectification configuration, has been presented to amplify the output voltage.

The proposed circuit along with principle of operation has been illustrated in Section 2. Section 3 deals with the steady state analysis of the proposed converter. Result and simulation verifying the feasibility of the proposed converter has been discussed in Section 4. The proposed converter is therefore able to achieve high step-up ratio along with improved efficiency, power factor and minimized THD.

2. Proposed Circuit Configuration and Operation

The proposed topology as shown in **Figure 2** comprises of a switched mode Integrated Boost-SEPIC (IBS) AC-DC converter based on the principle of CPSM. The proposed topology consists of four inductors (L_ϕ , L_1 - L_3), five capacitors (C_ϕ ,

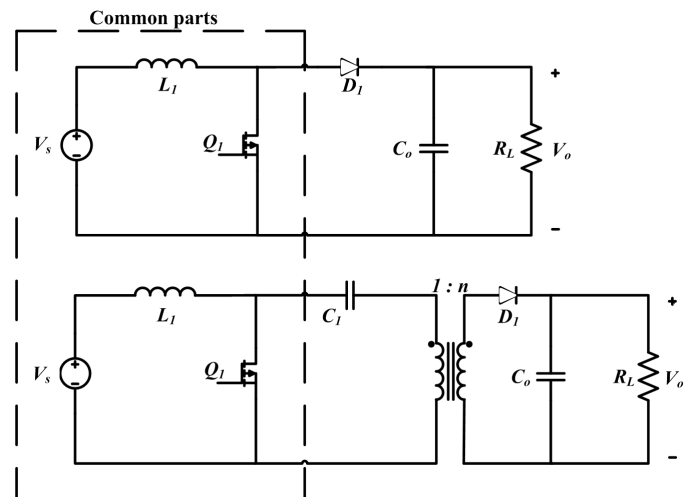


Figure 1. Common part sharing between boost and SEPIC converter.

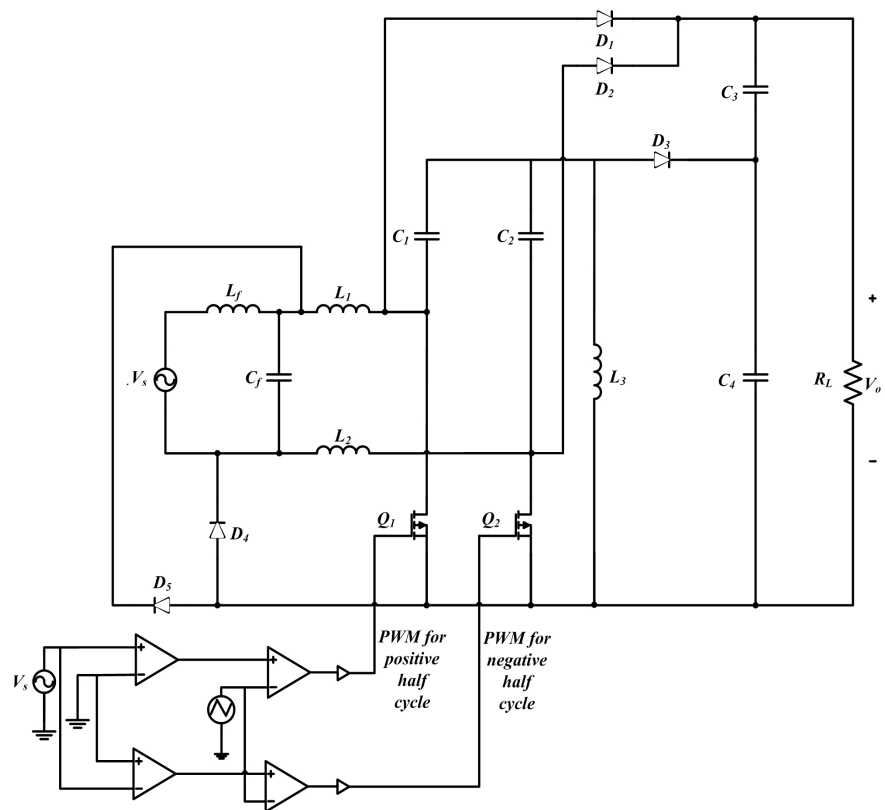


Figure 2. Proposed integrated Boost-SEPIC (IBS) converter.

C_1 - C_4), five diodes (D_1 - D_5) and two switches (Q_1 and Q_2).

Under the proposed converter, a sub-circuit has been proposed, providing the gating signal to the switches (Q_1 and Q_2). The proposed AC-DC converter can operate on both positive and negative half cycle of the input signal. Switch, Q_2 remains off throughout the positive half cycle of the input voltage and the switch Q_1 remains off throughout the negative half cycle of the input signal. In the positive

half cycle, the switch performs continuous on and off operation whereas in the negative half cycle the switch Q_2 performs continuous on and off operation. The inductor L_f and capacitor C_f functions as input electro-magnetic interference (EMI) filters, C_3 and C_4 are the output capacitors and R_L functions as the load respectively. The energy transferred to the load is unidirectional which is achieved through four modes of operation as shown in **Figure 3**.

3. Steady State Analysis of the Proposed Converter

The proposed converter has the output voltage equivalent to the summation of the Boost and SEPIC converter. In steady state operation considering the parameters as in continuous conduction mode, the equations are as follows:

In the boost portion of the circuit,

$$V_s t_{on} + (V_s - V_{o1} t_{off}) = 0$$

where, t_{on} = on time, t_{off} = off time, V_s = supply voltage and V_{o1} = output voltage of Boost converter.

$$V_s t_{on} + V_s t_{off} - V_{o1} t_{off} = 0$$

$$V_s (t_{on} + t_{off}) = V_{o1} t_{off}$$

$$\frac{V_s}{V_{o1}} = \frac{t_{off}}{t_{on} + t_{off}}$$

$$V_{o1} = \frac{1}{1-D} V_s \quad (1)$$

where, D = duty cycle.

In the SEPIC portion of the circuit,

$$V_s = \frac{1}{1-D} V_{o2}$$

where, V_{o2} = output voltage of SEPIC converter.

$$V_{o2} (1-D) = D V_s$$

$$V_{o2} = \frac{D V_s}{(1-D)} \quad (2)$$

The overall output voltage of the integrated Boost-SEPIC converter, combining Equations (1) and (2),

$$V_o = V_{o1} + V_{o2}$$

$$V_o = \frac{1}{1-D} V_s + \frac{D}{1-D} V_s$$

$$V_o = \left(\frac{1}{1-D} + \frac{D}{1-D} \right) V_s$$

$$V_o = \left(\frac{1+D}{1-D} \right) V_s \quad (3)$$

So, the voltage gain, G

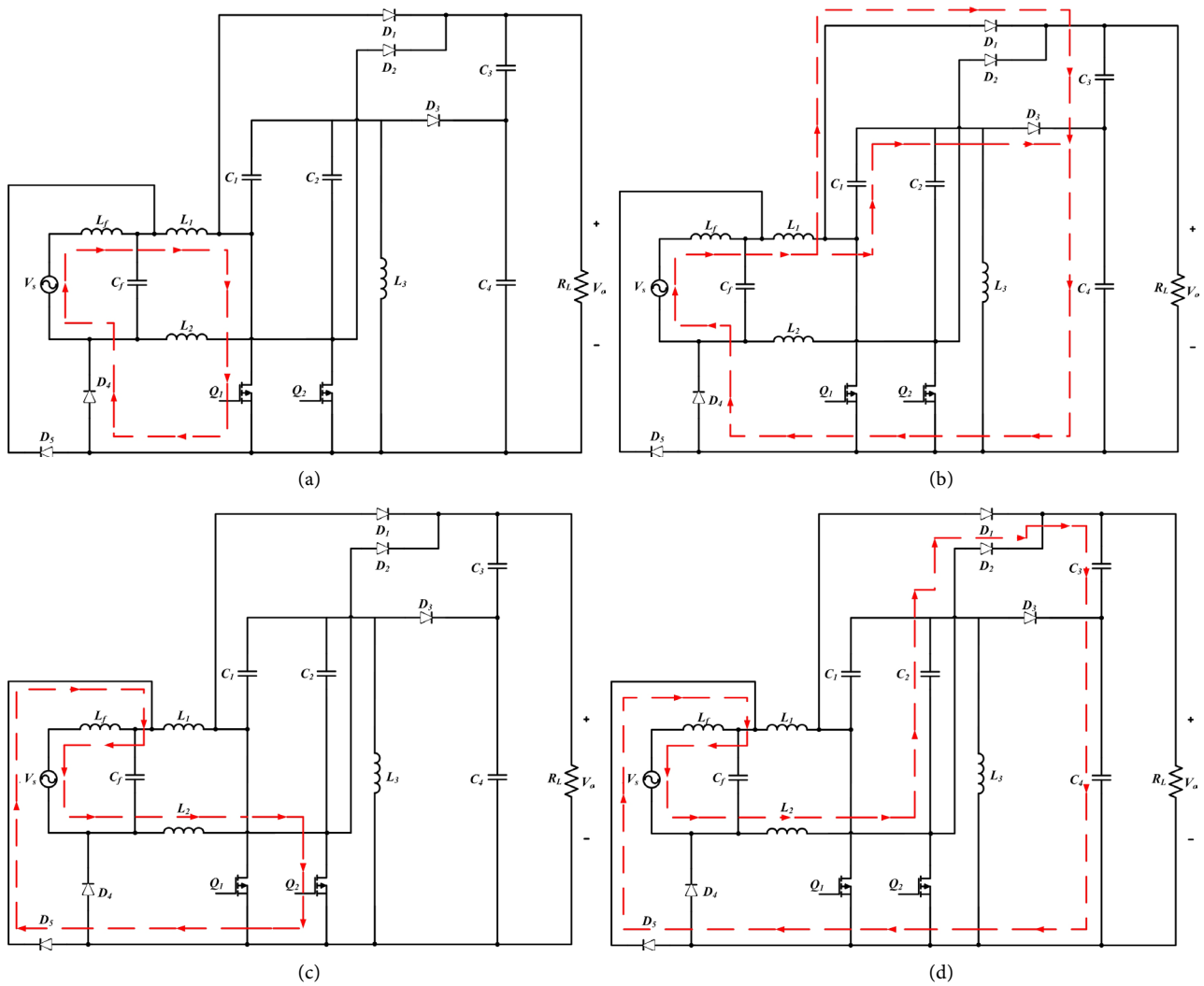


Figure 3. Principle of operation of IBS converter. (a) Mode 1: Positive half cycle when switch Q_1 is on and Q_2 is off, (b) Mode 2: Positive half cycle when switch Q_1 is off and Q_2 is off, (c) Mode 3: Negative half cycle when switch Q_1 is off and Q_2 is on and (d) Mode 4: Negative half cycle when switch Q_1 is off and Q_2 is off.

$$G = \frac{1+D}{1-D}$$

From the above equations it is observed that the output voltage is $\frac{1+D}{1-D}$ times the input voltage, which is significantly high.

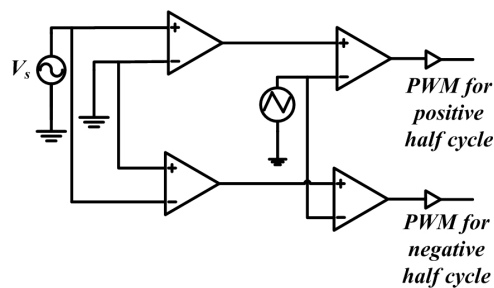
4. Result and Analysis

The proposed circuit has been designed and implemented using PSIM 9.1 environment. The parameters of the proposed circuit used for simulation is given in **Table 1**. The proposed IBS topology has been compared with conventional single-phase AC-DC diode-bridge Boost rectifier conversion circuit.

The gate driving circuit as shown in **Figure 4** generates PWM signal for the switches Q_1 and Q_2 . The gating sequence for activating different switches has

Table 1. Specification of design parameter of IBS converter.

Parameter	Value
Input voltage (V_s)	220 V (AC)
Input frequency (f_{in})	60 Hz
Switching Device	MOSFET
Switching frequency (f_{sw})	50 kHz
Inductor (L_β L_1 - L_3)	10 mH
EMI filter capacitor (C_f)	1 pF
Capacitor (C_1 and C_2)	5 pF
Output Capacitor (C_3 and C_4)	220 uF
Load (R_L)	100 Ω

**Figure 4.** Gate Driving circuit of the proposed IBS converter.

been shown in **Figure 5**.

Typical input voltage and current waveform is shown in **Figure 6(a)** and output voltage, current and power is shown in **Figure 6(b)** and **Figure 6(c)**.

For performance comparison among the proposed and conventional schemes, results are evaluated in terms of THD (%) of input current, input power factor and efficiency (%) of conversion. The outcomes of the discussion are discussed below as shown in **Figure 7**.

In terms of efficiency, the proposed IBS converter as shown in **Figure 7(a)** exhibits high efficiency (about 99%) over the whole range of duty cycle compared to the conventional converter. The proposed IBS converter exhibits lower input current THD and high input power factor throughout all the duty cycles compared to conventional schemes as shown in **Figure 7(b)** and **Figure 7(c)**. In addition, with the increment of duty cycle, the output voltage also increases significantly. The voltage gain, G with respect to duty cycle, D was plotted as shown in **Figure 7(d)** which is coherent with the output voltage Equation (3).

5. Conclusion

A novel topology of integrated Boost-SEPIC (IBS) converter for high step-up and high performance applications has been proposed combining the Boost converter and an isolated SEPIC converter using common part-sharing method (CPSM). The proposed converter achieves high step-up ratio with additional

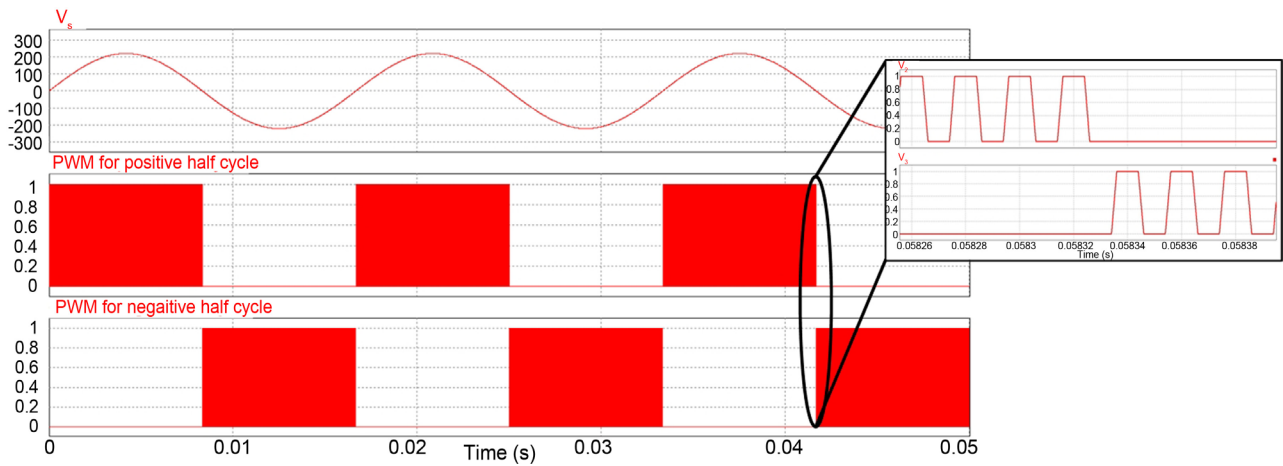
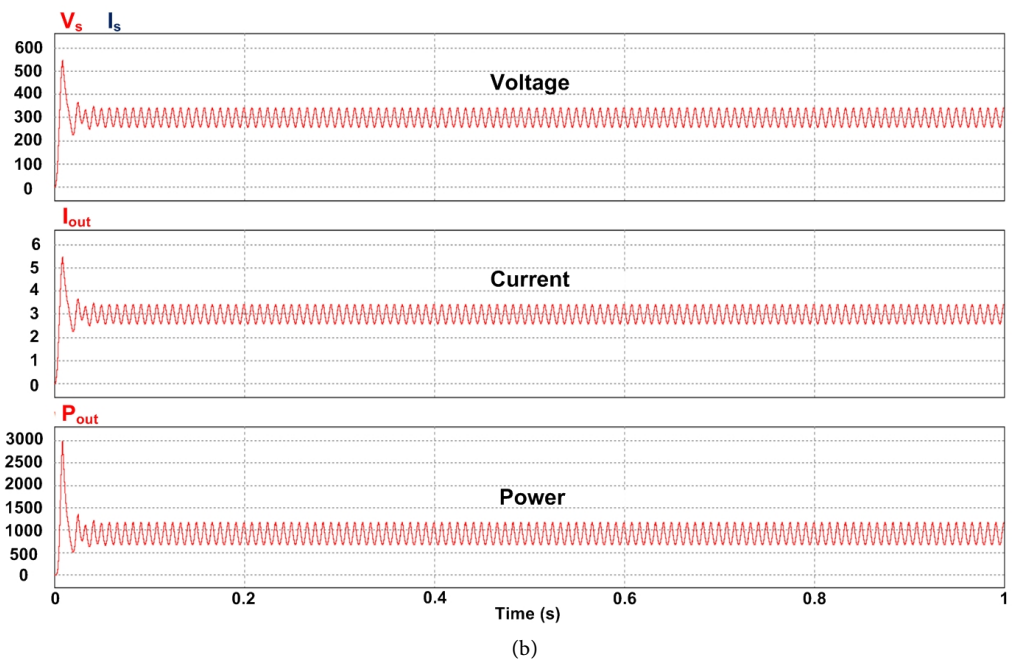
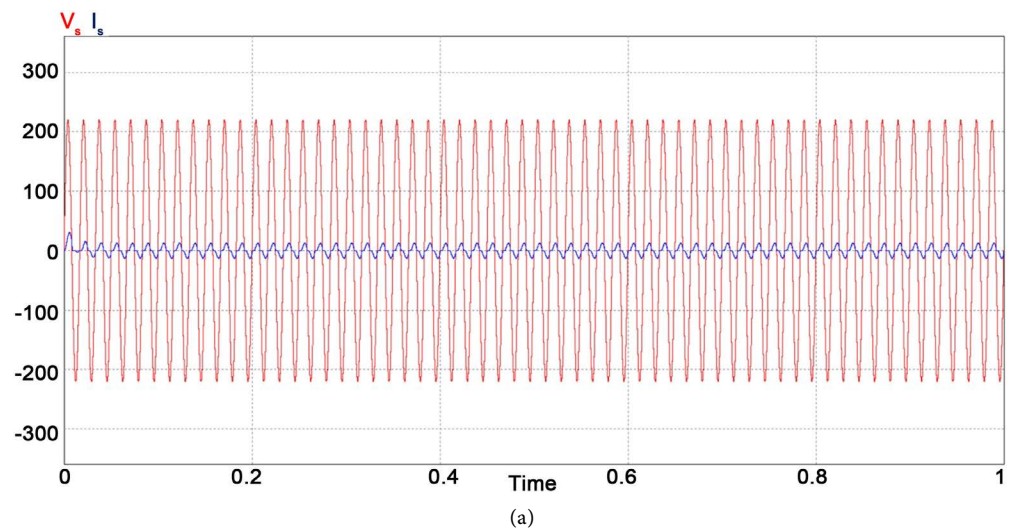


Figure 5. PWM signal generated by the proposed gate driving circuit for the IBS converter.



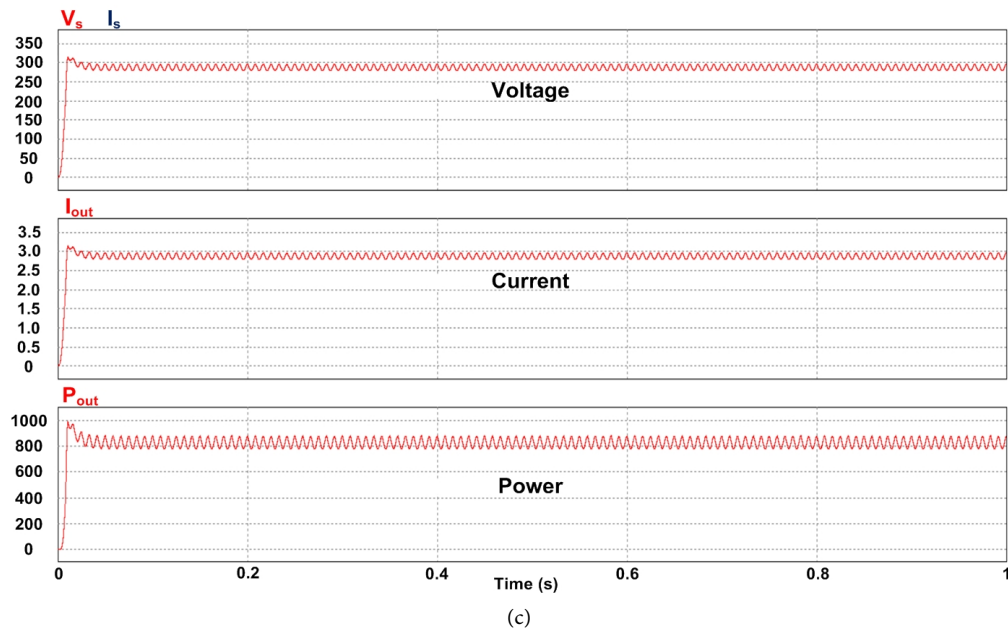


Figure 6. Input voltage and current waveforms for the proposed IBS converter. (b) Output voltage, current and power waveforms of the proposed IBS converter using output capacitor of 220 μF (c) Output voltage, current and power waveforms of the proposed IBS converter using an output bulk capacitor of 1000 μF .

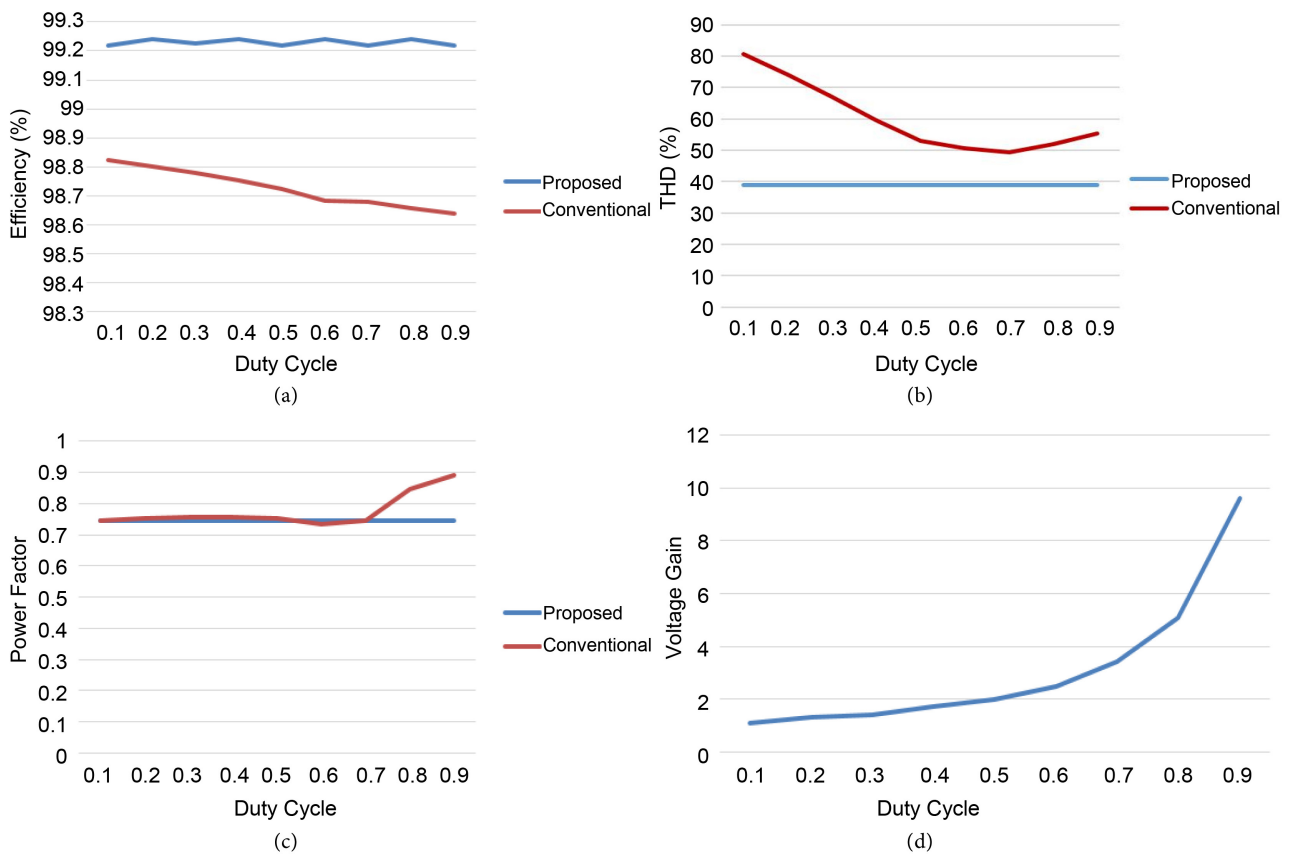


Figure 7. Comparison between proposed IBS converter and conventional AC-DC Boost converter. (a) Percentage efficiency, (b) percentage of Total Harmonic Distortion (THD), (c) Power Factor (PF) and (d) Voltage Gain of the proposed converter.

step-up ability of the isolated SEPIC converter, while at the same time maintaining the continuous input current characteristics of the Boost converter. Moreover, the proposed IBS converter exhibited improved performance in case of efficiency (99%), THD (38.8%) and maintained a leading power factor (0.75). In order to have better performance, close loop implementation of the proposed converter can be conducted to obtain better power factor by employing suitable power factor correction techniques.

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