

Dual Mode-Multiple Output SEPIC Converter Integrated with Passive Ripple Cancelling Circuit for Standalone PV Energy Harvesting System

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Abstract

This document addresses an exhaustive standalone Photovoltaic (PV) energy harvesting system considering two crucial issues: system efficiency and cost effectiveness. It contributes a compact resolution with a combined feature of Dual Mode-Multiple Output (DMMO) associated with input ripple reduction technique. Control strategy incorporates with aspect of Maximum Power Point Tracking (MPPT) and output voltage levels regulation. A theoretical analysis is conducted to evaluate the effect of ripple current on PV power. Proposed dual mode converter achieves efficiency of 98.36% and 97.76% respectively for mode-1 and mode-2 operation. However, simulation is performed applying MATLAB/SIMULINK tools to analyze the feasibility of the recommended system.

Keywords

Photovoltaic Cell, Current Ripple Reduction, Dual Mode Converter, Multiple Outputs, Efficiency

1. Introduction

Along with the decreasing storage of the fossil fuels and rising environmental concerns, the sustainable energy sources, such as the photovoltaic (PV), fuel cells, and wind energy are taken as the promising appellants for future energy supply. Furthermore, back-up storage elements are required to consume the irregular energy fluctuation generated by the sustainable energy sources [1] [2] [3]. Stand-alone systems are independent of utility grids; require storage elements to accommodate the intermittent generation of

solar energy [4] [5] [6] [7]. However, the output voltages of each PV panel and back-up battery cell are quite low; hence arise the need of high step-up and high-efficiency converters to upgrade the low voltage [8] [9] [10].

High frequency applications spontaneously develop current ripples in switching power converters, which may cause momentous impact on the output power [11] [12]. This ripple current influences filtering problems, control issues, output voltage noise, and other hurdles. Ripple reduction techniques contribute an approach for improved power converter performance. A simple and low cost Passive Ripple Cancelling Circuit (PRCC) [13] has been invented. Special features of the proposed PRCC include low cost, simple, modular structure, and independent of the duty ratio control of the main power circuit.

Multilevel converter facilitates the use of renewable energy sources and attains high power ratings, as well as accommodates multiple users. However, multiple-output dc-dc converter is a potential solution for applications requiring multiple supplies where the output voltages and power for each supply are largely different according to user's requirement and distance [14] [15] [16].

High-Voltage DC (HVDC) systems [17] are used exclusively for long distance, which grant higher efficiency and potentially reduce the cost. However, for short distance, Low Voltage Direct Current (LVDC) is a promising solution [18], which facilitates large power shifting capacity with low voltage and improvements to reliability and power quality.

This paper investigates the effect of ripple current on PV output power for single diode model with series and shunt resistance as well as proposes a complete standalone PV energy harvesting system with an effective ripple reduction technique. Comprehensive system is accompanied by Dual Mode-Multiple Output (DMMO) properties and control strategy to realize flexible power flow and high power capability.

2. Proposed System

Figure 1 exhibits the overview of the proposed system.

- A Photovoltaic module with standalone property is connected with a DC-DC converter. Converter is incorporate with the ability to work as dual state SEPIC converter facilitate both high voltage and low voltage system.
- To reduce the input current ripple, ripple reduction technique is integrated into the converter.
- Multiple-output dc-dc converter is a potential solution for applications requiring multiple supplies. The proposed system will be capable of delivering different output voltage levels from single dc-dc converter at the load side.
- At the situation when single voltage level is required among various levels, multiplexing scheme can be embedded into load side to fulfill user's requirements (**Figure 1**).

2.1. Impact of Current Ripple on Generated Power of Single Diode PV Module with Series and Shunt Resistances

Single diode model is the simplest as it has a current source in parallel to a diode. This

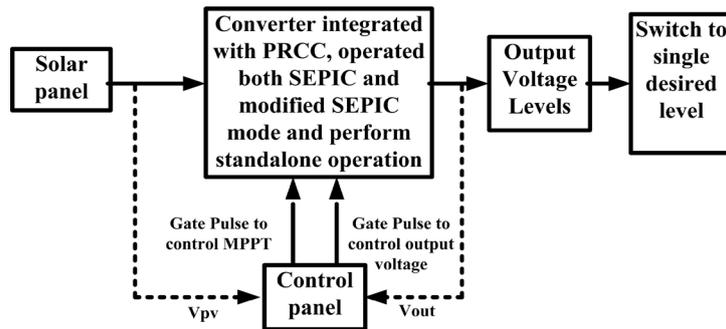


Figure 1. Block diagram of the proposed system.

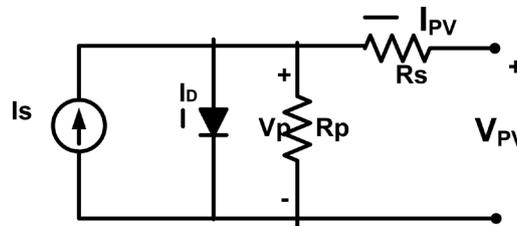


Figure 2. Mathematical model of PV module with series and shunt resistance [19] [20].

model is upgraded by the inclusion of one series resistance, R_s [21] [22]. In spite of its simplicity; it exhibits acute deficiencies when suffered from temperature deviations. An accretion of the model which introduces a supplementary shunt resistance R_p [23] [24] is shown in Figure 2.

I-V characteristics of PV module [25] [26] can be represented as:

$$I_{PV} = I_s - I_o \left[e^{\frac{V_{PV} + I_{PV} \cdot R_s}{\alpha}} - 1 \right] - \frac{V_P}{R_p} \tag{1}$$

where, $\alpha = A \cdot V_T$

$$V_T = \frac{KT}{q}$$

Different Parameters:

- I_s is the current generated by the incident light.
- I_o is the reverse saturation current.
- q is the electron charge [$1.60217646 \times 10^{-19}$ C].
- k is the Boltzmann constant [$1.3806503 \times 10^{-23}$ J/K].
- T [K] is the temperature of the p-n junction.
- A is ideality factor of diode.
- V_T is the thermal voltage of the module.
- R_s is the series resistance of the module.
- R_p is the parallel resistance of the module.

From Equation (1), the output voltage of PV module can be derived as follows:

$$V_{PV} = \alpha \cdot \ln \left[\frac{I_s + I_o - I_{PV}}{I_o} - \left(\frac{V_P}{I_o \cdot R_p} \right) \right] - I_{PV} \cdot R_s \tag{2}$$

Multiplying Equation (2) by I_{pv} , the output power of PV module can be obtained,

$$P_{pv} = I_{pv} \cdot \alpha \cdot \ln \left[\frac{I_s + I_o - I_{pv}}{I_o} - \left(\frac{V_p}{I_o \cdot R_p} \right) \right] - I_{pv}^2 \cdot R_s \quad (3)$$

From Equation (1) to Equation (3), it is observe that the I_{pv} , V_{pv} and P_{pv} are usually considered as pure DC values. However, in practical applications, the output voltage and current of PV module contain ripple components caused by the front-end converter of the system and this may cause significant impact on the output power. Hence appear the urgency to use a ripple reduction technique with the PV module.

Figure 3 shows PV output power perturbation caused by periodical ripple current. From **Figure 3**, periodically variation of p_{pv} due to periodical variation of i_{pv} , can easily be observed. As an illustration, consider a switching period from $t = 0$ to $t = T_s$ for the case when PV module is operated near MPP assuming the irradiance is fixed as shown in **Figure 3(b)**. When the active switch is turned on, i_{pv} will increase from I_a to I_b for $t \in [0, DT_s]$. At the same time, the corresponding p_{pv} trajectory is varied from P_a to P_b . It is seen that during this interval, the MPP is achieved only at one point [13].

Similarly, when the switch is turned off, i_{pv} will decrease from I_b to I_a for $t \in [DT_s, T_s]$. The corresponding p_{pv} is varied from P_b to P_a . Again, the MPP is achieved only at one point. Obviously, from **Figure 3(b)** it is clearly seen that the average power $P_{pv,avrg}$ is less than the available maximum PV output power P_M .

To analyze the ripple-affected power loss of PV module, at first, the i_{pv} can be defined as a periodically time-variant function as $i_{pv}(t)$.

- $I_{pv,r}(t)$ represents the current in the rising period.
- $I_{pv,f}(t)$ represents the current in the falling period.

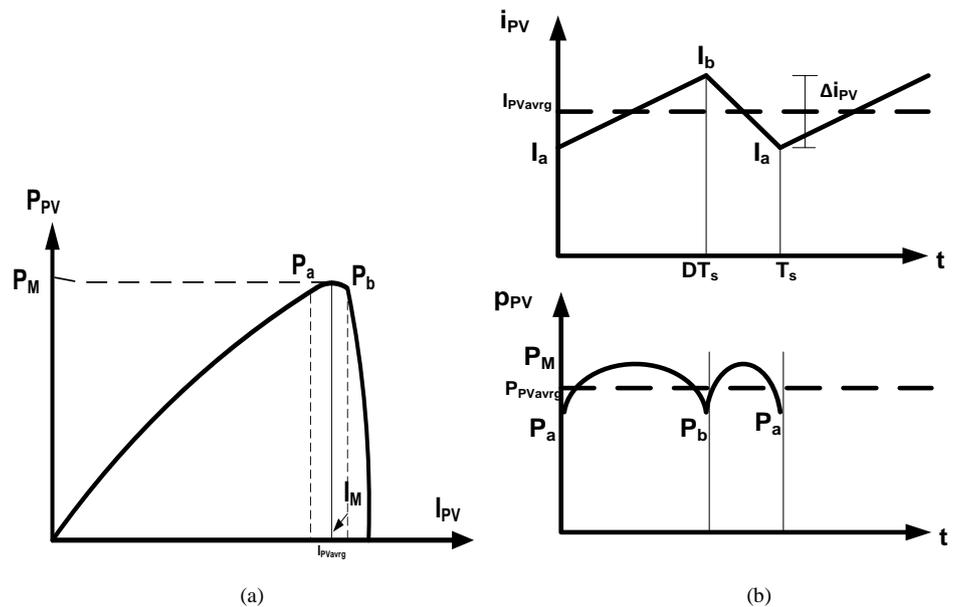


Figure 3. Illustrations of PV output power perturbation caused by ripple current. (a) P-I curve, (b) time-variant waveforms of i_{pv} and P_{pv} [13].

- $I_{PV,avg}$ represents the average value of PV current.
- Δi_{PV} is the ripple current.
- D is the duty ratio.
- T_s is the switching period.

For rise time,

$$i_{PV,r}(t) = \begin{cases} \frac{t-nT_s}{DT_s} \cdot \Delta i_{PV} + I_{PV,avg} - \frac{\Delta i_{PV}}{2}, & t \in [nT_s, (n+D)T_s] \\ 0, & t \notin [nT_s, (n+D)T_s] \end{cases} \quad (4)$$

For fall time,

$$i_{PV,r}(t) = \begin{cases} \frac{-\Delta i_{PV}}{(1-D)T_s} \cdot t + I_{PV,avg} + \Delta i_{PV} \frac{(1+D)}{2(1-D)}, & t \in [(n+D)T_s, (n+1)T_s] \\ 0, & t \notin [(n+D)T_s, (n+1)T_s] \end{cases} \quad (5)$$

Periodically time-variant function of the PV output power can be described as:

$$p_{PV} = p_{PV,r}(t) \cdot [u(t-nT_s) - u(t-(n+D)T_s)] \\ + p_{PV,f}(t) \cdot [u(t-(n+D)T_s) - u(t-(n+1)T_s)]$$

Then, substituting Equation (4) and Equation (5) into Equation (3), $P_{PV,r}(t)$ and $P_{PV,f}(t)$ can be derived as follows:

$$p_{PV,r}(t) = - \left(\frac{t-nT_s}{DT_s} \cdot \Delta i_{PV} + I_{PV,avg} - \frac{\Delta i_{PV}}{2} \right)^2 R_s \\ + \left(\frac{t-nT_s}{DT_s} \cdot \Delta i_{PV} + I_{PV,avg} - \frac{\Delta i_{PV}}{2} \right) \cdot \alpha \cdot \ln \beta \quad (6)$$

$$\text{where, } \beta = \left[\frac{I_s + I_o - \left(\frac{t-nT_s}{DT_s} \cdot \Delta i_{PV} + I_{PV,avg} - \frac{\Delta i_{PV}}{2} \right)}{I_o} - \left(\frac{V_p}{I_o \cdot R_p} \right) \right] \quad \& \quad n = 0, 1, 2, \dots, n$$

$$p_{PV,f}(t) = - \left(\frac{-\Delta i_{PV}}{(1-D)T_s} \cdot t + I_{PV,avg} + \Delta i_{PV} \frac{(1+D)}{2(1-D)} \right)^2 R_s \\ + \left(\frac{-\Delta i_{PV}}{(1-D)T_s} \cdot t + \Delta i_{PV} \frac{(1+D)}{2(1-D)} \right) \cdot \alpha \cdot \ln \gamma \quad (7)$$

$$\text{where, } \gamma = \left[\frac{I_s + I_o - \left(\frac{-\Delta i_{PV}}{(1-D)T_s} \cdot t + I_{PV,avg} + \Delta i_{PV} \frac{(1+D)}{2(1-D)} \right)}{I_o} - \left(\frac{V_p}{I_o \cdot R_p} \right) \right]$$

& $n = 0, 1, 2, \dots, n$.

Equation (6) and Equation (7) exhibits the presence of current ripple (Δi_{PV}) in the output power of PV module for both rise time and fall time. Thus the need for ripple

cancelling technique is arrived to solve this dilemma of PV module.

3. Proposed DMMO SEPIC Converter

Schematic of the proposed DMMO (dual mode-multiple output) SEPIC converter is shown in **Figure 4** and each part of the system is discussed in next subsections.

3.1. Passive Ripple Cancelling Circuit (PRCC)

PRCC are integrated into the input side of a conventional converter to eliminate the input current ripple. PRCC consists of a high frequency transformer modelling as an ideal transformer with turns ratio N and a magnetizing inductor Lm , a ripple mirror inductor $Lr1$ as well as two blocking capacitors $Cr1$, $Cr2$ that are connected to the primary and the secondary winding of the transformer respectively.

In addition, each terminal of the proposed PRCC is connected to one of the main inductor $L1$ terminals of the converter where the current ripple is generated. Due to the blocking capacitors of $Cr1$ and $Cr2$ as well as the reversal polarity of the transformer, only the high frequency ac voltage/current of inductor $L1$ are reflected to $Lr1$ automatically.

Wave shapes of **Figure 5** demonstrate the working fundamental of PRCC. It can be observed that when the switch S is turned on, i_{L1} exhibits a positive slope while i_{Lr1} exhibits a negative slope. When the switch S is turned off, i_{L1} exhibits a negative slope while i_{Lr1} exhibits a positive slope. Thus mirror inductor attenuates input current ripple [13].

$$\text{Equation of Input current ripple cancelling ratio is: } \delta = 1 - (\Delta i_s / \Delta i_{L1}).$$

3.2. Operating Principle of Proposed System

Figure 6 illustrates three operating states of the proposed system.

- In state 1, the PV array supplies power to load and possibly also to the battery, corresponding to the daytime operation of the PV system.
- In state 2, converter and loads are disconnected and the system enters into the stand-alone approach. The PV array charges battery without energy transferred to the load.
- In state 3, the battery supplies power to the load through the converter, indicating the nighttime operation of the stand-alone system.

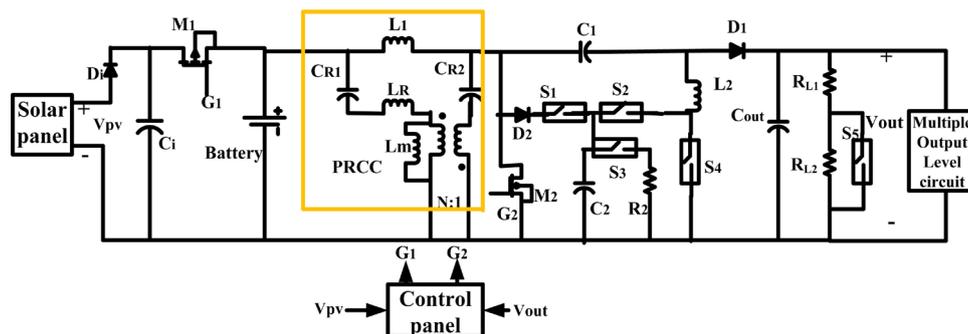


Figure 4. Circuit configuration of DMMO SEPIC converter integrated with passive ripple cancelling circuit (PRCC).

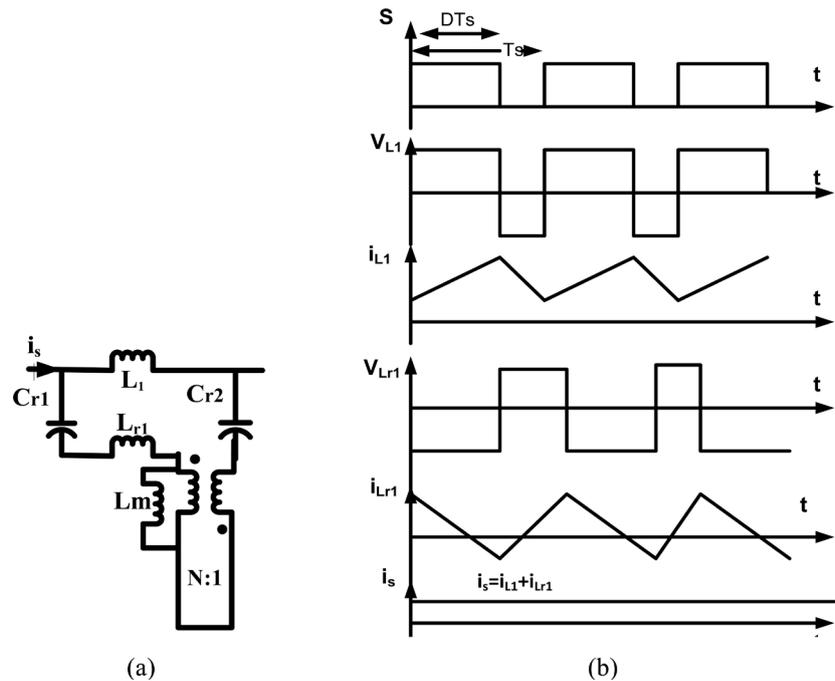


Figure 5. (a) Schematic diagram of PRCC, (b) Inductor voltage and current wave shapes for PRCC integrated converter.

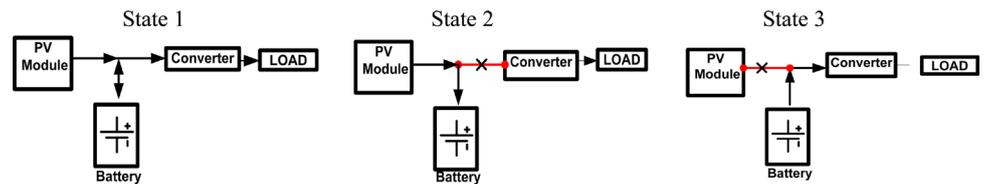


Figure 6. Three operation states of proposed converter.

3.3. Operating Modes of the Converter

Mode I (Figure 7):

Switch S_1 , S_2 are turned on and S_3 , S_4 and S_5 are turned off. Converter acts as the modified version of SEPIC [27] [28] providing high output voltage.

In this state, capacitor is being involved in the operation of the converter through S_1 and S_2 switches. Effect of resistance R_2 is isolated from the circuit by turning off switch S_3 .

- **State I:** Switch M_2 is turned-on and the diode D_1 is blocked and the inductors L_1 and L_2 store energy. The input voltage is applied to the input inductor L_1 through switch M_2 . C_2 , L_2 and C_1 complete a circuit without changing the direction of inductor current. Load is connected directly with output capacitor C_o .
- **State II:** Switch M_2 is turned-off and the energy stored in the input inductor L_1 is transferred to the output through the capacitor C_1 and output diode D_1 , and also to the capacitor C_2 through the diode D_2 . Therefore, the switch voltage is equal to the capacitor C_2 voltage. The energy stored in the inductor L_2 is transferred to the output through the diode D_1 .

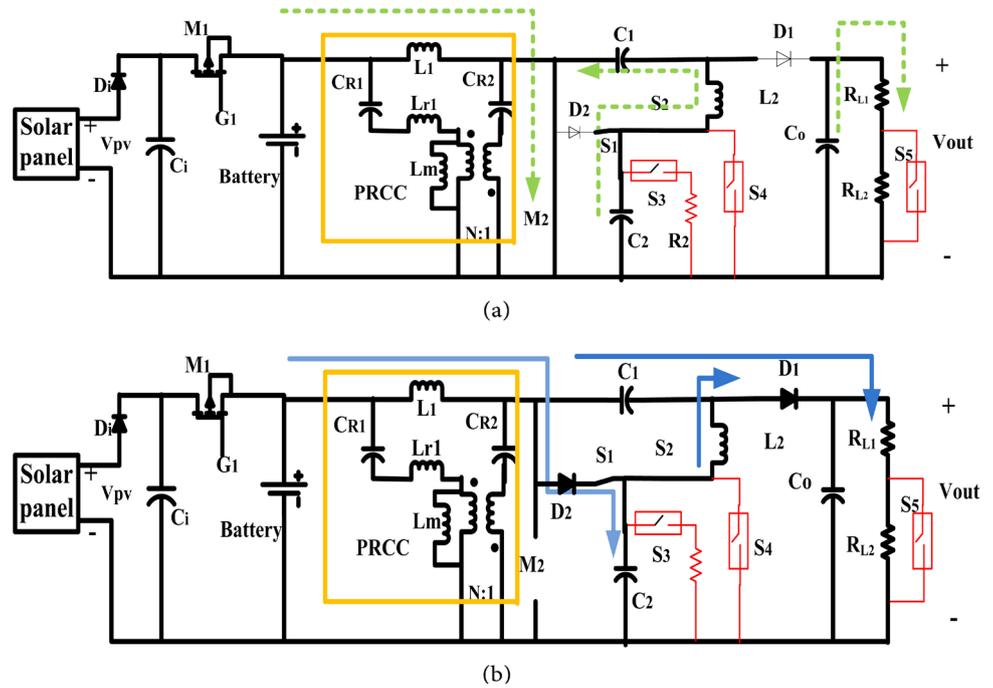


Figure 7. Operating states of the proposed converter in “Mode I” (a) state I (b) state II.

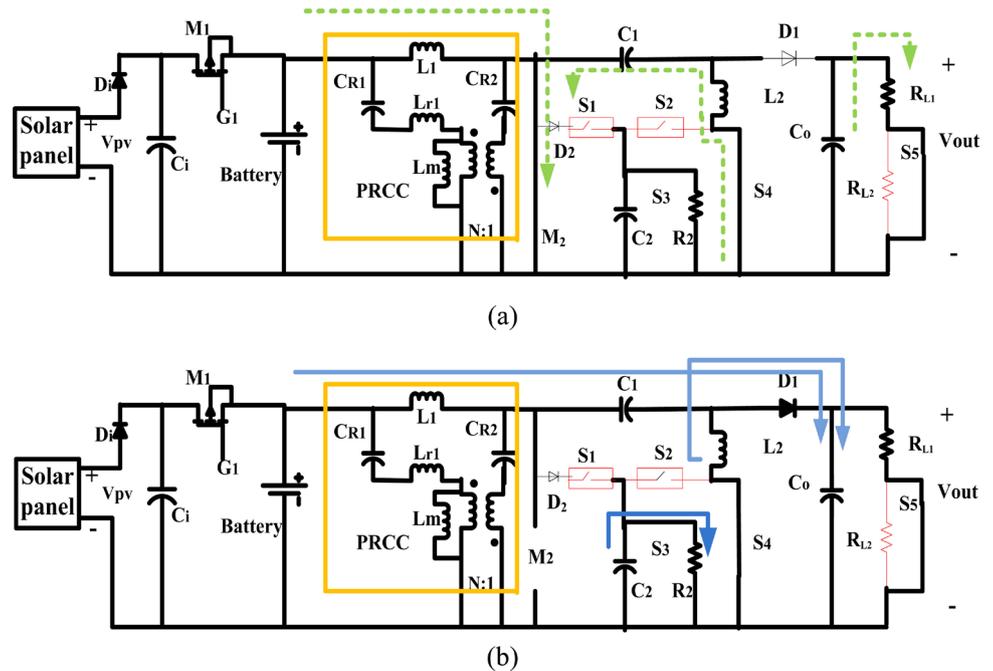


Figure 8. Operating states of the proposed converter in “Mode II” (a) state I (b) state II.

Mode II (Figure 8):

Switch S_1 , S_2 are turned off and S_3 , S_4 and S_5 are turned on. Converter acts as the conventional SEPIC [29] [30] converter. This state provides comparatively less step up ratio than mode I.

In this state of operation, diode D_2 is always reverse-biased and capacitor C_2 is being

isolated by switch S_1 and S_2 , as well as it will complete a circuit with R_2 through switch S_3 . Load resistance will be reduced by removing R_{L2} with the help of switch S_5 .

- **State I:** Switch M_2 is turned on, current i_{L1} increases and the current i_{L2} goes more negative. The capacitor C_1 supplies the energy to increase the magnitude of the current in i_{L2} , diode D_1 and D_2 are reverse-biased. C_o supplies energy to the load R_{L1} .
- **State II:** Switch M_2 is turned off. Current i_{Ct} becomes the same as the current i_{L1} . Inductors do not allow instantaneous changes in current. Power is delivered to the load from both L_2 and L_1 . However C_1 is being charged by L_1 during this off cycle, and will in turn recharge L_2 during the on cycle.

3.4. Multiple Outputs

Proposed topology of multiple output levels are being described in next sub section. The motivation of this study is to design a dual mode- multiple output (DMMO) converter for increasing the conversion efficiency and voltage gain, reducing the control complexity, and saving the manufacturing cost.

3.5. Operation of Multiple Output Circuit

Gate pulses Go_2 , Go_3 and Go_4 are the respective switching pulses for switches Mo_2 , Mo_3 and Mo_4 , shown in **Figure 9**, as well as they are provided fixed duty cycle of 80%, 50% and 30% subsequently. In **Figure 10**, four operating states are illustrated.

State I ($T_0 - T_1$): In this state, switches Mo_2 , Mo_3 and Mo_4 are turned ON for a span. Along with these diodes Do_2 , Do_3 and Do_4 are being turned OFF. Three levels are directly connected to the converter.

State II ($T_1 - T_2$): In this state, switches Mo_2 , Mo_3 are turned ON and diodes Do_2 , Do_3 are turned OFF. For this span, switch Mo_4 is turned OFF. Because of the polarity of inductor Lo_4 , diode Do_4 turns ON and the output loop is connected to the inductor Lo_4 through the diode Do_4 .

State III ($T_2 - T_3$): Only switch Mo_2 is turned ON and the corresponding diode Do_2 is turned OFF. From multiple levels only the first level is directly connected with the

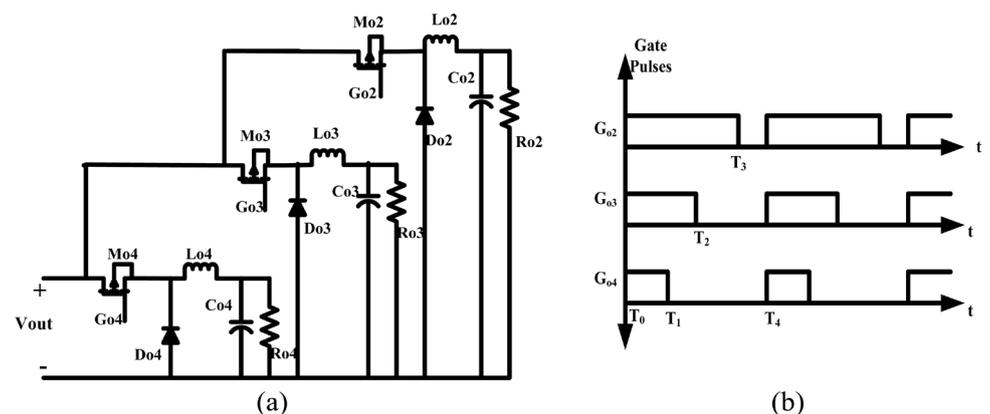


Figure 9. (a) Schematic of “Multiple Output Circuit” (b) Switching gate pulses of output level switches.

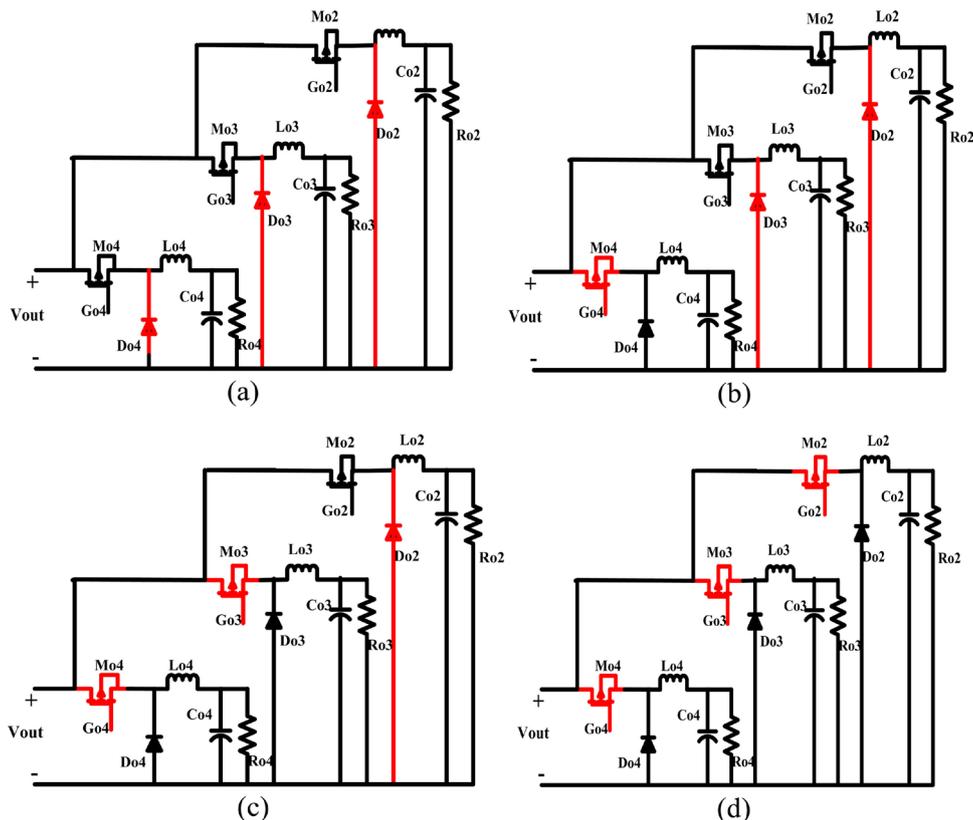


Figure 10. Operating states of the “Multiple Output Circuit” (a) state I (b) state II (c) state III (d) state IV.

converter circuit. Other two levels are connected to inductors L_{o3} and L_{o4} respectively, through corresponding diodes.

State IV ($T_3 - T_4$): Output loops are completed individually through respective inductors and diodes as all the three switches are being turned OFF.

3.6. Control Scheme

The maximum power point tracking (MPPT) can be implemented by adjusting the duty cycle of switching device M_1 shown in **Figure 4**. In the MPPT loop, the PV voltage is regulated to follow an optimal operating point, which is initially assigned to 80% of the open-circuit voltage of the PV array. This point can be determined by the “constant voltage method”. Moreover, the PV voltage regulation loop is used to improve the MPPT performance.

In Mode I, switch S_1 , S_2 are turned on and S_3 , S_4 and S_5 are turned off, when the converter act as modified SEPIC. On/off operation of these switches are complementary for mode II, when it acts as conventional SEPIC.

In the output voltage control loop shown, the duty cycle of switching device M_2 shown in **Figure 4** is the control variable, which regulates the output voltage to follow the expected voltage. To serve this purpose PI controller is used. When the output power of the PV array is lower than the load power, the battery should supply the dif-

ference. Here a single control scheme can regulate multiple output levels. The control block diagram of the proposed control scheme is illustrated in **Figure 11**.

➤ **Constant Voltage Method:**

The solar array is temporarily isolated from the MPPT, and a V_{OC} measurement is taken [31]. Next, the MPPT calculates the correct operating point using the equation mention below:

$$\frac{V_{MPP}}{V_{oc}} \cong K < 1$$

And the pre-set value of K , and adjusts the array's voltage until the calculated V_{MPP} is reached. This operation is repeated periodically to track the position of the MPP. Although this method is extremely simple, it is difficult to choose the optimal value of the constant K . Value of ranging from 73% to 80% [32] [33]. **Figure 12** shows the actual K values required for a given PV array over a temperature range of $0^{\circ}\text{C} - 60^{\circ}\text{C}$ and irradiance levels from 200 to 1000 W/m^2 . These curves were calculated using the I-V relationship for a PV cell.

➤ **Proportional Integral Controller:**

The PI-Controller is a combination of a proportional and integral controller, which has two tuning parameters to adjust: proportional (k_p) and integral (k_i). PI controller is mainly used to eliminate the steady state error resulting from P controller [35] **Figure 13** demonstrates the operating fundamentals of PI controller through block diagram.

$$CO = k_p \Delta + k_i \int \Delta dt$$

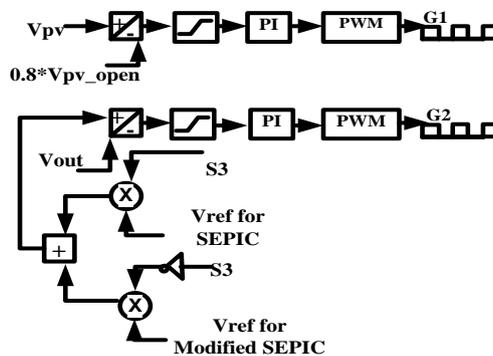


Figure 11. Schematic of control circuit.

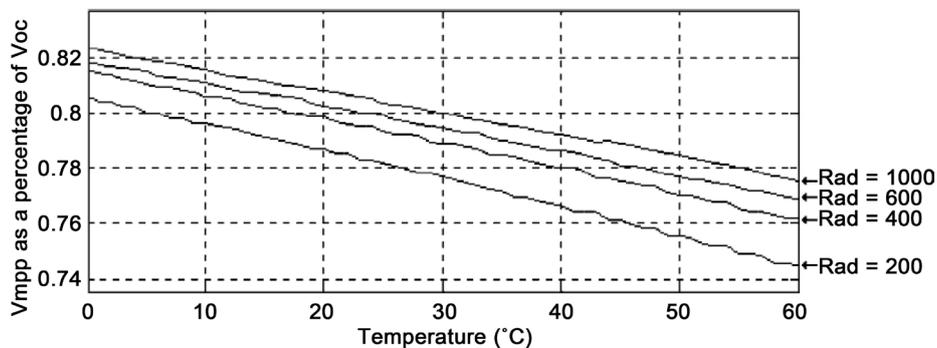


Figure 12. V_{MPP} as a percentage of V_{OC} as functions of temperature and irradiance [34].

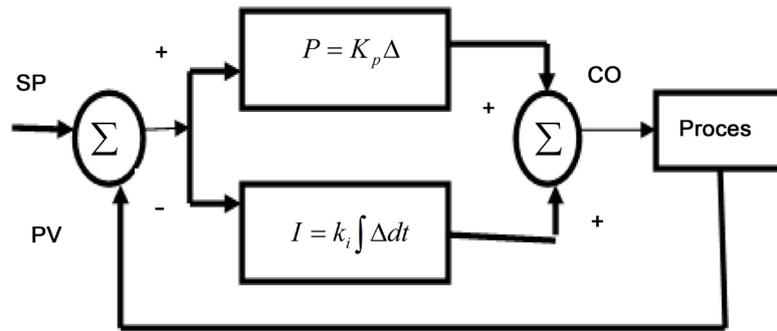


Figure 13. Block diagram of PI controller.

where, Δ = set point(SP) - process variable(PV)

CO = controller output signal

The integral term continually sums up error. Through constant summing, integral action accumulates influence based on how long and how far the measured PV has been from SP over time.

❖ Effect of (k_p):

- Increasing k_p will reduce the steady state error.
- After certain limit increasing k_p only causes overshoot.
- Increasing k_p reduces the rise time [36].

❖ Effect of (k_i):

- Integral control eliminates the steady state error.
- After certain limit, increasing k_i will only increase overshoot.
- Increasing k_i reduces the rise time a little.

4. Simulation and Observation

In order to verify the performance of the proposed system, simulation work is carried out in the MATLAB/SIMULINK environment. For simulating the system, PV panel specifications are set under 1000 W/m² irradiance and 30°C temperature condition.

Figure 14(a) shows voltage and current waveforms of the input side. As shown in **Figure 14(a)**, the PV voltage is regulated to 12.8 V, which represents the MPP (maximum power point) and PV current more closely approximates DC, with an average value of about 3.859 A. Consequently, output voltage is desired to be regulated on 100 V for mode-1. As seen from **Figure 14(b)**, output voltage is 99.14 V and output current is 0.49 A, as a result converter provides output power of 49.57 watt with 7.75 voltage step up ratio.

Figure 15(a) illustrates multiple output voltage levels for mode I at 80 V, 50 V and 30 V. Along with these, **Figure 15(b)** presents corresponding currents waveforms. This mode provides high voltage step up ratio which is applicable for long distance high voltage systems. **Figure 16(a)** presents PV voltage and current waveforms indicating maximum power point achieved at 12.8 V providing 49.39 watt input power. As seen in **Figure 16(b)**, output voltage is regulated at desired point of 50 V for mode II. Moreover this mode provides voltage step up ratio of 3.9. Converter output voltage and cur-

rent wave shapes expose that, steady state arrive earlier in mode II than mode I. As well as **Figure 17(a)** displays 3 voltage levels of 40 V, 20 V and 15 V of mode II. **Figure 17(b)** shows multi level output current wave shapes subsequently.

Table 1 exhibits high efficient feature of the proposed converter as it provides 98.35% and 97.76% efficiency subsequently for mode I and mode II. Therefore, **Table 2** presents different electrical properties of multiple output levels.

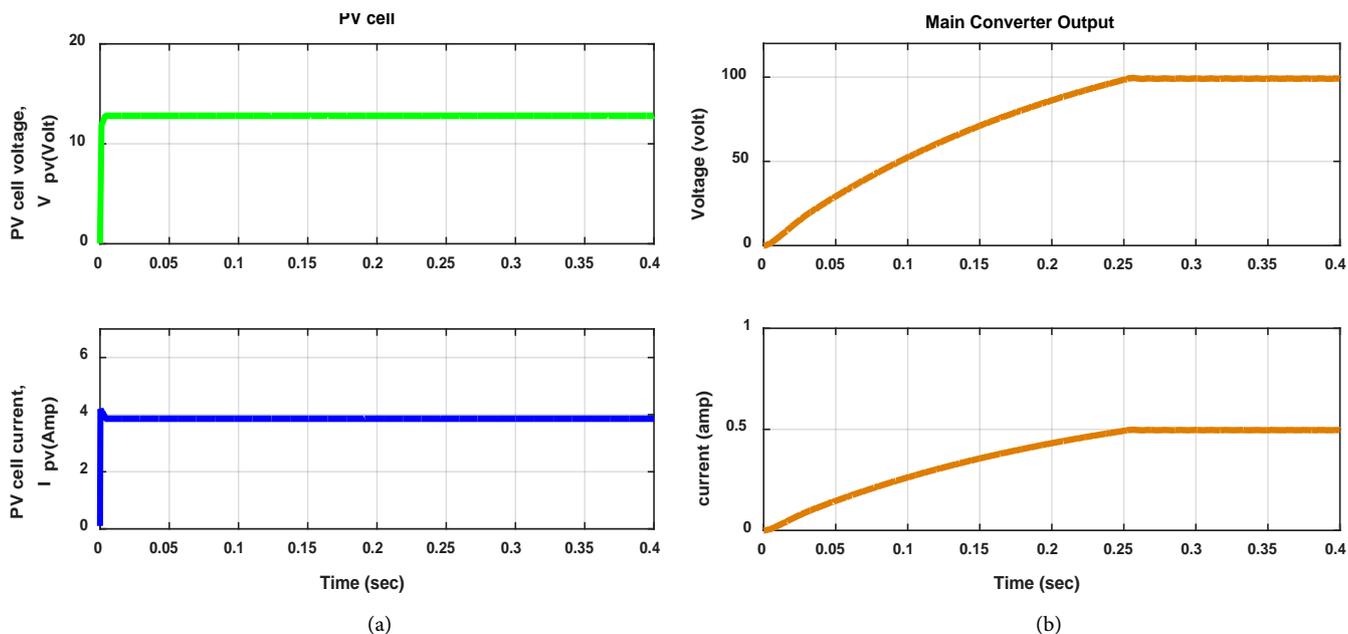


Figure 14. (a) Input voltage and current waveshapes of PV module (Mode I); (b) Waveshapes of multilevel current outputs (Mode I).

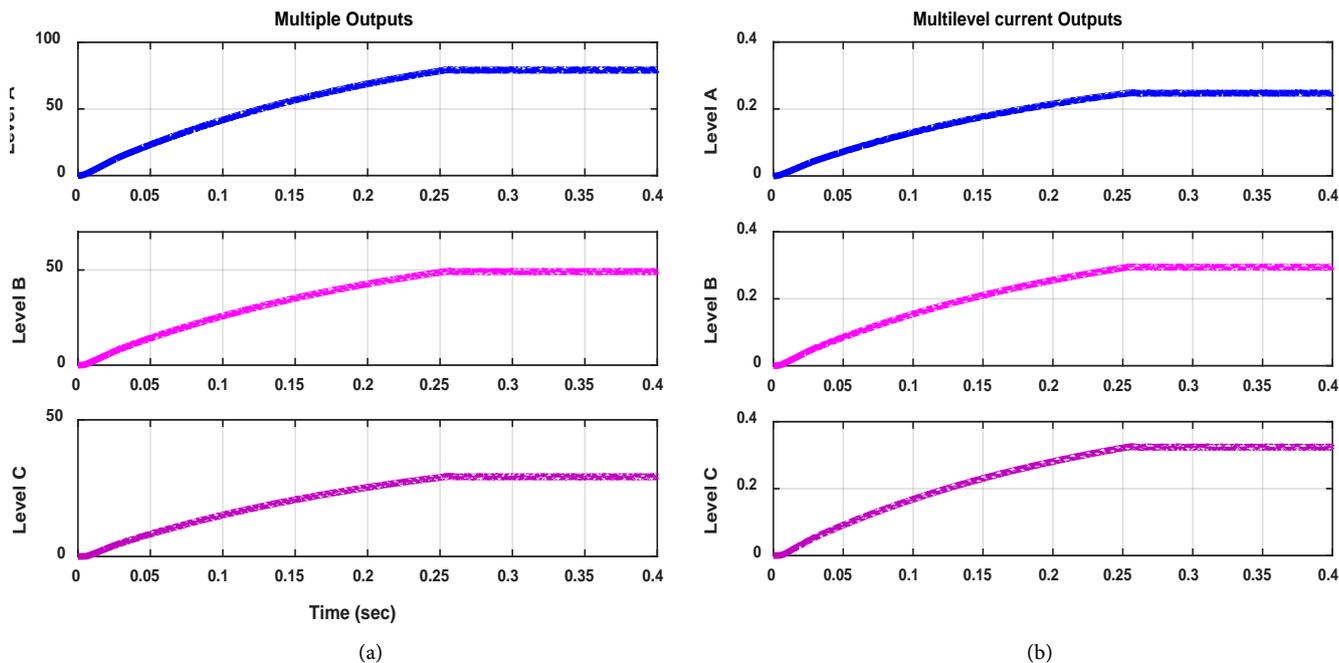


Figure 15. (a) Voltage waveshapes of multiple output levels (Mode I); (b) Current waveshapes of multiple output levels (Mode I).

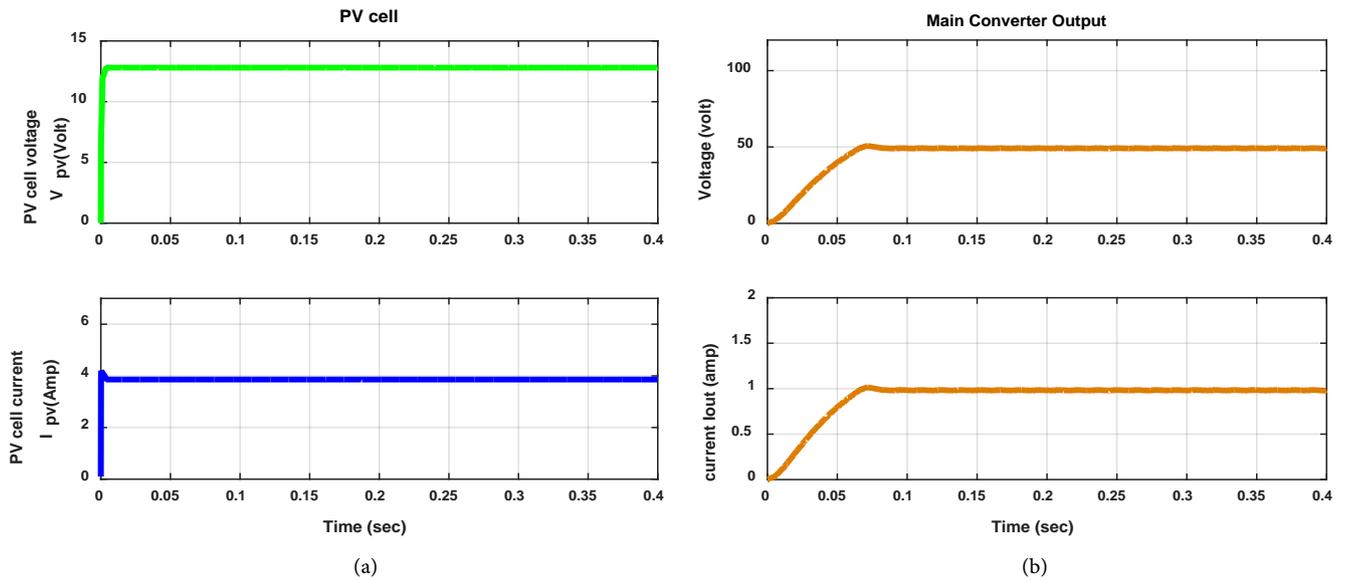


Figure 16. (a) Input voltage and current waveshapes of PV module (ModeII); (b) Output voltage and current waveshapes of the main converter (Mode II).

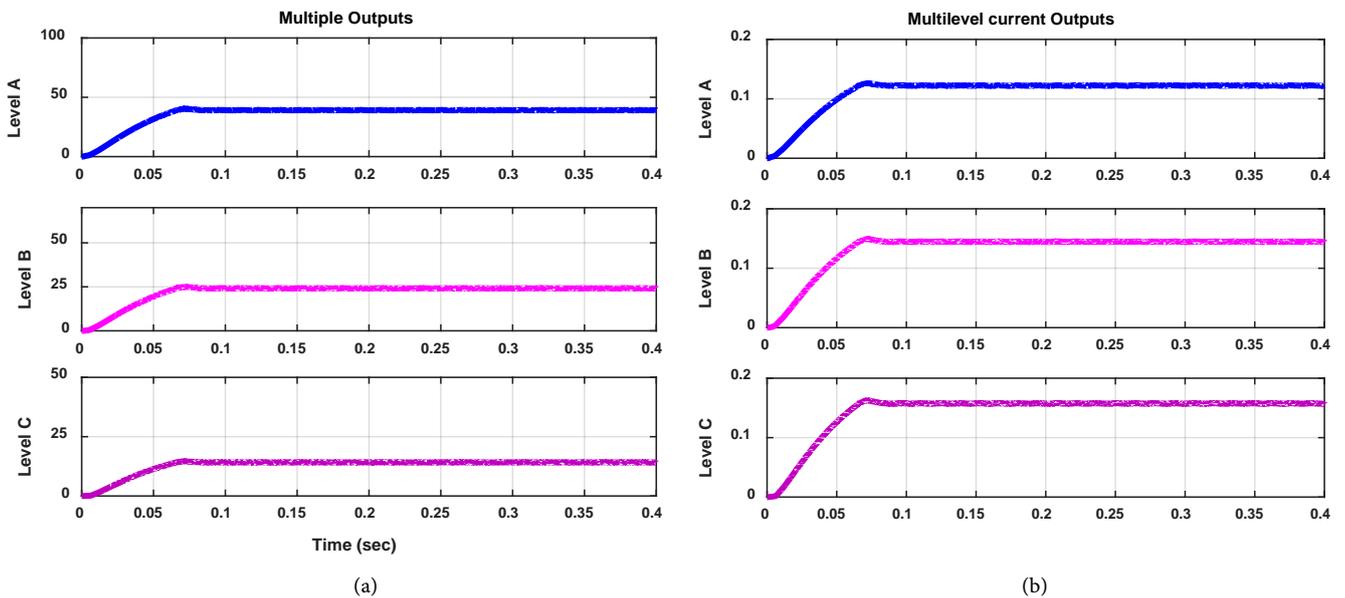


Figure 17. (a) Voltage waveshapes of multiple output levels (Mode II); (b) Waveshapes of multilevel current outputs (Mode II).

Table 1. Electrical parameters of input and output of proposed dual mode converter.

Converter	Input			Converter Output		
	Voltage (V)[Volt]	Current (I)[Amp]	Power (P)[Watt]	Voltage (V)[Volt]	Current (I) [Amp]	Power (P) [Watt]
Mode I [Modified SEPIC]	12.8	3.859	49.39	99.14	0.49	49.57
					Efficiency: 98.35%	
Mode II [SEPIC]	12.8	3.859	49.39	49.16	0.9823	48.29
					Efficiency: 97.76%	

Table 2. Electrical properties of output levels.

Converter	Output Levels								
	Level A			Level B			Level C		
	Vo2 (Volt)	Io2 (Amp)	Po2 (watt)	Vo3 (Volt)	Io3 (Amp)	Po3 (watt)	Vo4 (Volt)	Io4 (Amp)	Po4 (watt)
Mode I [Modified SEPIC]	79.32	0.2469	19.58	49.26	0.2943	14.5	29.25	0.3248	9.5
Mode II [SEPIC]	39.19	0.1224	4.79	24.08	0.1447	3.48	14.18	0.1572	2.22

5. Conclusion

This paper has presented an efficient Dual Mode-Multiple Output (DMMO) converter for stand-alone PV system, based on SEPIC topology. The converter can provide a high step-up capability for power conversion systems. The main benefits of this topology include: continuous supply to the load; mode can vary according to distance and requirements; a high conversion ratio; allowing high switching frequency; it can be implemented in modular form and more levels can be added without changing the main converter; reducing input current ripple with a passive circuit; a single control scheme reduces circuit complicacy and control scheme is consolidated with input and output control strategy. Two operating modes with different states are analyzed and simulation is performed to show the effective operation of the proposed topology for PV applications.

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