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An Ultra-Low Quiescent Current CMOS Low-Dropout Regulator with Small Output Voltage Variations

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Abstract

An ultra-low quiescent current low-dropout regulator with small output voltage variations and improved load regulation is presented in this paper. It makes use of dynamically-biased shunt feedback as the buffer stage and the LDO regulator can be stable for all load conditions. The proposed structure also employs a momentarily current-boosting circuit to reduce the output voltage to the normal value when output is switched from full load to no load. The whole circuit is designed in a 0.18 μm CMOS technology with a quiescent current of 550 nA. The maximum output-voltage variation is less than 20 mV when used with 1 μF external capacitor.

Keywords

Ultra-Low Quiescent Current; Low-Dropout Regulator; Small Output Variations

1. Introduction

Power-management circuits are becoming more important in portable electronics systems such as smart phones, laptops, and tablets. The performance of these portable devices is increasing fast and the battery life is becoming the bottleneck for their development. So it is in great demand to design the power-management circuits with ultra-low power dissipation and a wide output current range.

For power-management system, low-dropout regulator is the most common block due to better load transient response, less noise, simpler and lower cost than the switching regulator counterparts [1]-[3]. However, when it comes to design an ultra-low quiescent current LDO, it is difficult to satisfy these characteristics. In a conventional low-dropout regulator, there are several specifications to describe the LDO's performance, such as line and load regulations, loop stability and transient response. When the whole LDO's quiescent current is low, the loop stability and transient response are sacrificed a lot due to the low frequency pole at the error amplifier output, the decreased loop bandwidth and the limited slew rate at the gate of power transistor. Furthermore, the demand of a large maximum load-current also affects the loop stability and transient response because it introduc-

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es a large capacitor at the gate of power transistor. The large capacitor will reduce the value of the parasitic pole present at the gate of the power transistor and require more sourcing and sinking currents at the gate to maintain the slew rate. Therefore, there are two main challenges in the ultra-low quiescent current design. One is the frequency compensation strategy for the stability under whole load-current range, and the other is how to achieve good transient response [4].

Different approaches have been reported to address the above issues. For frequency compensation, the conventional method is making use of the equivalent series resistance (ESR) of the output capacitor to create a constant zero for compensating the non-dominant pole [5] [7]-[9]. However, it may not be fit for LDO with wide load current requirement, because the frequency of the output pole will change a lot when the load current varies. In [1], an emitter-follower with small output resistance has been adopted to push the pole at the gate of the power device beyond the unity-gain frequency of the LDO loop. However, when the LDO is used to source a larger load current, more current are needed in its emitter-follower. Thus the resistance at the gate of the power transistor can be further lowered to compensate the larger gate capacitance. Further architecture is used in [3] [6] to push the pole at the gate of the power transistor to a higher frequency.

Both of the loop-gain bandwidth and the slew rate at the gate of the power transistor dominate the transient response of a LDO. There are typically two methods to raise the slew rate at the gate of the power transistor. One is using a smaller area power transistor [10], and the other is providing more sourcing and sinking currents at the gate capacitor. Many design approaches have been proposed to realize the current boosting at the gate of power transistor they can be classified into three techniques depending on the changing time of the biasing current. In [11], the biasing current is always high and independent of the load current. Obviously, this approach is not suit for low quiescent current design for the high biasing current at light load. Consequently, the adaptive-biasing technique which can increase the bias current according to the magnitude of the output current is proposed in [1] [3] [6]. To further reduce power dissipation in the steady state, dynamic biasing which only increases the biasing current at the transient instant when the output current is changed is presented [4] [5] [12].

This paper presents an ultra-low quiescent LDO regulator using an adaptive-biasing voltage buffer and an overshoot reduction network in 0.18 μm CMOS process. Section 2 discusses the structure as well as the stability of the proposed LDO regulator. In Section 3, the details of the circuit implementation of the proposed structure are described. Simulation results and conclusions are given in the last two sections.

2. Structure of the Proposed LDO

Figure 1 shows the proposed LDO regulator architecture. It comprised a folded-cascode error amplifier, an adaptive biasing voltage buffer, a power transistor M_P, an overshoot reduction circuitry, a frequency compensation network and a feedback network. The adaptive-biasing voltage buffer is employed for isolating the large parasitic capacitance at the gate of MP from the high impedance at the error amplifier output. It is also used for the slew rate enhancement. In addition, the overshoot reduction network can decrease the output voltage down to the normal value at no load condition.

Thanks to the low out impedance of the voltage buffer, the pole at the gate of power transistor is located at sufficiently high frequencies under different load currents.

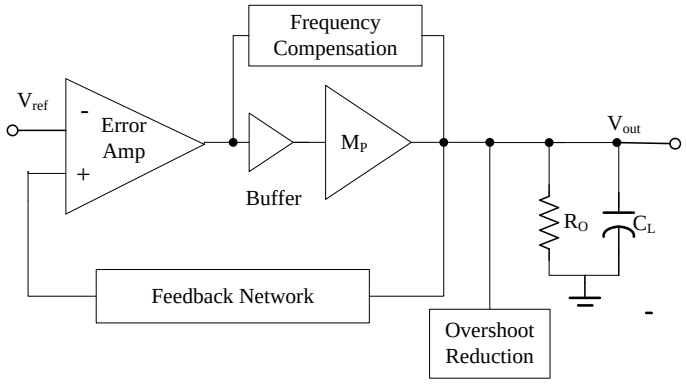

Figure 1. Structure of the proposed LDO regulator.

The stability of the whole system is achieved by cascode compensation technique, which allows the LDO to achieve wider unity gain frequency and enhanced power supply rejection [3]. The small-signal model of the proposed LDO is shown in **Figure 2**. Here, g_{m1} and g_{mp} represent the transconductances of input gain stage of error amplifier and power transistor respectively, R_1 is the output resistance of the error amplifier, C_1 is the input capacitance of the buffer stage, C_L is the output capacitance, and R_O is the equivalent resistance seen at the output of the LDO. The cascode compensation is formed by g_{mc} and C_C and only takes effect at heavy load. So at light load, the pole located at the output of the LDO is the dominant pole, and the pole located at the output of the error amplifier is the non-dominant pole. They are given by

$$p_{-3dB} = 1/(R_1 C_1) \tag{1}$$

$$p_{nd} = 1/(R_O C_O) \tag{2}$$

When the output load is heavy, the impedance at the output of LDO becomes small while the capacitor at the output or the error amplifier becomes large because of the enhancement of a Miller capacitance $(g_{mp}R_O)\,C_C$. So the above two poles will shift their positions at heavy load. The worst-case stability resides between light load and heavy load [6].

3. Circuit Design and Implementation

The full schematic of the proposed LDO is shown in **Figure 3**. The error amplifier is realized by a single folded-cascode stage with transistors M_0-M_8. The voltage buffer is formed by a source-follower M_{12}. And the transistor M_{14} is the feedback device connected in parallel to the output of M_{12} in order to reduce the output impedance. The adaptive biasing network is formed by transistor M_{15} and M_{16}, which is used for both compensation and slew rate enhancement. The feedback network is realized by a string of diode-connected PMOS transistors M_{18} - M_{21} biased in the sub threshold region to minimize quiescent as well as the silicon area. Transistor M_6 and capacitor C_C form the cascode compensation to make the LDO be stable under full load range. Finally, the overshoot reduction network is realized by R_b, C_b and transistor M_{17}. In a conventional LDO, when the load current suddenly decreases to zero, the diode-connected feedback network PMOS is the only path to discharge the extra current from power transistor M_P. So, even if the error amplifier reacts quickly to increase the gate voltage of M_P, the overshoot appears at the output would still take a very long time to recover to the nominal value. But with the help of overshoot reduction network, when the gate voltage of M_P suddenly increases, the change is sensed by C_b and is then coupled to the gate of M_{17}. Hence transistor M_{17} provides the second path to discharge the overshoot. When the gate voltage of M_P becomes steady, the gate voltage of M_{17} recovers to V_{b2} [4]. In steady state, the current flow through M_{17} is around 100 nA.

4. Simulation Results

The proposed ultra-low quiescent LDO regulator was designed and simulated in a 0.18 μm CMOS technology. The input voltage range of the LDO is designed from 1.8 V to 5.5 V and the output voltage is set to 1.6 V. The

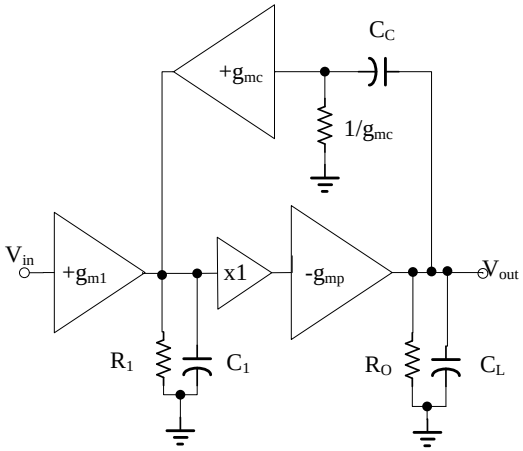

Figure 2. Small-signal modeling of the proposed LDO.

output capacitor is 1 μF. The output current range is from 0 to 100 mA when the dropout voltage is 0.2 V. The LDO consumes an ultra-low quiescent current of 550 nA under no-load condition, while a quiescent current of 135 μA is dissipated at full load condition.

The stability of the LDO under different load conditions was verified. **Figure 4** shows the simulated phase margin of the loop-gain transfer function under different load currents. The minimum phase margin is always larger than 54˚ for the entire range of load current.

Figure 5 shows the transient response of the proposed LDO when the load current is pulsating between 0 and 100mA with pulse rise and fall time of 1 μs. With the use of a 1μF output capacitor, the maximum output voltage variation is less than 20 mV when dropout voltage is 0.2 V, which includes output undershoots, overshoots and variations due to load regulation. It can be seen that the output voltage was hardly regulated to the nominal value without overshoot reduction. The line transient response is shown in **Figure 6**. The supply voltage changes between 1.8 V and 2 V in 10 μs with an output current of 100 mA. The simulated result shows that the total output voltage variations are less than 2 mV.

Finally, a comparison of some reported LDOs is given in **Table 1**. A figure of merit used in [3] is adopted here to compare the transient response of different LDOs. The smaller FOM value, the better is the transient performance metric. The proposed design achieves the smallest FOM value among the recently reported works.

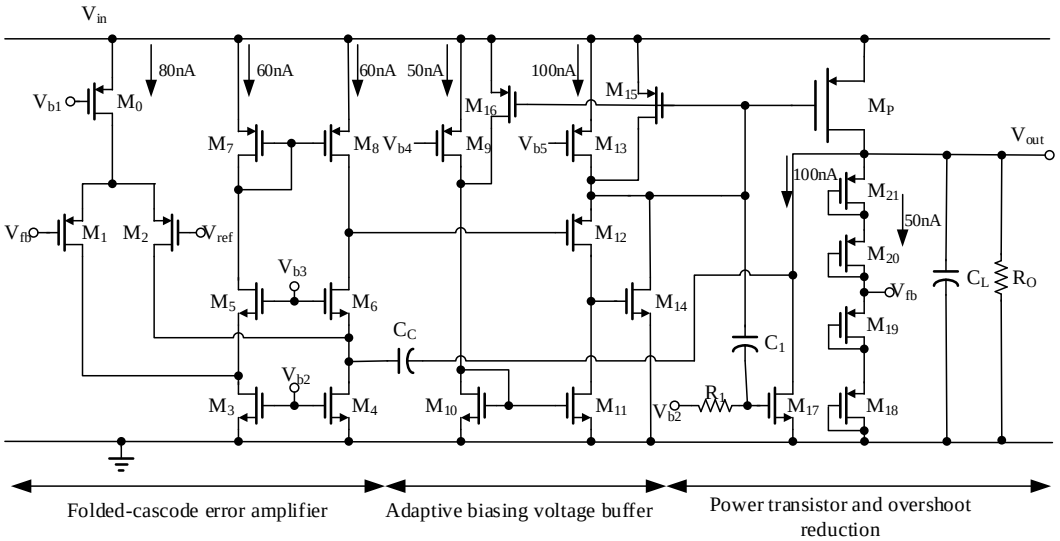

Figure 3. Schematic of the proposed LDO regulator.

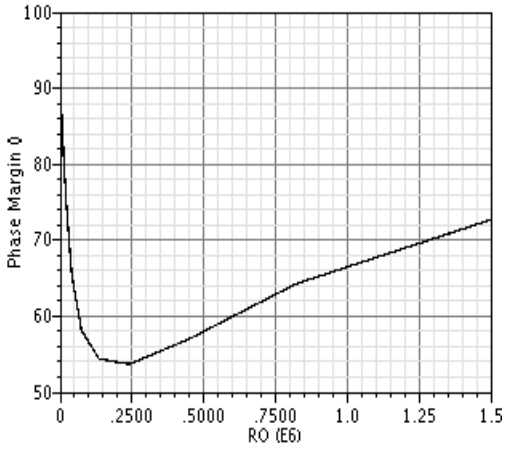

Figure 4. Phase margin of the proposed LDO loop-gain transfer function under different load currents with a 1 μF output capacitor.

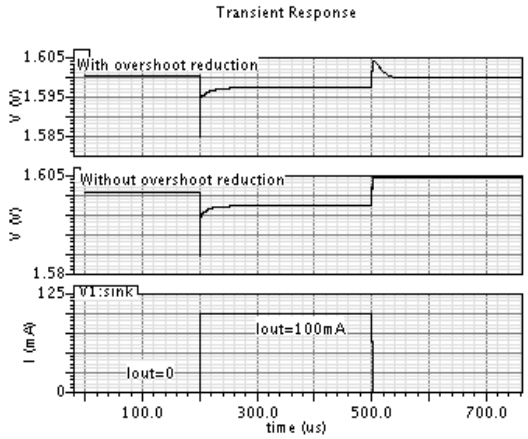

Figure 5. Simulated load transient response of the proposed LDO.

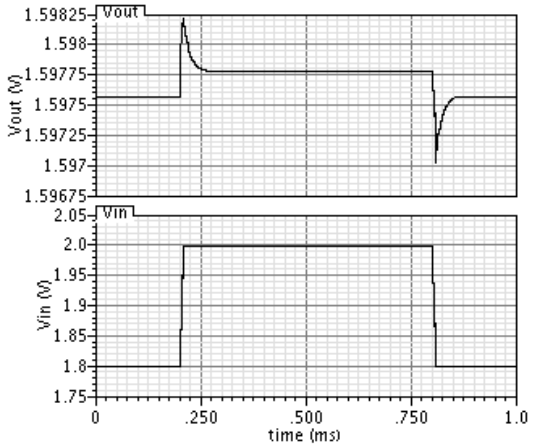

Figure 6. Simulated line transient response of the proposed LDO.

Table 1. Performance comparison with previously reported LDOs.

	[5] 2010	[6] 2011	[8] 2013	[9] 2013	This work
Technology (μm)	0.35	0.35	0.18	0.09	0.18
V_{in} (V)	2	3.3-7	1.8	1	1.8-5
V_{out} (V)	1.8	3	1.64	0.85	1.6
I_{max} (mA)	100	100	150	100	100
I_q (μA)	4	0.5	0.33	60	0.55
V_{do} (mV)	200	300	160	150	200
Load regulation (mV/mA)	N/A	0.15	0.33	0.28	0.03
C_L (μF)	1-10	1	13.125	1	1
ΔV_{out} (mV)	55	150	48	28	20
T_r (μs)	0.55	1.5	4.2	0.28	0.2
FOM* (ns)	0.022	0.0075	0.00924	0.168	0.0011

* $FOM = T_r(I_q / I_{L,max})$.

5. Conclusion

In this paper, an ultra-low quiescent current low dropout regulator based on an adaptive-biasing voltage buffer and an overshoot reduction network has been presented. The adaptive-biasing voltage buffer is employed both for frequency compensation and slew rate enhancement. In addition, an overshoot reduction net-work is used to regulate the output voltage back to its normal value when the output is switched from full load to no load. The LDO is able to source up to 100 mA of output current and dissipates only 550 nA quiescent current at no load condition.

Acknowledgements

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