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New Multilevel Mixed Topology Development to Improve Inverter Robustness for Domestic Photovoltaic Installations

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ABSTRACT

Multilevel inverters are well used in grid connected domestic photovoltaic applications because of their ability to generate a very good quality of waveforms, reducing switching frequency, and their low voltage stress across the power devices. However, this kind of inverter has to be modified to both limit common-mode currents and improve the robustness of the system. This paper presents a new mixed 5-level inverter that meets these challenges. The operating principle of the converter is proposed. Several experimental measurements are described to validate this new concept. The output voltage and current and the THD of the output voltage are particularly discussed.

Keywords: Domestic PV Applications; Common Mode Currents; Decoupling Capacitances; Mixed 5-Level Inverter

1. Introduction

The global market for solar photovoltaic (PV) systems using transformerless configuration has been growing over the last decade or more with an average rate from 30% to 40% per year. In particular, grid-connected PV installations contribute significantly to this average growth rate [1]. The technical performances and robustness of inverters are key elements that may have a significant impact on the generation of electricity and the profitability of domestic grid-connected PV systems.

PV inverters typically operate with a switching frequency of about 15 kHz. As can be seen in **Figure 1**, this frequency can be reflected to the DC bus and generate common-mode currents which flow through the metallic frame and the stray capacitances of the PV modules [2,3]. These parasitic capacitances are key contributors of a resonant circuit which consists of the PV modules, the AC filter elements and the grid impedance. The value of these stray capacitances, which could reach 150 $nF \cdot kW^{-1}$, depends on weather conditions, PV topology, PWM pattern, the material used in the metallic frame and the passive elements of the converters [4]. The transformerless configuration for PV systems could result in safety problems particularly when leakage currents appear at the positive and negative PV terminals. The DIN VDE 0126-1-1 document specifies that the maximum leakage ground current is equal to 300 mA [5]. Regarding domestic applications, the UTE C 15-712 standard requires the use of 30 mA differential circuit breaker inside the PV installation. However, the leakage current can increase over 30 mA that leads to the installation shutting down. So, the limitation of common-mode currents has become an important challenge.

NPC (Neutral Point Clamping) topologies are well-known converter structures that are able to eliminate common-mode currents because the middle point of the DC source is fixed (*i.e.* clamped by diodes). Therefore, no leakage current can be generated [6,7]. In symmetrical configuration, 5-level NPC inverter enables to significantly improve the Total Harmonic Distortion (THD) of the output voltage and current and decrease the voltage constraints across the semiconductor devices in comparison with the H-bridge converter topology. However, 5-level NPC inverter requires the use of 4 decoupling capacitors, 8 power switches and 6 clamping diodes that could considerably increase the complexity and cost-effectiveness of the system. It is important to notice that the electrolytic capacitors, used for power decoupling between and the single-phase grid, are the main limiting components inside the inverter. Equation (1) shows that the operational lifetime (L_{OP}) of the decoupling capacitor depends on the hotspot temperature (T_h). The $L_{OP,0}$-parameter is the lifetime at a hotspot temperature of T_0. The ΔT-parameter is the temperature increase that reduces the lifetime by a factor of two [8].

$$L_{OP} = L_{OP,0} \times 2^{(T_0 - T_h)/DT} \quad (1)$$

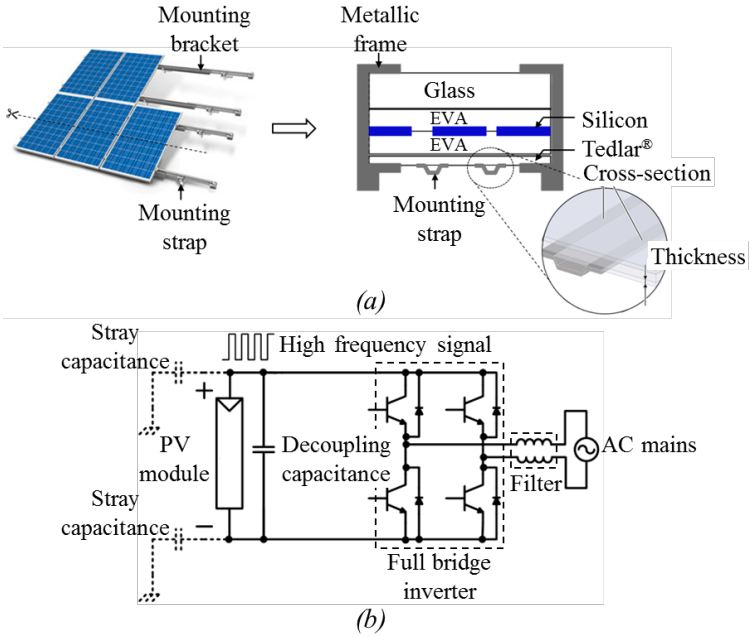

Figure 1. (a) Constitutive elements of a single-glass PV module; (b) Common-mode current generation (example of a PV plant using a full bridge inverter).

This article presents a new mixed 5-level inverter to limit common mode currents, while at the same time generating adequate robustness (limitation of decoupling capacitances and semiconductor devices) and cost-effectiveness of the system. The advantages of this new converter are pointed out and compared with 5-level NPC topology. A 500 W demonstrator is particularly proposed to validate the concept.

2. 5-Level NPC Inverter Limitations

2.1. Operation Principle Reminder

The conceptual schematic of 5-level NPC inverter used in symmetrical configuration is given in **Figure 2(a)**. Four DC voltage sources are needed for generating an output voltage composed of 5 levels (*i.e.* 0, +E/2, +E, −E/2, −E). The amplitude of each DC source is equal to +E/2.

A widely used method to control inverter connected to the grid is the Pulse Width Modulation (PWM) and particularly, Sinusoidal Pulse Width Modulation (SPWM) [9]. This method is used to ensure that output signal quality is as close as possible. It means that harmonics must be shifted to higher values to improve the Total Harmonic Distortion (THD) of the output voltage and current. The control of the inverter consists in comparing a sinus-shaped modulating signal with four triangular carriers. As can be seen in **Figure 2(b)**, the "Tri_1" and "Tri_2" carriers enable to generate the output voltage levels equal to +E/2 and +E respectively. In a symmetric set-up, the level equal to −E/2 and −E are induced by the "Tri_3" and "Tri_4" carriers respectively. The switching conditions of each controllable device are summarized in **Table 1**.

2.2. Advantages and Limitations

5-level NPC inverter used in symmetrical configuration helps to limit the voltage constraints across the semiconductor switches (off-state voltage equal to E/2). In particular, these constraints are two times lower than 3-level NPC inverter ones. The NPC function enables to eradicate the common-mode currents.

Despite all the advantages mentioned previously, 5-level inverter has major limitations. Firstly, four PV sources are needed to supply the DC-AC converter. The amplitude of each voltage source has to be equal to E/2. Secondly, four decoupling capacitances and four MPPT (Maximum Power Point Tracking) stages must be used. Finally, the 5-level inverter is composed of 8 controllable power switches and 6 clamping diodes. To conclude, the number of conversion stages, active (power switches and clamping diodes) and passive elements (decoupling capacitors) is too high. Since the reliability of these capacitances is a critical factor, it is necessary to propose alternative topologies to increase the robustness of grid-connected PV inverter.

3. New Mixed 5-Level Inverter Proposal

3.1. Theoretical Analysis

Figure 3 shows the electrical schematic of the new mixed 5-level inverter. This new topology is based on

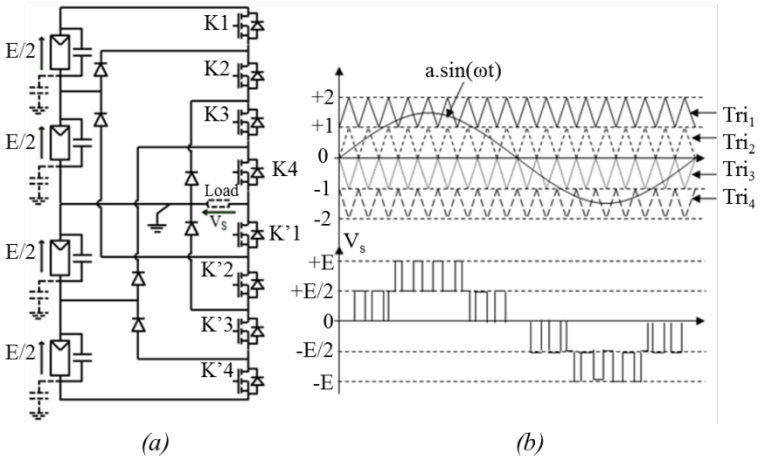

Figure 2. Conceptual schematic (a) and control principle (b) of a 5-level NPC inverter used in symmetrical configuration.

Table 1. Switching conditions of each controllable device of the 5-level NPC structure used in symmetrical mode.

Switching conditions	Devices in On-state	V_s
$Tri_3(t) < a.\sin(\omega t) < Tri_1(t)$	K'1, K'2	0
$a.\sin(\omega t) > Tri_1(t)$	K'1, K'2, K'3	+E/2
$a.\sin(\omega t) > Tri_2(t)$	K'1, K'2, K'3, K'4	+E
$a.\sin(\omega t) < Tri_3(t)$	K2, K3, K4	−E/2
$a.\sin(\omega t) < Tri_4(t)$	K1, K2, K3, K4	−E

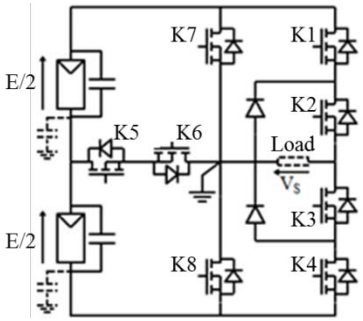

Figure 3. Conceptual schematic of the new mixed 5-level inverter.

one 2-level leg (composed of K7 and K8) coupled with 3-level NPC one (composed of K1, K2, K3, K4 and the two clamping diodes). The K5 and K6 power switches allow a bidirectional current and voltage operating mode because of the symmetrical configuration of the converter (one phase inverter). Thus, the new mixed 5-level inverter is composed of 8 controllable semi-conductor devices (the same number as the 5-level NPC inverter one) and 2 clamping diodes (3 times lower than the 5-level NPC inverter one). Most important, the number of decoupling capacitances is divided by 2 compared with 5-level NPC inverter used in symmetrical configuration. The control technique of the new converter is the same as 5-level NPC inverter one. The switching conditions of each controllable device are summarized in **Table 2**.

Table 2. Switching conditions of each controllable device of the new mixed 5-level inverter.

Switching conditions	Devices in On-state	V_s
$Tri_3(t) < a.\sin(\omega t) < Tri_1(t)$	K2, K3	0
$Tri_1(t) < a.\sin(\omega t) < Tri_2(t)$	K1, K2, K5, K6	+E/2
$a.\sin(\omega t) > Tri_2(t)$	K1, K2, K8	+E
$Tri_4(t) < a.\sin(\omega t) < Tri_3(t)$	K3, K4, K5, K6	−E/2
$a.\sin(\omega t) < Tri_4(t)$	K3, K4, K7	−E

3.2. Demonstrator Presentation

Figure 4 shows the demonstrator of the new mixed 5-level inverter. A SPWM technique is used to control the DC-AC converter. A digital interface provides the formatting of control signals. An analog control is implemented to adapt the signal generated to the power semiconductor devices while managing dead-time. A dsPIC30F6010A Digital Signal Processor (DSP from Microchip) enables to generate independently 4 PWM signals. It means that the output of the DSP operate in an independent manner and particularly, without any interaction from the main program uploaded into the processor. The DSP is coded in C using the free MPLAB environment by Microchip. The PWM function operates as follows. Firstly, a triangular carrier is generated. A constant enables to fix the duty-cycle. This constant value is loaded into a register and then, compared with the triangular signal. The result of this comparison generates TTL logic (0 V DC or 5 V DC) with constant duty-cycle. As mentioned previously, the mixed 5-level inverter is controlled by SPWM technique. The sinusoidal modulating signal (signal frequency equal to 18 kHz) is discretized in the form of data list and loaded into the register. The logic output of each PWM signal is thus the end result of the comparison between the sinusoidal-shaped modulating signal and the triangular carriers.

An analog circuit is implemented to create the drive

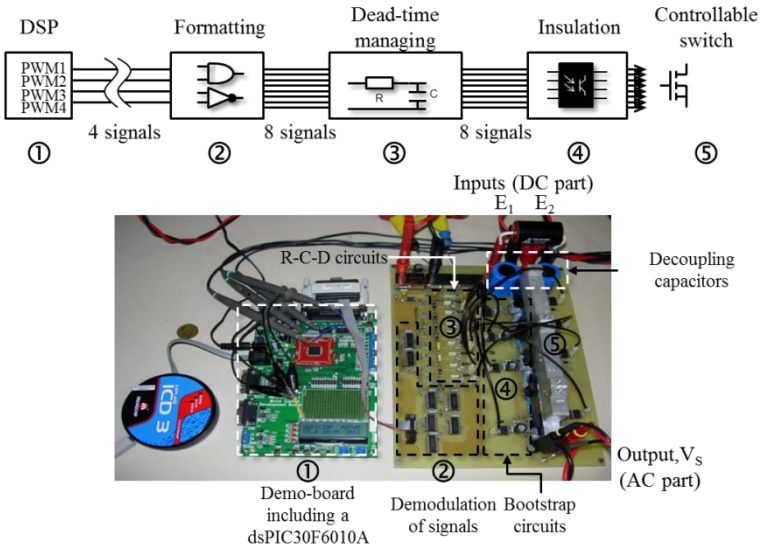

Figure 4. New mixed 5-level inverter demonstrator.

signals to control 8 power switches from the PWM signals generated by the DSP. This analog circuit is composed of a formatting stage, an R-C-D circuit that is able to manage dead-time and an amplitude adjustment stage (voltage and current of the control signals). AND, OR and NAND logic gates (74HC08, 74HC32 and 74HC04) are responsible for the formatting of the signals from the DSP. The manufacturer of these logic gates gives the signal propagation delays about 7 ns. The R-C-D circuit, that manages dead-time, is used to avoid any combination (*i.e*. simultaneous control of the following power switches: [K5; K6; K7], [K5; K6; K8], [K7; K8] or [K1; K2; K3; K4]) that could lead to the voltage source short-circuit during the switching phases. It is important to notice that the delay is active for each rising edge of the drive signal (a diode is connected head-to-tail from the gate resistor).

The new mixed 5-level topology requires a floating and insulated control circuit. The bootstap technique is used to generate 6 floating supplies (for K1, K2, K3, K4, K7, K8) [10,11]. Regarding the control of K5 and K6, an insulated voltage source is selected because the bootstrap is not able to generate a common reference for the other power devices. Optocouplers (HCPL-3101 from Agilent with the signal propagation delays and the output current equal to 0.3 µs and 400 mA respectively) enable to create the insulation of the control circuit.

The power part of the inverter is composed of eight 650 V, 33 A, 70 mΩ super-junction MOSFETs (STP42N65M5 from STMicroelectronics) and two 600 V, 60 A, ultra-fast and soft recovery (recovery time equal to 75 ns) diodes (60APU06 from International Rectifier). The diodes of the NPC leg must conduct the current as quickly as possible. That is the reason why the soft recovery diodes are used. All the power devices mentionned previously have been designed as to ensure that the inverter may operate for 3 kW domestic PV installations.

3.3. Experimental Measurements

Several experimental measurements have been performed to validate the new inverter concept functioning. Two 150 V, 10 A DC generators are used to power the demonstrator. The peak input power of the inverter is about 500 W. The output current is set up with a rheostat. The measurements have been done with 500 MHz digital oscilloscope (TDS5054 from Tektronix). Voltages and currents have been measured using differential probes (P5205 from Tektronix, 100 MHz bandwith) and DC coupled current probe (TCP202 from Tektronix, 50 MHz bandwith) respectively. The output voltage and current THD have been determined indirectly. Firstly, the output voltage and current have been measured. Then, the graphs have been drawn up with the LTspice post-processing tool. Finally, output voltage and current THD have been calculated using the LTspice simulator.

Figure 5 gives the output current and voltage that demonstrate the proper functioning of the DC-AC converter. The graph clearly shows that the output voltage is composed of 5 levels. Its RMS value is about 220 V. The RMS value of the output current is about 2 A with little variation induced by the inductive behavior of the rheostat. The measurement of the inverter efficiency has been carried out using two High-End Digital Multimeters with Power and Energy Measurement (METRAHit29S from METRAHIT ENERGY, measurement accuracy equal to 0.1 W). Its value is equal to 90%. It is important to notice that no design optimization of the prototype has been done.

Figure 6 shows the comparison between the mea-

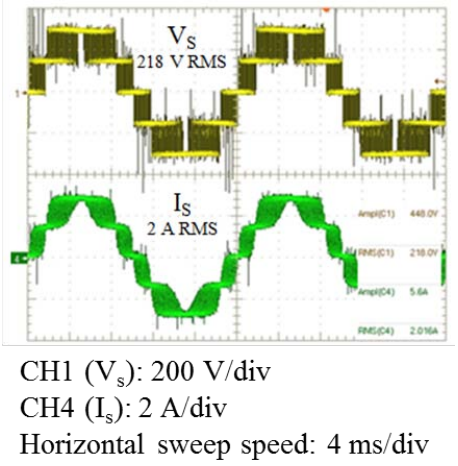

Figure 5. Output measurements (voltage and current) of the new mixed 5-level inverter.

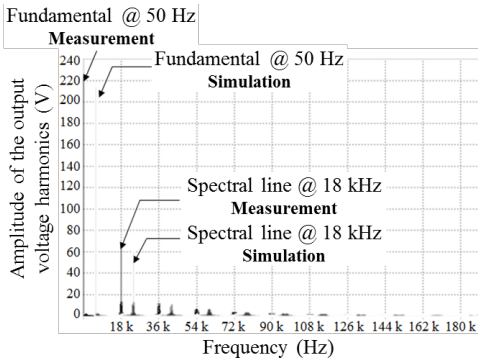

Figure 6. Comparison between the measurement and the simulation of the output voltage harmonic spectrum of the new mixed 5-level inverter.

surement and the simulation of the output voltage harmonic spectrum. This spectrum is composed of 50 Hz fundamental frequency, the other spectral lines being harmonics of the modulation frequency (*i.e*. 18 kHz). Operation, the output voltage THD, extracted using the indirect method as mentioned previously, is about 26%. This value is comparable with that which would obtain if experimental measurements were done on 5-level NPC inverter in symmetrical configuration. **Figure 6** shows also the simulated output voltage harmonic spectrum is broadly similar to the measured one (the dispersion of the results is about 4%) [12].

3.4. Discussion

The concept of the new mixed 5-level inverter described in this paper has been validated through many experimental measurements. The output voltage and current correspond to what might be expected on the basis of an assessment of need. This new architecture allows keeping the same characteristics in terms of power quality (voltage and current THD) as the 5-level NPC inverter ones. The design of this new topology is much easier (2 NPC diodes instead of 4, 8 controllable switches, 2 DC sources instead of 4, 2 decoupling capacitors instead of 4) making the inverter more robust (lower decoupling capacitors) and cost-effectiveness (low number of semiconductor devices).

However, it should be noticed that all the power switches are not subjected to the same voltage constraints during the on-state. Some of them have to hold the full voltage (*i.e*. E), while others hold half of the DC voltage (*i.e*. E/2). This is not the case for the 5-level NPC inverter, since the voltage across each power device is equal to E/2.

Some points remained open for improvement, including the design of the prototype to maximize the efficiency of the inverter and to increase its nominal power (e.g. 3 kW typically used for domestic PV plants).

4. Conclusions

In this paper, a new mixed 5-level topology has been proposed to improve the robustness of inverter used in domestic photovoltaic applications. This new inverter is based on the mixture between a 2-level H-Bridge converter and a 3-level NPC structure

The new mixed 5-level structure operation has been validated through experimental measurements. The measurement results help to highlight the advantages of this new topology compared with existing multilevel DC-AC converters. In particular, the new mixed 5-level inverter may ensure the best compromise between common-mode current limitations (via the 3-level NPC leg), the number of DC sources (2 voltage sources) and semiconductor devices (8 controllable switches and 2 NPC diodes) to optimize the cost-effectiveness of the system, the limitation of decoupling capacitors (2 decoupling capacitances) to increase the robustness of the system and the voltage constraints across the power switches during the off-state (may be higher than 5-level NPC inverter ones).

Additional measurements are required to complete the analysis, including the design optimization of the structure to increase its nominal power (e.g. 3 kW typically used for domestic grid-connected PV installations) and its efficiency.

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