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A New Analyzing Method of Single Event Latch-Up Protection Circuit Based on Current Comparing and Its Performance Verification

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Abstract

Single event latch-up (SEL) is a significant issue for electronics design in space application, which would cause large currents in electronic devices, and may lead to burning out of devices. A new monitoring circuit based on current-comparing method is designed to protect the electronics away from SEL's damage in radiation environment. The response time of protection circuit has been analyzed. The signal simulation results indicated that the operating time of the SEL protection circuit is dependent on the action time of current comparator and system application recovery time. The function of the monitoring circuit protection device away from SEL's damage has validated through experiment at last.

Keywords

SEL Protection Circuit, Power-On Time, Cut-Off Time, Adjustable Recovery Time, COTS

1. Introduction

With the development of satellite technologies, there has been highly increasing demand for lower power and more cost-effective spacecrafts. For this reason, more and more spacecrafts try to employ commercial-off-the-shelf (COTS) electronics, due to the high performance, short delivery time and low cost [1] [2]. However, since there is no radiation hardened technology applied in manufacture of (COTS) electronics, COTS technologies are

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vulnerable to total ionizing dose (TID) and single event effects (SEE) in the space radiation environment, especially to SEL [3]-[5]. In order to reduce the risk of using COTS components in space application, radiation hardening techniques need to be taken.

High-energy particles (include protons cosmic rays) cannot only generate soft errors, but also cause SEL. The mechanism causing SEL is similar to the mechanism for electrical latch-up, and the difference is that SEL is triggered by radiation-induced charges. SEL is a potentially destructive condition involving parasitic circuit elements forming a silicon controlled rectifier (SCR). The consequences of an SEL are often more severe than that of a soft error because a power-reset is required, and the IC can be permanently damaged if not currently limited and removed "in time". Also, SEL is extremely hazardous to electronics in space environment, causing permanent damage to electronics or hardware in an ultra-short time due to the emergence of high currents [6] [7]. These permanent damages can induce partial malfunction or instrument failure of spacecrafts [8] [9]. Therefore, a removal of power from the device is required in all non-catastrophic SEL conditions in order to recover device operations

The SEL rate increases significantly with increasing supply voltage and with increasing operating temperature [10]. Theoretically, decreasing supply voltage and controlling temperature would reduce the SEL rate when coming to space design. However, to decrease supply voltage and temperature-controlling could not only eliminate SEL, but also affect the circuits, even the system performance. There are the other two methods which can protect COTS devices away from SEL's damage. One method is using resistance to limiting current, which can mitigate SEL [11]. However, this makes the designer's job difficult in specifying the required current limit [12]. Large value of the resistance will affect the normal work of circuit, whereas small value may fail to provide protection. The second method is using cut-off circuits based on current comparison. Integrated circuits for single event latch-up protection have published [13] [14], but the action time of protection process is not mentioned.

In this paper, a design method of SEL protection circuit has been presented based on the current comparison. The time has been analyzed about protecting response process of the designed-circuit that has been analyzed. Heavy ion irradiation tests have been investigated to check the function of this new designed circuit. The result shows that this new designed circuit can automatically provide device protection far away from SEL's damage during heavy ion irradiation. Finally, the application note of this SEL protection circuit has been discussed.

2. Methodology

2.1. Design Principle of Protection Circuit

The construction of design principle diagram of SEL protection circuit is shown in **Figure 1**. The protection circuit is mainly composed of four parts: current sensing resistor, integrated circuit voltage regulator, DSP control unit, dual D flip-flop and amplification comparison circuit.

According to its operation principle, the input voltage passes through current sensing resistors, then the current from resistors are changed into voltages by amplification comparison circuit. The output signal state from Dual D flip-flop which are control output voltage from integrated circuit regulator is dependent on the compared result. Normally, the comparison output of operational amplifier is high level, then output signal state is high level, so the voltage regulator is powered normally and output normal voltage. Once SEL is happen, the current is soaring in short time, the voltage which amplified by amplifier circuit has changed, Then the low level signal state is output by Dual D flip-flop when compared to threshold voltage. Further, the output voltage from integrated

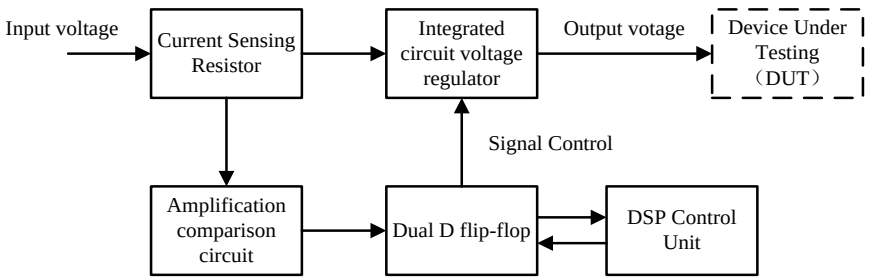

Figure 1. Schematic diagram of SEL protection circuit.

circuit voltage regulator is cut off, and then the DUT is powered off. When Dual D flip-flop became low level, the DSP control units sent a signal which can make Dual D flip-flop convert into high level, then integrated circuit voltage regulator output normal voltage for DUT. The Devices which are sensitive for SEL would be protected by this circuit.

2.2. Operating Time Analysis

There are three working state for this latch-up protection circuit, which are "current cut-off", "adjustable recovery time" and "power-on time", respectively, as shown in **Figure 2**.

When current was increased beyond the reference value, the regulator output voltage would be cut-off by the signals which are enabled from D flip-flop. The time during this progress is recorded as T_{off}.

$$T_{off} = T_{C1} + T_{PHL} \tag{1}$$

T_{C1} is for the output up-set time from current comparator when the currents was beyond reference value, T_{PLH} is the output upset time from D flip-flop.

When DUT's current get to 0 mA, the control unit would be sent a low signal to D flip-flop, and DUT will be powered on while preset side of D flip-flop sent control asynchronous set to "1". The time from the start of electrification to back to normal working current is recorded as power-on time T_{on}.

$$T_{on} = T_{C2} + T_{PLH} \tag{2}$$

T_{C2} is for the output up-set time from current comparator when the currents get to 0 mA, T_{PHL} is for the output upset time from D flip-flop. The value of T_{PLH} and T_{PHL} are shown on **Table 1**.

The simulation output waveform of comparator from SEL protection circuits form **Figure 3**. The action time of comparator, set as $T_{C1} \approx 30\ \mu S$. From **Table 1**, the T_{PLH} and T_{PHL} are both at 40 ns, are far smaller than T_{C1}. And T_{C2} and T_{C1} are from the one comparator, and means the same action, so the $T_{C2} = T_{C1}$, Then the formula (1), (2) can be set as:

$$T_{off} = T_{C1} + T_{PHL} \approx T_{C1} = T_{C2} \approx T_{on}$$

So

$$T_{off} \approx T_{C1} \approx T_{on} \tag{3}$$

The time between cut-off current to 0 mA and Power on DUT's current form 0 mA is called recovery time, set as T_R, it can be adjustable when comes to different application circuits. Then the total time from SEL happened

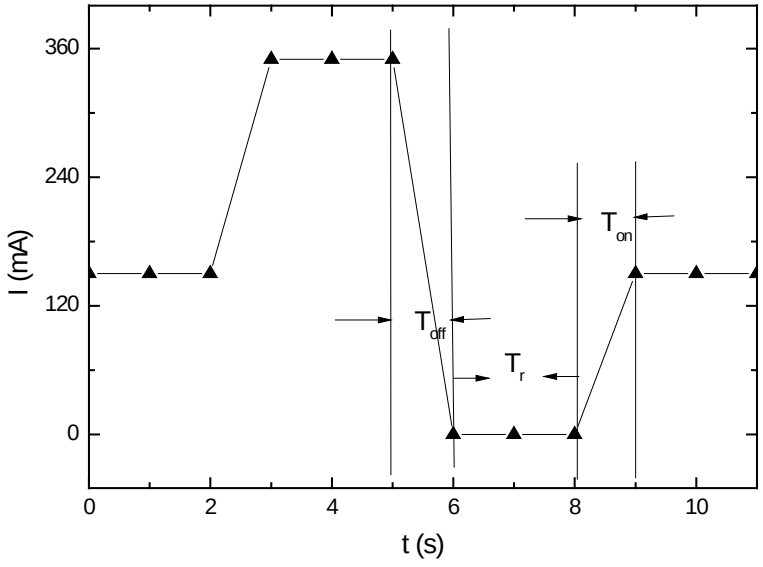

Figure 2. Schematic diagram of operating principle of SEL protection circuit.

Table 1. The parameter value from D flip-flop [15].

Code	Parameter name	Reference value			Test Conditions	units
		min	normal	max		
t_{PLH}	Time from "0" to "1"	/	13	25	$V_{CC}=5.0$ V, $C_L=15$ PF, $R_L=2$ KΩ	ns
t_{PHL}	Time from "1" to "0"	/	25	40		

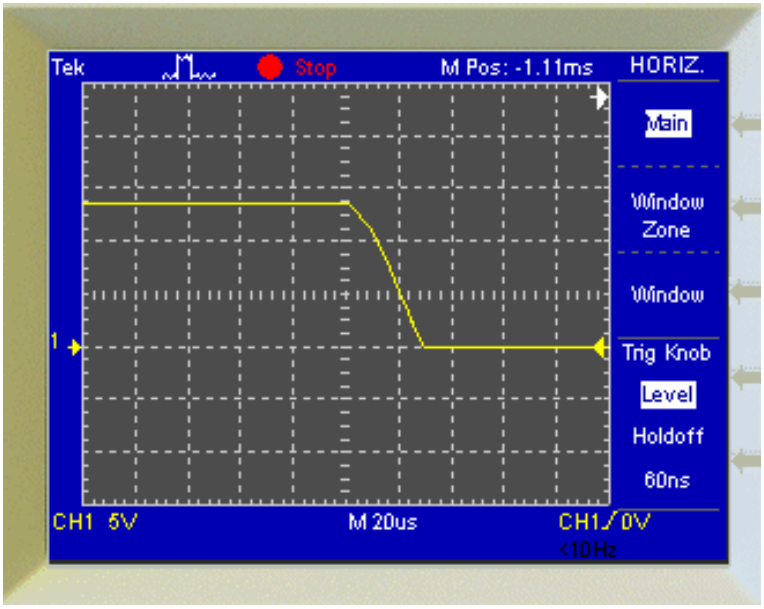

Figure 3. The simulation output waveform of comparator from SEL protection circuits.

to DUT Power-on can be expressed as follows:

$$T_{total}=T_{off}+T_{on}+T_R=T_{C1}+T_{C2}+T_{PHL}+T_{PLH}+T_R\approx 2T_{C1}+T_R \quad (4)$$

So the Total time of the SEL protection circuits which are from cut-off current to power-on device is depended on T_{C1} and T_R.

2.3. Sample Description and Test Conditions

Internal chip of DDS device is plastic encapsulated device made by CMOS technique, and 2 samples were used. The device was de-capped before the irradiation. The device's SEL LET threshold was between 9.31 and 13.6 MeV·cm^2/mg. The device sample information is shown in **Table 2**.

The test was conducted in the vacuum environment from electrostatic tandem accelerator HI-13 of China Institute of Atomic Energy, and adopted perpendicular irradiation. The characteristics of test ion are shown in **Table 3**. For the test, the ion fluence rate was set as about 7500 ions/cm^2·s^1.

3. Result and Discussion

Arsenic ions are selected as the irradiation heavy ion for evaluating SEL protection circuit as mentioned above. During irradiation, the supply current of tested chip is set as 500 mA. Automatic sampling records are made to automatically record the SEL, current cut-off and power-on phenomena every 10 seconds during irradiation test.

As shown in **Figure 4**, the work stable current of DDS is 150 mA at beginning, and the current suddenly increased to 300 mA after about 3 s, and keeping on about 2.5 s. During these time, the protection circuit is not working since the value of current isn't come up to pre-designed value when the work current is shapely down to the 0 mA at about 00:05:30 s, this mean that SEL on DDS was happened, and the protection circuit was cut-off

Table 2. Device sample description.

Progress Technique	Sample Size	Date Code.	Sample No.	Package
CMOS	2	0704	5#,7#	TQFP-100

Table 3. Characteristics of test ion.

Ion	Energy in MeV	Surface LET in MeV.cm^2/mg	Rang in μm (Si)
As	215	38.5	30.65

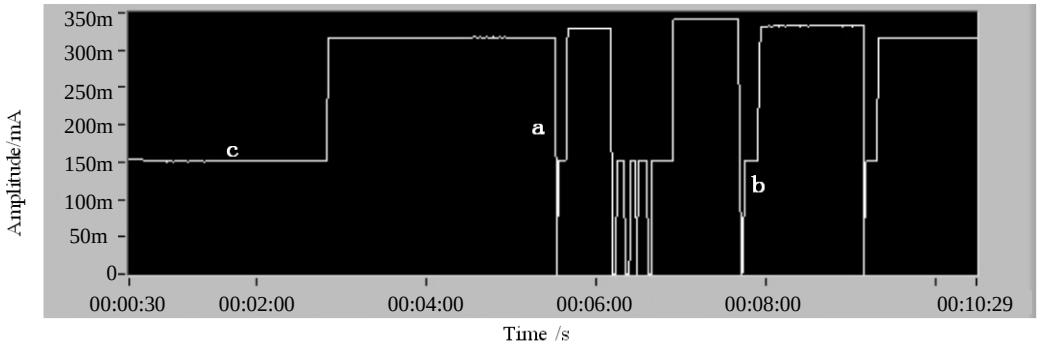

Figure 4. Working conditions of protection circuit at the recovery time of 300 ms from No5 device. (Note: "a" Means cut-off: when SEL happen, the current fall; "b" Means turn-on: when device power-off, the current rise; "c" Means device work on the stable current.)

the work current, then after 300 ms, the device was powered-on by protection circuit. These are full progress which records automatically SEL detective, power-off, recover time, and power-on. There are three working states, which are "fall", "rise" and "stable current", respectively, as shown in **Figure 4**. Therefore, it can be concluded that this new designed protection circuit has ability of power-off protection and restart functions against SEL effect.

For different system applications, the recovery time are required differently. The test results based on recovery time of 50 ms are shown in **Figure 5**. The only difference between the two recovery times is the time under 0 mA, which is longer under 300 ms than that under 50 ms. So different recovery time could be sited for requirement of systems application.

The cut-off time and Power on time is at microsecond level, which are not approved from verification test experiments, because of low current sampling precision of the test system. The recovery time which is adjustable from protection circuit should be more considered for system's normal working requirements. So most system whose signal responsive requirement are above 50 ms can choose this SEL protection circuit, but those whose signal responsive requirement are below 50 ms should be more careful to choose this SEL protection circuit. According to the experimental results, it's obvious that the new designed SEL protection circuit can automatically perform the "power-off" and "power-on" on latched devices without the help of any additional system resources, and this method can widely promote the application of COTS devices which are sensitive to SEL in space radiation environment.

From formula (4), the total time of SEL protection circuit from the occurrence of latch-up to the device's return to normal work state is dependent upon the action time of comparator and recovery time. The action time of comparator is at microseconds, and recovery time is adjustable for its different application. So the minimum processing time of SEL protection circuit is at microseconds. It is important that the needs of system minimum response time should be considered in order to avoiding the impact on application of back-end circuits for its long protecting response time.

4. Conclusions

In the paper, the design method of SEL protection circuit has been presented, and the validation of this circuit

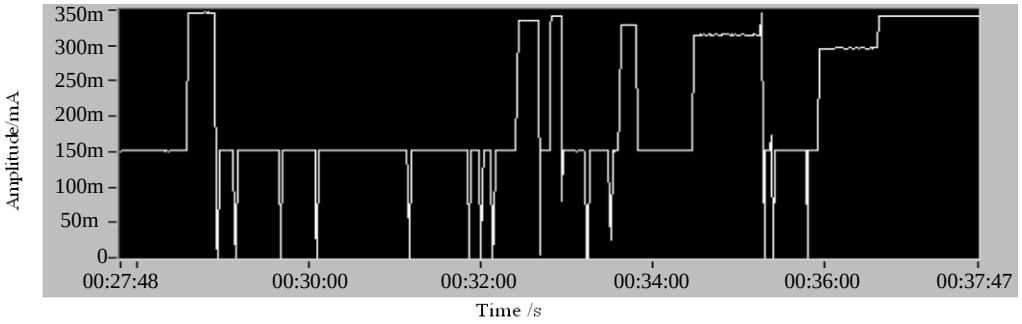

Figure 5. Working conditions of protection circuit at the recovery time of 50 ms from no7 device.

has been evaluated from arsenic ions' irradiation on SEL sensitive device. Base on circuit analysis and the experimental results, conclusions can be made as follows:

1) The time of protecting process of designed SEL protection circuit which based on current comparing method is at microseconds, which is dependent mainly on the action time of current comparator.

2) The designed SEL protection circuit can automatically perform "power-off" and "power-on" protecting action for the SEL sensitive devices to mitigate SEL.

3) The minimum response time from system needs should be considerate on this designed circuit to avoiding the impact on application of back-end circuits for its long protecting response time.

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