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Design and Implementation of a Novel Digital Frequency Superposition Testing Power Supply for Induction Motor

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ABSTRACT

A novel design and implementation of frequency superposition testing power supply for induction motor is proposed. An equivalent power using dynamic space voltage vector synthesis is generated to replace the two separate powers of the traditional method. The principle of frequency superposition testing is firstly introduced, and then the detailed design and implementation of the digital frequency superposition power are given. The simulation of the power supply system shows the promising results. Finally, experimental results validate the feasibility and reliability of the proposed power.

Keywords: *Digital Power, Frequency-Superposition Testing, SVPWM*

1. Introduction

Currently, there are two main methods for temperature rising testing which is an important index of induction motors. One is direct loading testing; the other is frequency superposition testing [1]. When a direct loading testing is performed, a duplicate motor must be coupled with the tested induction motor mechanically. However, for a large scale induction motor, it's difficult to add a rated load on the shaft and it's not safe. Frequency superposition testing is an equivalent loading testing with out a duplicate motor coupled. The tested induction motor is fed with two separate voltage sources of two different frequencies. When a frequency superposition testing is performed, the most sophisticated case is that the two power supplies are supported by a dynamotor. There must be at least 4 to 5 operators to operate it. Another drawback is that the dynamotor runs with a big noise.

This paper designs and implements a digital frequency superposition testing power supply by using open loop constant volts per hertz control based on SVPWM (Space Vector Pulse Width Modulation). The reference voltage is synthesized with the main reference voltage and the auxiliary reference target voltage by using parallelogram rule. The two reference voltages are controlled via a HMI (Human Machine Interface) client.

The concept of frequency superposition testing is simply described in Section 2. The method to generate a synthesized voltage vector using space voltage vector synthesis and the digital implementation of the frequency superposition testing power supply are described in Section 3. The simulation and the experiment results of the power supply proposed are given in Section 4, Section 5 respectively. The conclusion is presented in Section 6.

2. Traditional Frequency Superposition Testing Power

In the traditional frequency superposition testing [1,2], the tested motor is fed with two independent powers coupled with a transformer. Figure 1 shows the schematic of the traditional frequency superposition power with dynamotor fed. Traditionally, the auxiliary frequency is (80% - 120%) times of main frequency. Under the synthesized power supply, the voltage, current, speed, flux of the tested motor run with a beating frequency. When the synthesized stator flux runs faster than the rotor's, the tested motor runs as a motor, when the synthesized stator flux runs slower than the rotor's, the tested motor runs as a generator. The RMS (Root Mean Square) values of the stator currents increase while the auxiliary voltage increases. Until the RMS values of the electrical parameters are around the rated values. The motor works as a rated load added on its shaft.
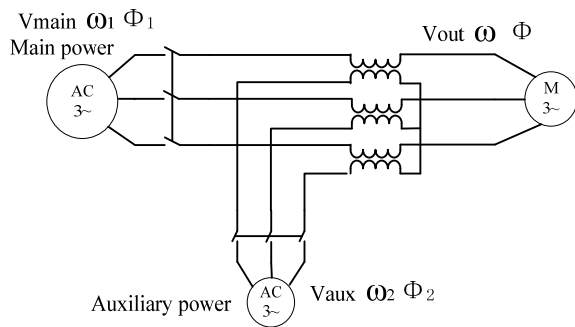
Figure 1. Schematic of the traditional frequency superposition testing with dynamotor fed for induction motor

3. Design and Implementation of the Digital Frequency Superposition Testing Power Supply

3.1 Design of the Proposed Frequency Super-Position Testing Power Supply

The hardware diagram of the proposed power has been shown in Figure 2. The hardware system consists of 1 power converter unit, 1 digital control board, 1 power analyzers and 1 HMI client.

The drive is based on TMS320LF2812 DSP platform. The main and auxiliary reference voltages are sent to the control board from the HMI client.

3.2 Implementation of the Power Converter Unit

The structure of the proposed three-phase voltage source power converter is shown in Figure 3. Uu, Uv and Uw are the output voltages. S1…S6 are the six IGBTs that shape the output, which are controlled by Su+ and Su-, Sv+ and Sv-, Sw+ and Sw-. When an upper IGBT is switched on, the corresponding lower IGBT is switched

off, i.e., when Su+, Sv+ or Sw+ is 1.the corresponding Su-, Sv- or Sw- is 0. The on and off demonstrates the states of the up transistors S1, S3 and S5.

There are eight possible combinations of on and off patterns for Su+, Sv+, Sw+. The derived output phase and line-to-line voltages in terms of DC supply voltage Udc are shown in Table 1.

The objective of SVPWM technique [3] is to approximate the reference voltage vector Uo by a combination of the eight switching patterns. One combination is shown in Figure 4.

For every PWM period, the desired reference voltage Uo can be approximated by having the power converter in two adjacent switching pattern U_x, U_{x+1} of T1 and T2 duration, respectively. The output voltages are decided by the selection of the duration time T1 and T2. The output voltage space vector is shown in Figure 5.

3.3 Synthesis of the Output Reference Voltage

Figure 6 shows a synthesis of the dynamic space voltage vectors.

According to Figure 6, using the parallelogram rule, we have:

$$U_{out} = \sqrt{\left|U_{main}\right|^2 + \left|U_{aux}\right|^2 + 2\cdot\left|U_{main}\right|\cdot\left|U_{aux}\right|\cdot\cos(\alpha_2 - \alpha_1)}$$

(1)

$$\alpha = \arg\tan\left(\frac{\left|U_{main}\right|\cdot\sin\alpha_1 + \left|U_{aux}\right|\cdot\sin\alpha_2}{\left|U_{main}\right|\cdot\cos\alpha_1 + \left|U_{aux}\right|\cdot\cos\alpha_2}\right)$$

(2)

where, U_{main}, α_1 are the amplitude and electrical angle of the main voltage vector. U_{aux}, α_2 are the amplitude and electrical angle of the auxiliary voltage vector. U_{out}, α are the amplitude and electrical angle of the synthesized voltage vector.
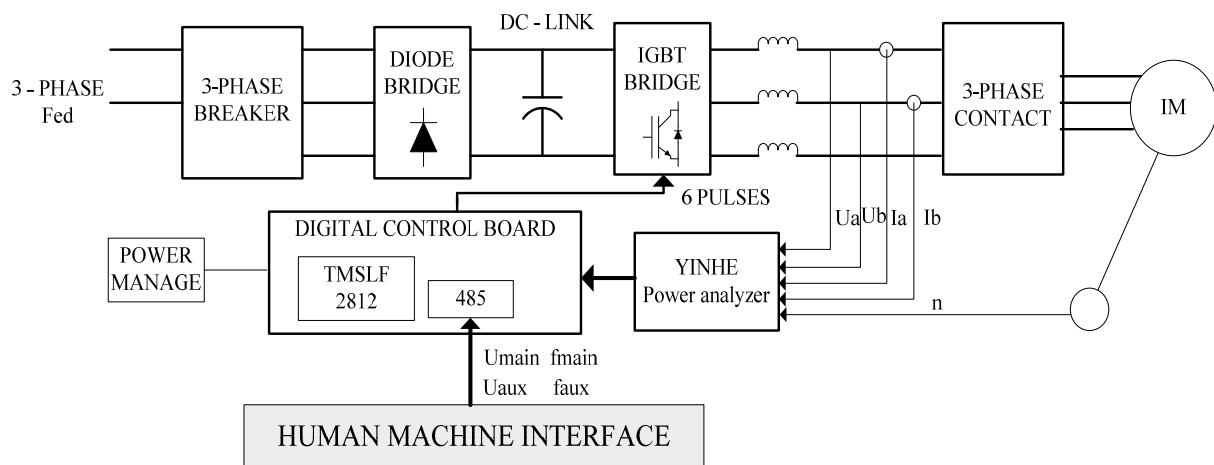

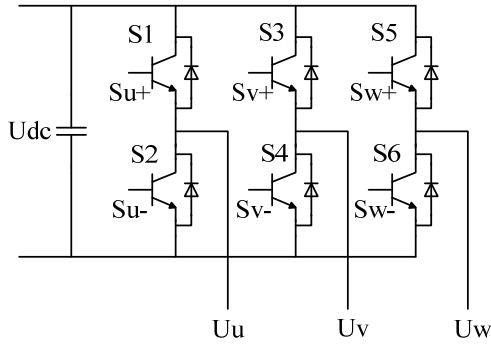**Figure 2. Hardware diagram of digital power for frequency superposition testing**

Figure 3. The diagram of the power converter unit

Table 1. Output phase and line-to-line voltages in terms of DC supply Udc

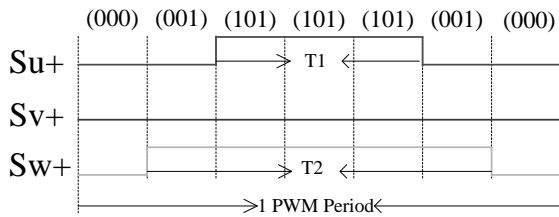| Su+	Sv+	Sw+	Uu	Uv	Uw	Uuv	Uvw	Uwu
0	0	0	0	0	0	0	0	0
0	0	1	-1/3	-1/3	2/3	0	-1	1
0	1	1	-2/3	1/3	1/3	-1	0	1
0	1	0	-1/3	2/3	-1/3	-1	1	0
1	1	0	1/3	1/3	-2/3	0	1	-1
1	0	0	2/3	-1/3	-1/3	1	0	-1
1	0	1	1/3	-2/3	1/3	1	-1	0
1	1	1	0	0	0	0	0	0

Figure 4. One combination of the eight switch patterns

According to (1), (2) we can get the target voltage space vector $\overrightarrow{U_{out}}$ in every carrier period. The sector, the target voltage space vectors and the duration time of the two nearest adjacent voltage vectors can be decided by using SVPWM principle [4−7].

4. Simulation Results

In order to verify the validity of the proposed frequency superposition power, some simulation work has been performed. The parameters of the tested induction motor involved in the simulation are given in Table 2. Figure 7 gives the simulation results of the proposed model.

Before 2s, the motor is only fed with the main power; the voltage of the auxiliary power is set to 0, i.e. the motor runs under No-Load Mode.

At 2s, the auxiliary power is added to the motor, the motor runs under a frequency superposition mode.

5. Experimental Results

Figure 8 shows the DC bus voltage and the stator current obtained with the Tektronix Scope. Such experimental results were obtained with a roller induction motor. The parameters of the tested motor the experiment are given in Table 2.

In this case, the main frequency is given to 21.8Hz, the auxiliary one is 17.8Hz (82% of 21.8). The auxiliary voltage is 0.2 times as the main power which is given to the rated voltage.

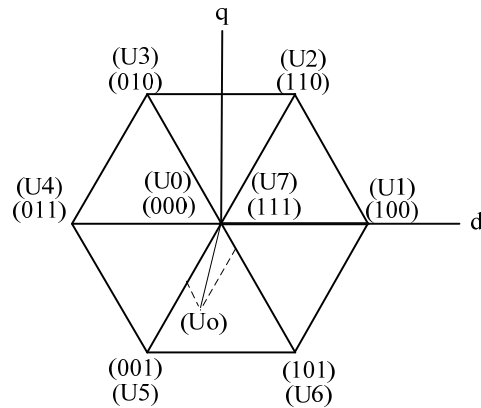This experimental figure shows that the stator current is oscillated at a RMS value equals to the rate current.
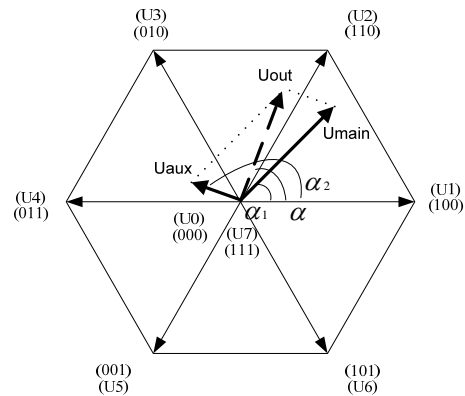

Figure 5. Diagram of the voltage space vector

Figure 6. Synthesis of the dynamic space voltage vectors

Table 2. Rated parameters of the tested induction motor

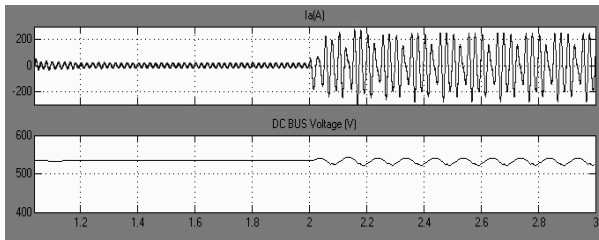| Parameters	Value
Rated voltage (V)	380
Rated current (A)	107
Rated frequency (Hz)	21.8
Rated power (kW)	60

Figure 7. Simulation results of the stator phase A current and the DC bus voltage
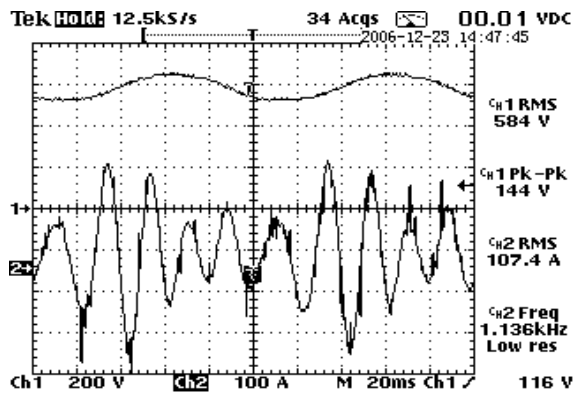

Figure 8. Experimental results of the proposed frequency superposition power supply

6. Conclusions

In this paper, a design of digital motor drive for frequency superposition testing is proposed. It has been implemented in an open loop control by using digital signal processor TMS320LF2812. Simulation results show that the stator current oscillated at a beating frequency after Frequency-Superposition. The tested motor runs as a rated load coupled with it. The experimental results indicate that this power supply can realize the equivalent loading test.

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