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A Review of the Study on the Electromigration and Power Electronics

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Abstract

Electromigration is a main challenge in the pursuit of power electronics, because physical limit to increase current density in power electronics is electromigration (EM), whereas much higher electrical current and voltage are required for power electronics packaging. So the effect of EM is an important issue in applications where high current densities are used, such as in microelectronics and related structures (e.g., Power ICs). Since the structure size of integrated circuits (ICs) decreases and the practical significance of this effect increases, the result is EM failure. On the other hand, in the next generation power electronics technology electrical current density is expected to exceed 10^7 A/cm^2 which is another challenge. This review work has been carried out to identify the mechanism of EM damage in power electronics (e.g., pure metallization and solder joints) and also how to control this kind of damage.

Keywords

Voids and Hillocks, Interconnect, Solder Joint, Thermomigration, MTF, Reliability of IC

1. Introduction

Future technologies demand increasing device densities [1] (e.g., trend towards higher integrations) continuously and line widths continue to shrink [2]. So interconnects are increasingly important in setting not only the device performance, but also the overall device reliability, where EM is a major road block of reliability [3]-[6]. It

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can cause the eventual loss of connections or failure of a circuit [7]. Whereas the reliability of interconnect under high electrical stressing is essential for high power electronics packaging. So it is an important issue for economic and human safety, and survival reasons.

EM is the phenomenon of interconnect metal by self-diffusion along an interconnection as high current density is passing through the interconnect [8] [9] in **Figure 1**, which is nothing but the "transport of material due to the gradual movement of the ions in a conductor by simple momentum transfer between conducting electrons and diffusing metal atoms" [10]. So EM occurs within a metal conductor when large numbers of high-speed current carrying electrons impact on metal lattice and dislodge atoms by simple momentum exchange shown in **Figure 2** [3] [11].

As a result voids will be formed on some parts of the interconnection [14] and hillock due to the accumulation of the metal atoms will be formed on different parts of the interconnection [5]. The presence of voids will increase the resistance [15] [16] of the interconnection or even open, while increased mechanical stress may result in dielectric fractures and leakage between adjacent interconnects in **Figure 3** and **Figure 4**. On the other hand, the presence of hillock will cause short circuit between the adjacent interconnections if the hillock is developed side-way, and short circuit between the different levels of interconnections if it is developed vertically and punch through the inter-metal dielectric. Finally, the function of the integrated circuit is failure. Since repair of a microprocessor chip is impossible and has no alternate way to replace the failed chip [11] [17], this review work has been done to identify the EM failure in power electronics and also how to control this kind of failure.

2. EM Failure Mechanisms

There are three main mechanisms which are responsible for EM failure [12] and these are:

a) The metallurgical-statistical properties of the interconnect;

b) The thermal accelerating process;

c) The healing effects.

(a) The metallurgical-statistical properties of the interconnect

The metallurgical-statistical properties of a conductor film refer to the misorientation of microstructural parameters of the conductor material e.g., grain size distribution. Where grain boundaries and material interfaces lattice structure are not uniform distribution and grain boundaries are inclined with respect to electron flow. Due to

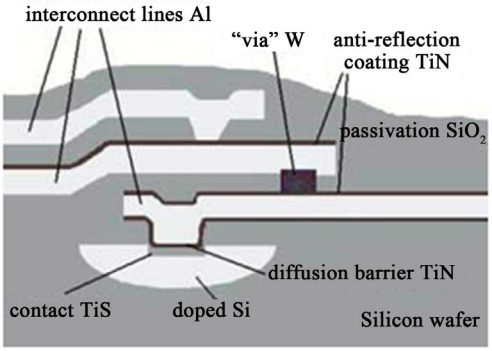


Figure 1. A cross-sectional view of the interconnect structure [12].

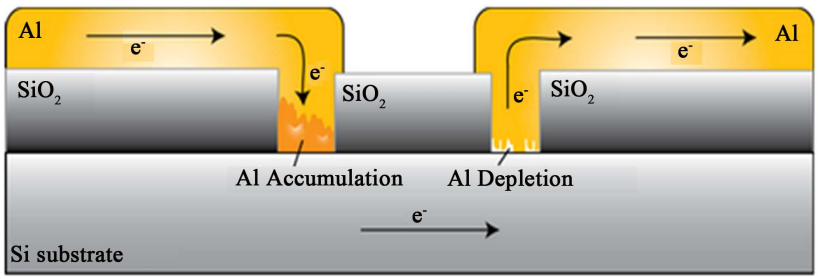


Figure 2. During EM, current flow direction through the sample [13].

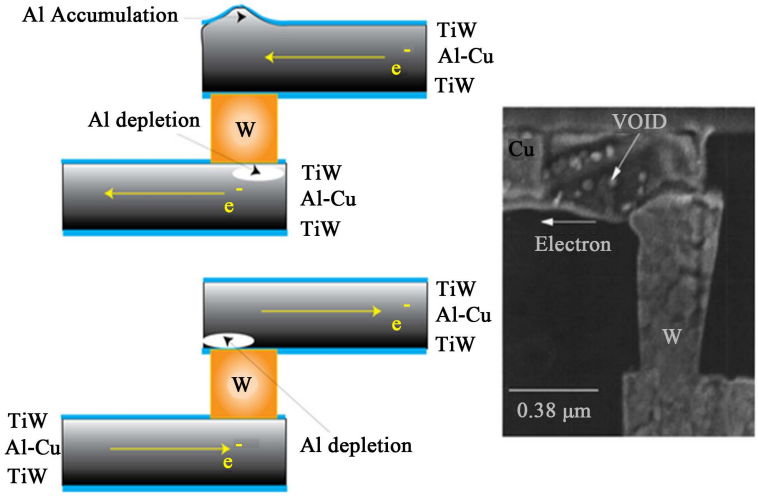


Figure 3. Voids form where the electrons flow away from the via, while a hillock forms when electrons flow towards the via [14].

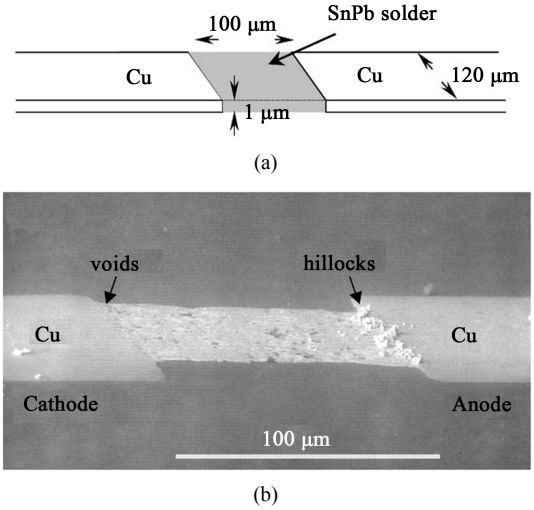


Figure 4. (a) Schematic diagram of the thin stripe sample for EM test; (b) After current stressing voids and hillocks are formed near the cathode and anode side [18].

the random orientation of metallurgical parameters causes a non-uniform distribution of atomic flow rate. Therefore non-zero atomic flux divergence exists where, either a mass depletion (divergence > 0) or accumulation (divergence < 0), which is nothing but the formation of voids and hillocks.

(b) The thermal accelerating process

Acceleration process of EM damage due to the local increase in temperature is refers to the thermal accelerating process. When voids will form in interconnect that increases the current density in the vicinity around itself because it reduces the cross sectional area of the conductor. This increase of the local current density is known as the current crowding. The current crowding effect leads to a local temperature rise around the void due to joule heating [16] that further accelerates the void growth and the whole process continues till the void is large enough to break the line and the process is shown in **Figure 5**.

(c) The healing effects

The cause of atomic flow in the direction opposite to the electron wind force *i.e.*, the back-flow, during or after EM is referred as the healing effects. Due to back flow of mass which begins to take place once a redistribution of mass has begin to form. Because of this back-flow of mass is inhomogenities, such as temperature or concentration gradients, resulting from EM damage.

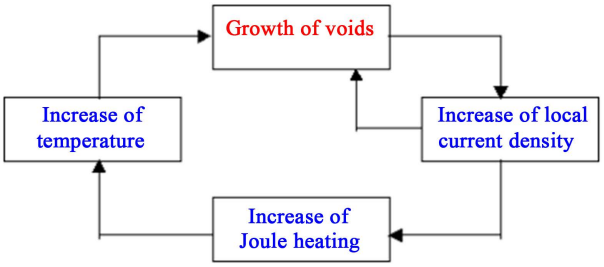


Figure 5. Thermal acceleration loop during EM [19].

2.1. EM in Pure Metal Wire Materials

Aluminium (Al) used in integrated circuits as a most common conductor due to its better properties [20] but it soon appeared that pure Al is susceptible to EM (get rapid formation of hillocks and voids). After adding 2% - 4% of Cu to Al its shows better performance in ICs but problem is grain boundary segregation of Cu, which greatly inhibits the diffusion of Al atoms across grain boundaries. In advanced semiconductor manufacturing processes, Cu has been replaced Al as the interconnect material of choice, because it is less vulnerable as it has higher mass and a higher melting point. Although it's greater fragility in the fabrication process, Cu is preferred for its superior conductivity. Cu is also intrinsically less susceptible to EM. However, EM continues to be an ever present challenge to device fabrication, and therefore the EM research for Cu interconnects is ongoing [12]. On the other hand, the use of Cu plate as substrates, where the electrical connection can be made very simply and they can sustain a fairly large electrical current. It is important in power ICs because we want the EM to be restricted only to the solder bumps as it is well known that the EM of the thin film metal lines in ICs is the major reliability problem since 1970s [16] [21].

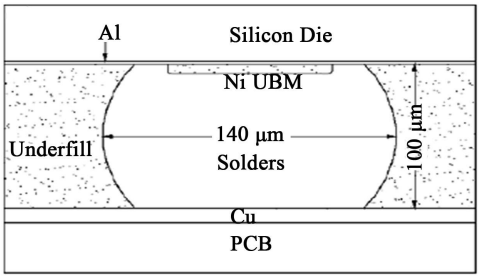
2.2. EM in Solder Joints

EM of interconnect metal lines is the major failure phenomenon in Power ICs [16] [22], but a seldom recognized reliability concern for solder joints. Most of the published literature on EM focused on thin pure metal lines and little on solder interconnects (explained in later section). In Cu or Al interconnects, EM occurs typical current density ranges 10^6 to 10^7 A/cm^2, but for solder joint used in power ICs, however EM occurs at much lower current densities, e.g. 10^4 A/cm^2 because the solder has a low melting point and therefore greater atomic diffusivity at higher operating temperature. So under this high current stressing, a diffusion process occurs to cause drift of metal atoms of bump solder in the direction of the electron flow. The diffusion of solder metal atoms may cause the formation of micro voids near the cathode side and pileup or hillocks near the anode side of solder bump. Due to the current crowding effect, voids form first at the corner of the solder joint. Then the voids extend and decrease the cross-section-area of the solder contact and increase the local current density and local resistance. This expected positive feedback cycle may eventually lead to a so-called EM induced catastrophic failure [23].

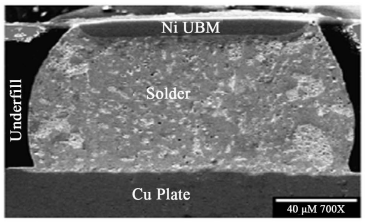
2.2.1. EM Results for SnPb Solder Joint

EM damage is nothing but failure of IC's, the first symptoms is intermittent glitches and is quite challenging to diagnose. When some interconnections fail before others, the circuit exhibits seemingly random errors, which may be indistinguishable from other failure mechanism. Scanning electron microscopy (SEM) is used to identify the image of EM failure.

Eutectic SnPb solder joint was cross-sectioned and polished for direct observation of EM. A schematic cross-section of the solder joint and the SEM secondary image of the cross-section are shown in **Figure 6(a)** and **Figure 6(b)** [23]. Then the solder joint was subjected to current stressing with 1A DC at room temperature, yielding an average current density through the solder joint is 1.3×10^4 A/cm^2 based on the diameter of solder joint. Finally, the solder joint was taken off for SEM analysis. The SEM backscattered images of cross-sectioned surface of solder joint are shown in **Figures 7(a)-(d)**, for initial, 6, 14.5, and 37.5 h of current stressing, respectively [23]. From the SEM backscattered image we can get more information about elemental composition, whereas the secondary image gives more topographic information. SEM secondary images of the solder joint at several magnifications are shown in **Figures 8(a)-(c)** for 37.5 h of stressing. Electron flow direction is from Ni

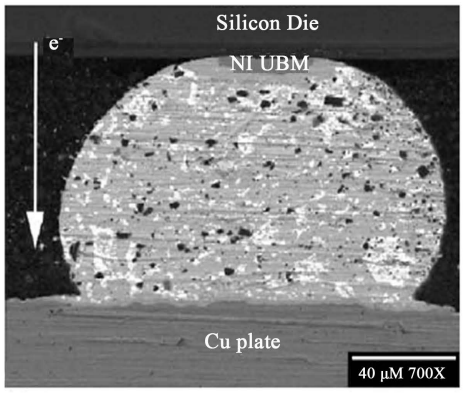


(a)

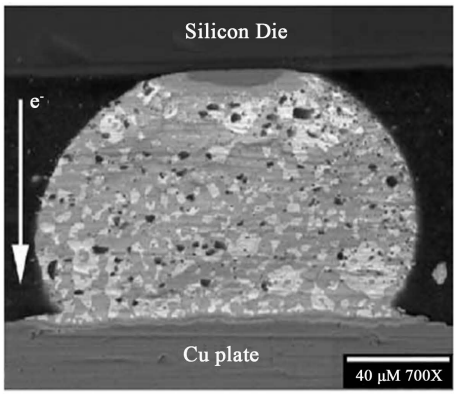


(b)

Figure 6. (a) A schematic cross-section; (b) SEM secondary image of SnPb solder joint [23].



(a)



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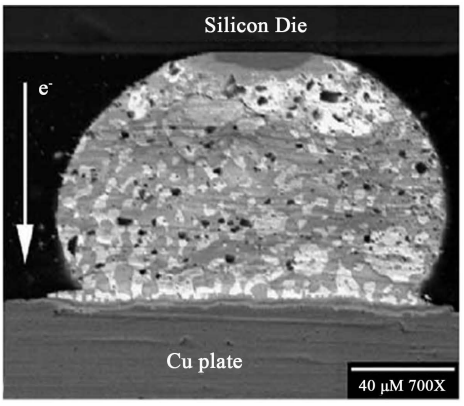
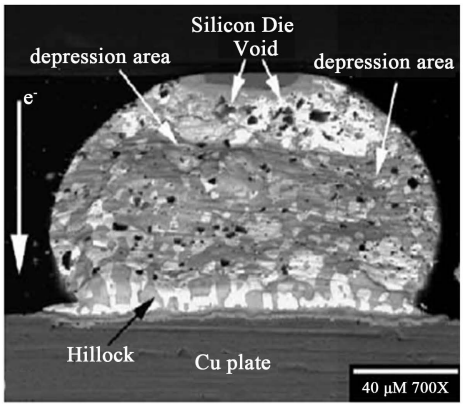


(c)



(d)

Figure 7. SEM back scattered image of solder joint for: (a) initial; (b) 6 h; (c) 14.5 h and (d) 37.5 h [23]. (a) SEM backscattered image of solder joint for initial; (b) SEM backscattered image of solder joint after 6 h; (c) SEM backscattered image of solder joint after 14.5 h; (d) SEM backscattered image of solder joint after 37.5 h.

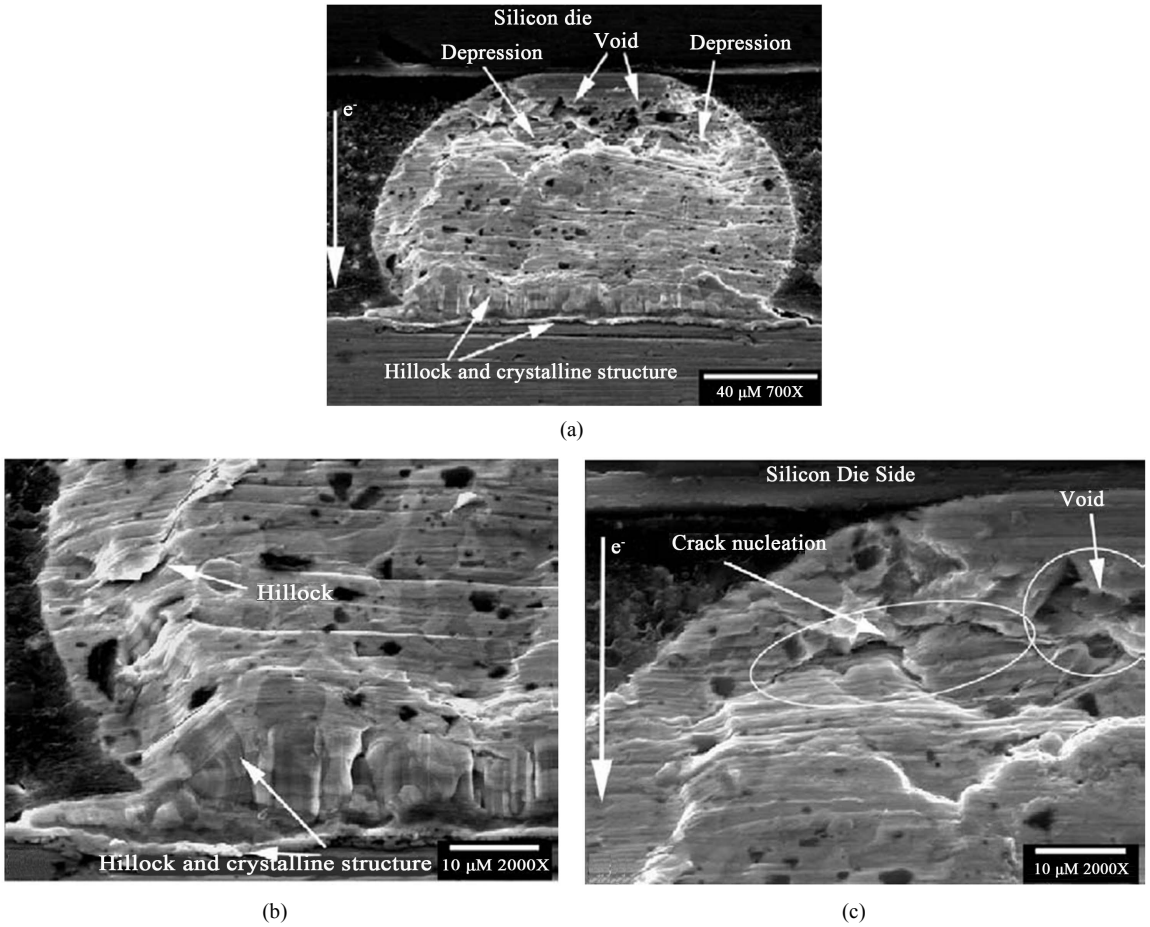


Figure 8. SEM secondary images [23]. (a) after 37.5h, magnification 700×; (b) area on the PCB board side(anode) 2000×; (c) area on the silicon side(cathode) 2000×.

under bump metallization (UBM) on silicon die side to Cu plate on PCB side or top to bottom in the same figure.

The mass accumulation on the anode side and the void formation on the cathode side can be seen in **Figure 7** and **Figure 8**. After 37.5 h stressing, the surface of the cross-sectioned solder joint became very rough due to EM. As a result large depression areas were formed on the cathode side and big voids formed near the Ni UBM side, indicating large amount of mass depletion in the region. Hillocks and crystalline formation were clearly shown in the anode region in **Figure 8(a)**, due to mass accumulation. On the other hand, voids and cracks clearly visible near the cathode region in **Figure 8(c)**. For solder joints it is important to point out that in the real working condition, which is surrounded by epoxy underfill, hillock formation may be impeded. One can expect that much larger compression stress would develop near anode region and tension stress would develop near cathode region compared to the partially exposed cross-sectioned solder joint under test. Where, the development of compressive and tensile stresses will in turn affect the rate of EM as in the case of thin film EM [24].

2.2.2. Analysis of EM through Surface Marker Displacement in Solder Joint

The Cu plate/solder interface was chosen as the fixed frame of reference [23] [25] where some inert particles (e.g., SiC) were left on the sectioned solder surface during polishing, these particles were used as markers in order to measure the atomic flux in the solder joint due to current stressing. In **Figure 9** and **Figure 10** noted the markers position and their movement, where all the markers have moved to the cathode side, which is the opposite direction of the EM flux. Hue Ye *et al.* (2003) have measured the markers movement in the their experiment by measuring the change in marker position with respect to the reference frame on the SEM backscatter images after 6, 14.5 and 37.5 h of current stressing. In **Figure 11**, dashed line shows the average movement of the

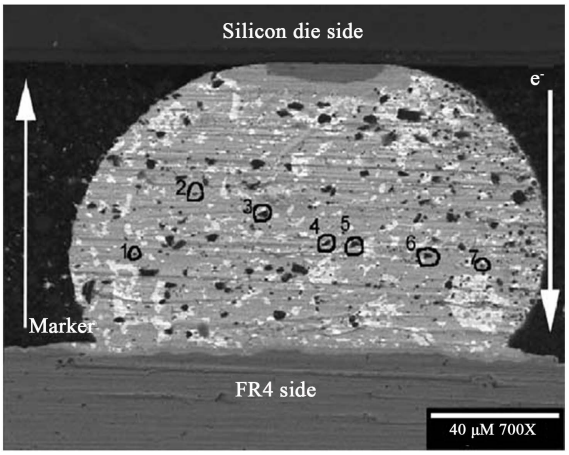


Figure 9. Markers position on the cross-sectioned surface (initial SEM backscatter image) [23].

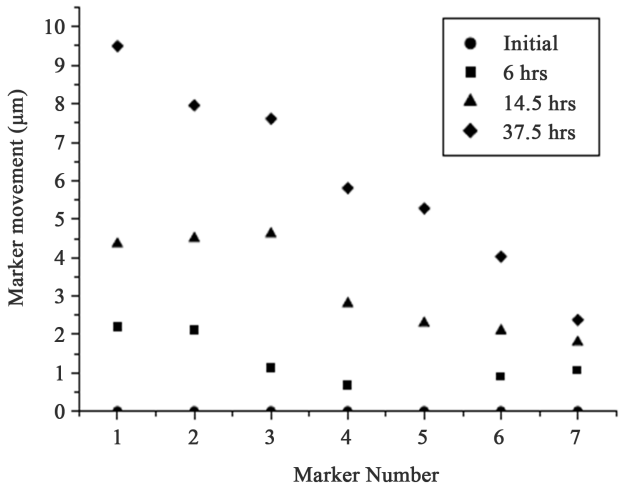


Figure 10. The marker movement on the sectioned eutectic SnPb surface [23].

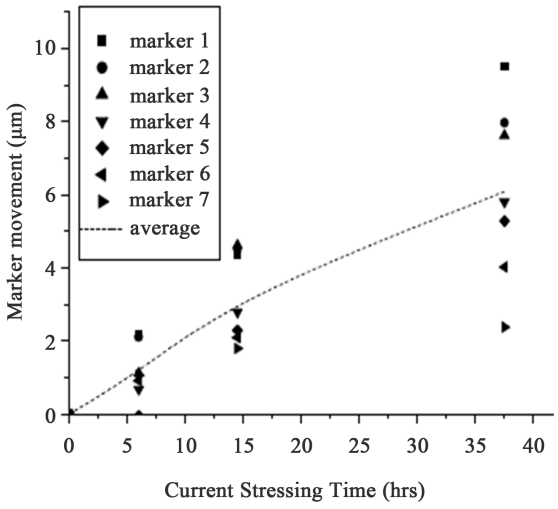


Figure 11. The marker movement vs. current stressing time [23].

markers linear dependence on current stressing time. Hue Ye *et al.* (2003) also calculated in their experiment volume of solder movement by EM (V_{EM}) 4.51×10^{-8} cm^3 after 37.5 h of current stressing. The cross-sectional area of solder joint at the initial marker position is 7.697×10^{-5} cm^2.

The average marker movement is 6.078 μm. Finally, they computed the values $D \times Z^*$ in their experiment and compared with the previous published result shown in **Table 1**. The basic difference is that they have performed their experiment at room temperature whereas the previous all experiment was performed at elevated temperature (120˚C). Since the diffusivity (D) of solder at room temperature is known, so the effective charge number Z^* can be easily extracted [23].

2.2.3. Thermomigration

Thermomigration have investigated in flip chip solder bump system, which is nothing but as a movement of metal atoms from hot side to cold side between chip and substrate due to Joule heating induced thermal gradient. H. V. Nguyena *et al.* [26] has developed a physical model in which the important parameters were C_v, T, j and σ are treated under perturbed state in the presence of a temperature gradient and to analyze the effect of temperature gradient on the EM induced failure. In the meantime Ru *et al*. and H.V. Nguyen *et al.* already proved in different experiment that temperature gradient plays a significant role in the EM-induced failure. EM process is enhanced by temperature gradient. The failures will occur mainly near the local heating elements at the site of maximum temperature gradient [26].

D. Yang *et al.* (2006) [27] found in their experiment for eutectic SnPb flip chip solder joints, no significant thermomigration occurred after 100 h at 20˚C and at 100˚C. Only microstructural coarsening was observed in solder joints **Figure 14**. But at higher temperature 150˚C after 50 h they observed that Pb thermomigration and phase segregation. **Figure 12** shows a typical bonded sample prepared for testing. A typical sketch of flip chip solder joints shown in **Figure 13** has been used for this study where two pairs of solder joints (joint 5, 6, 7 and 8) were powered with a current of 1.8 A at different ambient temperatures.

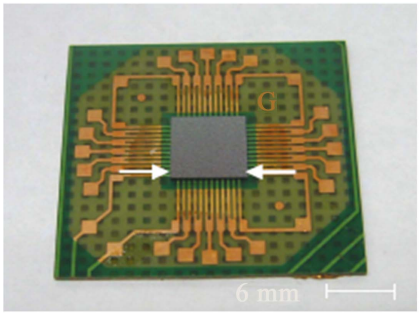


Figure 12. A Flip chip sample (The arrowed region shows the area which is given as an expanded sketch [27].

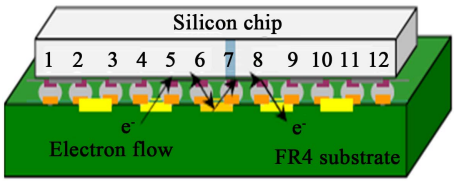


Figure 13. Sketch of solder joints with four solder joints (joint 5 to 8) under current stressing [27].

Table 1. Comparison of $D \times Z^*$.

	Lee *et al.* (2001)	Lee and Tu (2001)	Hue Ye *et al.* (2003)
Temperature (˚C)	120˚C	120˚C	Room Temperature
Current density A/cm^2	2×10^4	3.8×10^4	1.3×10^4
Time (h)	324	39.5	37.5
$D \times Z^*$	2.16×10^{-11}	1.85×10^{-10}	3.62×10^{-10}

2.2.4. Grain Coarsening and Pb-Phase Region Growth

If the average phase size exceeds a pre-set critical size then the PbSn eutectic solder joint is assumed to be a failed joint due to electrical current induced coarsening. In PbSn eutectic solder joints coarsening is very often used as degradation metric. Due to thermal cycling or strain, grain coarsening and phase growth of eutectic solder alloys has been extensively reported in the literature. As EM is a diffusion process which is driven by a high-density direct current or electron wind, so phase growth is expected. Finally, mass accumulation near the anode side, void formation near the cathode side and coarsening of a Pb-phase region usually observed during experimentation [23]. D. Yang *et al.* (2006) [27] also explained coarsening in their literature. **Figure 14(a)** and **Figure 14(b)** are shown the original microstructure of solder joints before the experiments.

In the fine scale, bright region corresponds to the Pb rich region and dark region corresponds to the Sn rich region because of their difference in element numbers in the periodic table. When a current 1.8 A was applied of this solder joint at 20˚C and 100˚C after 100 h the phase coarsening were observed shown in **Figure 14(c)** and **Figure 14(d)** [11]. H. Ye *et al.* (2003) [23] also found in their experiment the average area and diameter of Pb rich regions were increasing according to current stressing time. The "average diameter" is calculated from the average length of several lines drawn through the centroid of the phase region and only the "average area" is an ASTM standard. The average Pb phase size and average Pb phase diameter of Pb regions vs. stressing time are shown in **Figure 15**.

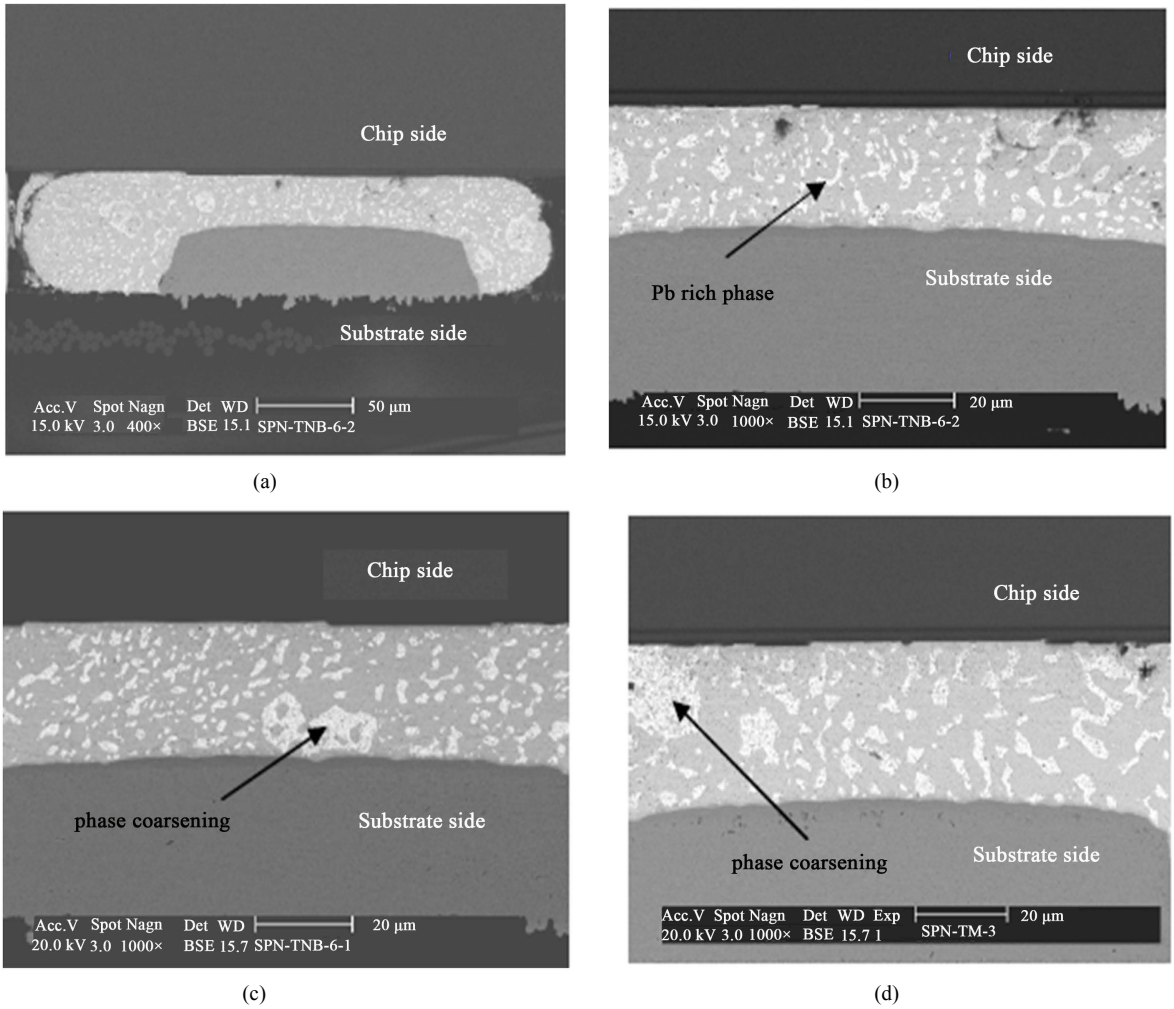
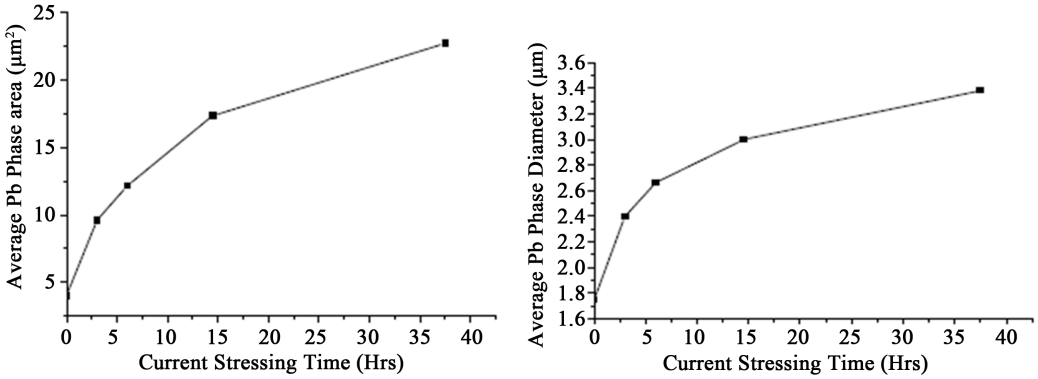


Figure 14. (a) SEM micrograph of original micro structure of solder joints (as-reflowed); (b) Local magnified micrograph; (c) SEM micrograph of phase coarsening in an unpowered solder joint after 100 h at 20˚C; (d) SEM micrograph of phase coarsening in an unpowered solder joint after 100 h at 100˚C [27].



(a) (b)

Figure15. Pb phase: (a) average area vs. stressing time; (b) average diameter vs. stressing time [23].

3. Mean Time to Failure (MTF) of Interconnection in IC

Due to difficulty of testing under real conditions of IC, at the end of the 1960s J. R. Black developed an empirical equation to estimate the MTF of a metal wire interconnection, taking EM into consideration and this equation has been widely used till now to predict the life time of ICs [15] [26] [28].

$$\mathrm{MTF} = A\left(J - J_{\mathrm{crit}}\right)^{-n} \exp\left(E_a / KT\right)$$

where, A = Constant based on the cross-sectional area of the interconnection;

J = Current density; J_{crit} = Critical (threshold) current density necessary to produce failure;

E_a = Thermal activation energy (e.g. 0.7 eV for grain boundary diffusion in Al [29]);

K = Boltzmann's Constant; T = Line temperature;

n = Scaling factor (usually set to 2 according to Black [30]).

So, it is clear from the above equation, current density (J) and the temperature (T) are the affecting parameters at the MTF of the interconnection. During rising temperatures for an interconnection to remain reliable, the maximum tolerable current density of the conductor must necessarily decrease. Usually, both the average J and average T are increasing as the semiconductor technology advances. Consequently, more precise EDA (Electronic design automation**)** tools that are able to account for the thermal effects are required to design in reliability which is nothing but to accurately simulate the current density and temperature of interconnects in order to prevent EM induce failures.

4. Importance of EM

EM is the dominate failure mechanism in Power ICs and decreases the reliability of chips integrated circuits (ICs). So Interconnect reliability is the main factor that determines the circuit reliability especially when the line width becomes much narrower which renders high current density [31]. It also noted that the failure rate of a scaled 65 nm processor is more than three times higher than a similarly pipelined 180 nm processor, where EM and time-dependent dielectric breakdown showing the most dominant mechanisms according to the advancement in the technology nodes.

So increasing the failure rate is believed due to an interconnection with narrower line width and the increasing sensitivity of the circuits to interconnect line resistances as the circuits are operating at higher frequency. For illustration purpose they used a simple CMOS voltage inverter circuit as shown in **Figure 16**. They found in their experiment resistance in the interconnection increases with time due to EM. When the interconnect resistance is higher the circuit performances is very bad. e.g., longer signal delay and higher power consumption and such impact of interconnect resistance to IC performance is greater as the operating frequency of the integrated circuits became higher. From the simulation setup they showed that when the circuit operating frequency increases (e.g. from 100 MHz to 1 GHz), the resulting temperature of the circuit also increases. C. M. Tan *et al.* [31] showed in their experiment the EM degradation rate increases when the circuit temperature is increases. e.g., shorten the life time and degrade the reliability of an integrated circuit.

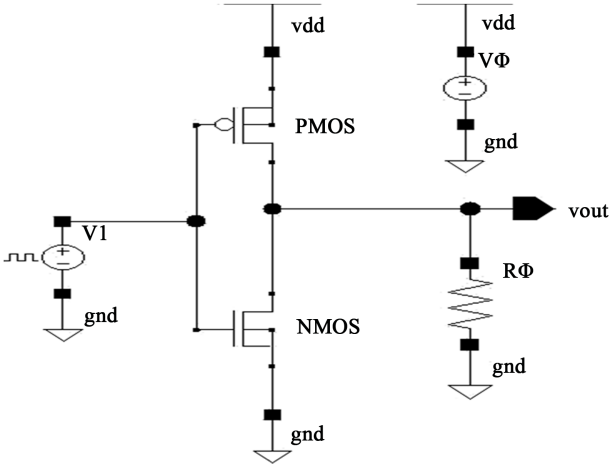


Figure 16. Schematic of a simple inverter circuit to illustrate the increasing sensitivity of circuit performance to inter connect [19].

5. Improvement of Interconnect Reliability

From the EM studies it is noted that the interconnect reliability in ICs is most important issues as technology node advances in order to ensure its reliability. Recent work [32] showed that chip failures because of power grid issues, where EM already being discovered by chip designers. Analysis of power grid is becoming a required addition to many design flows. The interconnect system is facing a number of different challenges ahead. Novel interconnect systems such as 3D interconnect are proposed and experimented, new interconnect materials are also being explored but the reliability of these new proposals remains unknown. C. Goossens *et al*. and J. Guo [23] [32] mentioned in their work additional efforts at the design stage are essential to obtain robust and reliable chips. In order to provide adequate knowledge on the interconnect EM for both the IC manufacturers and designers, the testing methodologies of interconnect reliability and the modeling of EM is necessary. The modeling of EM is particularly important because it helps to identify the critical weak spots of an interconnection system in a short time. A typical IC layout has millions of interconnection. Analyzing the reliability problems on each of them is prohibitively time consuming. So using EM modeling the key interconnects easily can be investigated. Also, modeling of EM can be integrated into EDA tool, where a complete EM aware IC design can be realized. Using the advancement in numerical tools, key factors that affect the EM performances of an interconnect system can be identified. Which is more significant for ULSI development so that a reliable interconnect system can be built as ULSI technology is advancing and the demand for ULSI in term of speed and functionality are ever increasing [14] [29]. Another recent work [15], where EM reliability of the contact hole in SiC power devices was evaluated for an improved Al electrode sandwiched between thin TaN layers. They showed that Al electrode demonstrated long-term reliability even at higher junction temperatures. They found MTF of approximately 3400 years under conditions of Tj = 300˚C and $J = 10^4$ A/cm^2. On the other hand, many ICs have an intended MTF is at least 10 years [17]. But in modern power electronic devices, power ICs are rarely fail due to EM effects, because most of the IC design houses use automated EDA tools to check and correct EM problems at the transistor layout-level. When devices are operated within the manufacturer's specified temperature and voltage range, a properly designed IC device is more likely to fail from other causes may be environmental or such as cumulative damage from gamma-ray bombardment.

6. Conclusion

Reliability is the key issue for the next generation power electronics under high electrical current stressing. Some recent published literature concerning reliability proposed a good dynamic reliability model, which was capable to return reliability equivalent temperatures and currents, for EM under non-uniform temperature distributions, easily obtained close bounding temperatures to estimate the actual lifetime. On the other hand, Black's equation is still applicable by using constant reliability equivalent temperatures. So blindly using the maximum or average temperature is not appropriate to evaluate EM lifetime. Some proposed model also enables the de-

signers to more aggressively explore the design space and to reclaim the design margin imposed by less accurate, more pessimistic models. This analysis shows that temperature-aware designers are to evaluate the system reliability using runtime information, which increases the confidence about the actual behavior of the system. Generally, when the operating temperature increases, lifetime is being consumed more rapidly and vice versa. But if the operating temperature is below a nominal temperature (*i.e.*, the threshold temperature used in DTM techniques), lifetime can be easily consumed at a slower rather than nominal rate. This is nothing but banking lifetime for future consumption. As a result, much better performance gains would be expected because more lifetimes can be banked.

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