Scientific Research Publishing

Journal of Computer and Communications, 2016, 4, 151-159
http://www.scirp.org/journal/jcc
ISSN Online: 2327-5227
ISSN Print: 2327-5219

Design of Polymorphic Operators for Efficient Synthesis of Multifunctional Circuits

Radek Tesař, Václav Šimek, Richard Růžička, Adam Crha

Faculty of Information Technology, Brno University of Technology, Brno, Czech Republic
Email: itesar@fit.vutbr.cz

How to cite this paper: Tesař, R., Šimek, V., Růžička, R. and Crha, A. (2016) Design of Polymorphic Operators for Efficient Synthesis of Multifunctional Circuits. *Journal of Computer and Communications*, **4**, 151-159.
http://dx.doi.org/10.4236/jcc.2016.415015

Received: November 8, 2016
Accepted: November 26, 2016
Published: November 29, 2016

Abstract

Systematic effort dedicated to the exploration of feasible ways how to permanently come up with even more space-efficient implementation of digital circuits based on conventional CMOS technology node may soon reach the ultimate point, which is mostly given by the constraints associated with physical scaling of fundamental electronic components. One of the possible ways of how to mitigate this problem can be recognized in deployment of multifunctional circuit elements. In addition, the polymorphic electronics paradigm, with its considerable independence on a particular technology, opens a way how to fulfil this objective through the adoption of emerging semiconductor materials and advanced synthesis methods. In this paper, main attention is focused on the introduction of polymorphic operators (*i.e.* digital logic gates) that would allow to further increase the efficiency of multifunctional circuit synthesis techniques. Key aspect depicting the novelty of the proposed approach is primarily based on the intrinsic exploitation of components with ambipolar conduction property. Finally, relevant models of the polymorphic operators are presented in conjunction with the experimental results.

Keywords

Digital Circuits, Reconfiguration, Multifunctional Logic, Ambipolarity, Polymorphic Electronics, Synthesis Methods

1. Introduction

Seemingly endless trend of downscaling CMOS technology features in almost linear manner according to the Moore's law [1], as it was a rather common practice during several previous decades, has enabled the semiconductor industry to fit an ever-increasing number of devices per unit area and also achieve higher performance expressed as unit of energy (watt) spent in performing computational tasks. Various

research directions have been mostly addressing possible ways how to achieve even a greater scaling of the technology features in order to push the actual integration level further beyond the existing boundaries. Nevertheless, the existence of physical limits to this growth is generally recognized today: the electronics-based technologies cannot be scaled down beyond certain dimensions that are inherently defined by some physical constraints [2]. Nowadays, it is possible to identify a lot of diverse application areas where a digital circuit with the inherent ability to perform a set of different functions at particular moments in time may prove to be a very efficient means of solution. Obviously the most immediate approach, how to address this specific need, is to design as many different circuits as the overall number of functions that are actually needed in a given situation. As a next step involved within the execution flow, individual outputs of these circuits are switched in such a way that only the presently required function will be taken into account. However, the main drawback behind this conception, and its essential limitation as well, will emerge in direct connection with the overall size of the resulting implementation on the circuit level that needs to be placed into a target area of a restricted dimensions.

Recent advancements within the field of digital design techniques and components for digital circuits provide a vital evidence that yet another feasible strategy may be employed—area and time-efficient circuit design based on utilization of individual structural elements exhibiting multifunctional nature [3]. In this case, the entity of multifunctional circuit is devised as a compact structure involving set of multifunctional components, where their mutual, low-level interconnection scheme remains untouched in all allowable operating modes and only the active function of these components is expected to change intentionally.

A special case related to these multifunctional circuits is based on adoption of polymorphic electronics approach [4]. Such circuits typically change their function in accordance to the actual state of a target operating environment, which is represented by a physical quantity with notable influence on some of the physical parameters of electronic structures–power supply voltage level, voltage amplitude of a signal, temperature, etc. In addition, no configuration network with a global scope or dedicated input pins of these components are required [5]. It's important to point out that change of the active function, which is executed by the polymorphic circuit, takes place immediately.

Today's applications are generally based on exploitation of unipolar semiconductor transistors. However, the concept of polymorphic electronics has more profound nature and allows to conveniently employ new emerging devices with ambipolar behaviour. In fact, relevant aspects of the emerging materials and technologies can be approached from various standpoints through the formulation of several abstraction levels [6]. Without the ambition to provide their complete and exhaustive list, the most interesting candidates for a replacement of unipolar CMOS technology in the suggested scenario may include silicon nanowires (Si-NWs) [7] [8], carbon nanotubes [9] [10], graphene nanoribbons [11] [12], organic polymers with semiconductor-like properties

[13] and presumably even other suitable emerging nanostructures and materials [14], which make it possible to obtain new generation of advanced multi-functional logic elements.

The structure of this paper is organized as follows: the opening section explains basic aspects of multifunctional circuits. Section II is briefly explaining key aspects behind polymorphic electronics and the benefits to be obtained when using ambipolar components. Brief review of selected polymorphic circuit synthesis methods can be found in section III. Then, ambipolar transistor model is shown in section IV together with specification of basic components. Finally, section V provides the conclusion.

2. Polymorphic Electronics

The notion of polymorphic electronics [4] determines, in its own essence, a standalone category of reconfigurable circuits, which represents a highly appealing prospect how to implement all the required functional properties in a resource-efficient way. In the case of these circuits assuming the principles of polymorphic electronics, various modifications in the key physical characteristics of building components (e.g. in a transistor's operation point, usage of ambipolar charge carrier conductivity) are predominantly involved behind the change of their behaviour as a straight response to the influence of external stimuli–temperature, power supply voltage, light intensity, special signal, etc. However, the structure of the circuit itself remains unchanged on the interconnection level for all the intended functions.

2.1. Survey of Existing Polymorphic Gates

It is pertinent that the availability of suitable building components can be identified as one of the key prerequisites enabling the practical deployment of polymorphic circuits. As it is demonstrated in **Table 1**, there already exist a number of polymorphic gates

Table 1. Overview of existing polymorphic gates.

Gate	*Value*	*Cntrl.*	*Size*	*Ref.*
Nand/Nor	3.3/1.8V	V_{dd}	6	[16]
And/Or	1.2/3.3V	V_{dd}	8	[17]
Nand/Nor	5/3.3V	V_{dd}	8	[18]
And/Or	27/125˚C	temp.	6	[4]
And/Or	5/90˚C	temp.	8	[4]
Nand/Nor	0/5 V	ext. voltage	10	[20]
Nand/Nor	5/0 V	ext. voltage	8	[21]
Nand/Nor	5/0 V	ext. voltage	10	[21]
Nand/xOr	5/0 V	ext. voltage	9	[21]
And/Or	0/3.3 V	ext. voltage	6	[4]
And/Or/xOr	3.3/1.5/0 V	ext. voltage	9	[4]
Nand/Nor	0/5 V	ext. voltage	10	[19]

which are implementing various functions. These gates were mostly constructed by means of using certain variation of conventional CMOS fabrication process. Main drawback in this case can be attributed precisely to the fact that it is necessary to use transistors with different channel width and length dimensions in order to achieve the polymorphic behaviour. This observation also explains the reason why individual transistors in such circuitry may also operate in linear mode instead of adhering to the switching mode only. As a consequence steady current flow through such gates leads to significant rise in power consumption.

2.2. Benefits of Amnipolarity

Therefore unconventional approach to the construction of polymorphic gates using technologies such as transistors with ambipolar characteristics [15] is highly desirable. Such gates contains less transistors and also operate exclusively in switching mode. An example of ambipolar polymorphic gate is given on **Figure 1**. This gate exhibits NOR function when M1 and M2 are in N-mode and M3 and M4 are in P-mode. When all transistors change the polarity, NAND function is exhibited by the gate. The polarity of transistors, and by this the function of the gate, is controlled by power–polarity of voltages V0 & V1.

2.3. Synthesis of Polymorphic Circuits

Nowadays, design of polymorphic circuits is performed almost exclusively at a gate level. Results of practical experiments in this domain indicate that meaningful polymorphic circuits always include a combination of several polymorphic gates alongside the selection of ordinary gates. In most situations only one type of polymorphic gate (e.g. NAND/NOR) is employed in the whole design procedure [22]. The overall design efficiency (in terms of circuit size or speed) could be further improved if a more diverse selection of polymorphic gates (other types besides NAND/NOR variant as well) is taken into account. However, it would be definitely paid by a more complicated synthesis process due to the state space growth. Let's also note that none of the existing synthesis methods takes into account yet the polymorphic gates based on ambipolar behaviour.

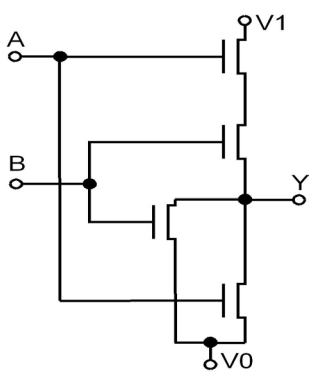

Figure 1. Polymorphic NAND/NOR gate using ambipolar transistors.

2.4. Evolutionary Approach

Digital circuit synthesis and optimization techniques based on thoughtful exploitation of convenient evolutionary-inspired paradigms, as demonstrated by Sekanina [23] (and before initially suggested e.g. by Miller [24]), could establish a way how to achieve a rather unconventional but, at the same time, interesting and useful solution. Needless to say, also the original concept of polymorphic electronics emerged virtually as a side effect of evolutionary design experiments [4]. Almost all polymorphic circuits, more complex than just a few gates, have been designed using Carthesian Genetic Programming (CGP) [24] till now.

2.5. Conventional Methods

The first method from this cathegory involves the so-called polymorphic multiplexing [22]. For each function, a digital circuit is synthesized and the outputs of these circuits are then multiplexed by a polymorphic multiplexor. The structure of a circuit designed by this method shows a relatively low optimality. However, possible workaround towards the desirable improvement dwells in the partial sharing of some logic resources between individual functions.

In addition to the already introduced method, Gajda [22] proposed a method of polymorphic circuit synthesis utilizing binary decision diagrams (BDD). The method is called PolyBDD. Its core is based on Multi-terminal BDD (MTBDD), which is an extension of binary decision diagrams. MTBDD representation, which is created for desired functions F1 and F2, is further converted into a circuit, where the nodes assume the role of multiplexers and the terminals are replaced by a proper polymorphic subcircuit according to the previously assigned integer number.

3. Ambipolar Transistor Model and Components

This section is dealing with a definition of fundamental model for ambipolar transistors, which are important means for describing operation of polymorphic gates. **Figure 2** shows an example of ambipolar transistor model created by means of utilizing conventional silicon MOSFET transistors. For the construction of such a model, transistors with terminated substrate would be preferable. Unfortunately, such transistors are rare, so the model was created from the standard P-type and N-type transistors.

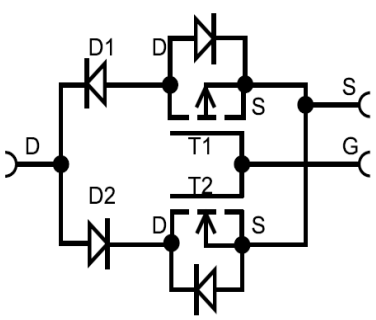

Figure 2. Basic model of an ambipolar transistor.

Each instance of the unipolar MOSFET transistor has an integrated body diode where its unwanted influence must be eliminated by anti-serial connection of diodes D1 and D2.

The function of this model is explained in details within **Table 2**. Its columns D, S, G denotes the individual terminals of the transistor model; their values are + or -, which corresponds to the supply voltage polarity (Vcc, GND). Then, columns D1, D2 simply denote anti-serial diodes from transistor model and have values of F (forward direction) or R (reverse direction). Columns T1 and T2 are related to transistors from the same model. If a value is ON, the transistor is closed (current flows through the transistor), while OFF signature denotes that transistor is open (and therefore current cannot flow across this element). The last column depicts the behavior of the model where HiZ represents the high impedance state (model is "tri-stated"). "Close" option simply means that the model is closed and the conductive pat his available for current.

Ambipolar Inverter and Negation/Identity Gate

The simplest gate formed from an ambipolar transistors is an inverter. Unlike to conventional CMOS-based one, when the ambipolar transistors are used, both are of the same type. It means that the transistors will autonomously select their operating mode with respect to their deployment inside a given circuit. This makes the ambipolar inverter resistant to power supply polarity change—if the Vcc and GND are swapped, the type of transistors will change.

Figure 3 above shows the configuration of polymorphic inverter model, which is using simulated ambipolar transistors. Input of the inverter is connected to GND (logic L level). The output is expected to reach the level of Vcc. Results obtained from measurement are depicted on **Figure 4**. Situation, when the input signal is assigned to H level (close to Vcc) is very similar. The only difference is that output of the inverter is constantly staying at L level. Finally, negation/identity gate is shown on **Figure 5**.

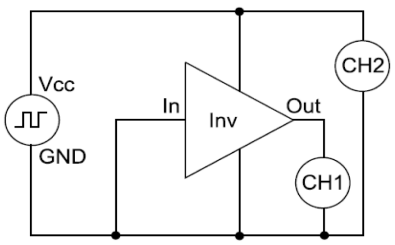

Figure 3. Evaluation setup of ambipolar polymorphic inverter-input connected to GND (logil level L close to amplitude of 0 V).

Table 2. Operating states of an ambipolar transistor model.

D	*S*	*G*	*D1*	*D2*	*T1*	*T2*	*D-S*
+	−	v	R	F	OFF	OFF	HiZ
−	+	−	F	R	OFF	ON	Close
+	−	+	R	F	ON	OFF	Close
−	+	+	F	R	OFF	OFF	HiZ

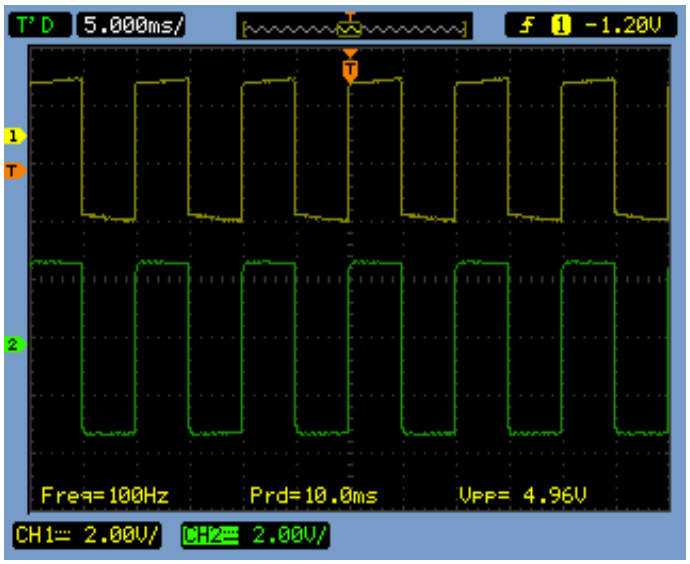

Figure 4. Measured characteristics of ambipolar inverter, input attached to L.

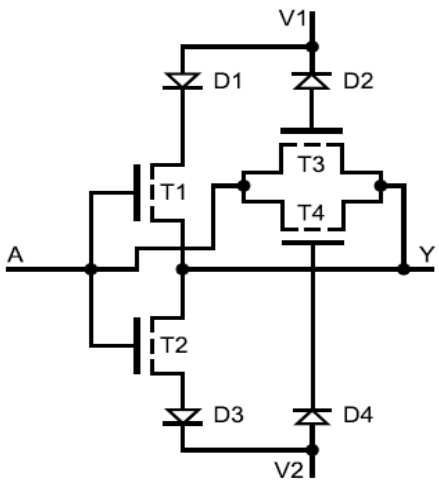

Figure 5. Ambipolar polymorphic gate with the function of negation/idnetity.

4. Conclusion

It is fortunate that we have at hand a property called ambipolarity. This important property allows to design efficient implementation of various polymorphic gates in comparison with conventional approach. Further steps will include the adoption of a platform with configurable matrix of Si-NW transistors [15] for truly ambipolar solution.

Acknowledgements

This work was generously supported by the internal grant Architecture of parallel and embedded computer systems (no. FIT-S-14-2297) and by national COST grant Unconventional Design Techniques for Intrinsic Reconfiguration of Digital Circuits: From Materials to Implementation (no. LD14055).

References

[1] Moore, G.E. (1998) Cramming More Components Onto Integrated Circuits. *Proc. of the IEEE*, **86**, 82-85.

[2] Cerofolini, G.F. (2006) Realistic Limits to Computation. II. The Technological Side. *Applied Physics A*: *Materials Science and Processing*, **86**, 31-42.

[3] Růžička, R. and Šimek, V. (2013) More Complex Polymorphic Circuits: A Way to Implementation of Smart Dependable Systems. *ElectroScope*, **7**, 1-6.

[4] Stoica, A., Zebulum, R.S. and Keymeulen, D. (2001) Polymorphic Electronics. *Proceedings of Evolvable Systems—From Biology to Hardware Conference*, **2001**, No. 2210, 291-302.

[5] Sekanina, L., Růžička, R., Vašíček, Z., Prokop, R. and Fujcik, L. (2009) REPOMO32—New Reconfigurable Polymorphic Integrated Circuit for Adaptive Hardware. In: *Proc. of the* 2009 *IEEE Symposium Series on Computational Intelligence— Workshop on Evolvable and Adaptive Hardware*, IEEE Computational Intelligence Society, Nashville, 36-46.

[6] ITRS (2014) More than Moore White Paper [online]. c2014, Version 2.3 [cit. 2016-06-05]. http://www.itrs2.net/uploads/4/9/7/7/49775221/irc-itrs-mtm-v2_3.pdf

[7] Palacios, T. (2012) Applied Physics: Nanowire Electronics Comes of Age. *Nature*, **481**, 152-153.

[8] Thelander, C., Agarwal, P., Brongersma, S., *et al.* (2006) Nanowire-Based Onedimensional Electronics. *Materials Today*, **9**, 28-35.

[9] Collins, P.G., Arnold, M.S. and Avouris, P. (2000) Nanotubes for Electronics. *Scientific American*, **283**, 62-69.

[10] Chae, S.H. and Lee, Y.H. (2014) Carbon Nanotubes and Graphene Towards Soft Electronics. *Nano Convergence*, **1**, 1-26.

[11] Yazyev, O.V. (2013) A Guide to the Design of Electronic Properties of Graphene Nanoribbons. *Accounts of Chemical Research*, **46**, 2319-2328.

[12] Chang, S.L., *et al.* (2014) Geometric and Electronic Properties of Edge-Decorated Graphene Nanoribbons. *Scientific Reports*, **4**, 1-8.

[13] Chen, Z., Lee, M.J., Ashraf, R.S., Gu, Y., Seinfried, S.A., Nielsen, M.M., *et al.* (2012) High-Performance Ambipolar Diketopyrrolopyrrole-Thieno[3,2-b]thiophene Copolymer Field-Effect Transistors with Balanced Hole and Electron Mobilities. *Advance Materials*, **24**, 647-652. https://doi.org/10.1002/adma.201102786

[14] Bernstein, K., *et al.* (2010) Device and Architecture Outlook for Beyond CMOS Switches. *Proc. of the IEEE*, **98**, 2169-2184.

[15] Heinzig, A., Trommer, J., Grimm, D., Mikolajick, T. and Weber, W. (2013) Dually Active Silicon Nanowire Transistors and Circuits with Equal Electron and Hole Transport. *Nano Letters*, **13**, 4176-4181.

[16] Stoica, A., Zebulum, R. S., Guo, X., Keymeulen, D., Ferguson, I. and Duong, V. (2004) Taking Evolutionary Circuit Design from Experimentation to Implementation: Some Useful Techniques and a Silicon Demonstration. *IEE Proc.-Comp. Digit. Tech.*, **151**, 295-300.

[17] Stoica, A., Zebulum, R.S., Keymeulen, D. and Lohn, J. (2002) On Polymorphic Circuits and their Design using Evolutionary Algorithms. In: *Proc. of IASTED International Conference on Applied Informatics* (AI2002), Acta Press, Insbruck, 1-6.

[18] Růžička, R., Sekanina, L. and Prokop, R. (2008) Physical Demonstration of Polymorphic Self-checking Circuits. In: *Proc. of the* 14*th IEEE Int. On-Line Testing Symposium*, IEEE Computer Society, Los Alamitos, 31-36.

[19] Žaloudek, L. and Sekanina, L. (2008) Transistor-Level Evolution of Digital Circuits Using a Special Circuit Simulator. *Proc. of Evolvable Systems*: *From Biology to Hardware*, Springer, Berlin, 320-331.

[20] McDermott, M.W. and Turner, J.E. (1997) Configurable NAND/NOR Element. US Pat. 5592107, January 1997.

[21] Růžička, R. (2008) On Bifunctional Polymorphic Gates Controlled by a Special Signal. *WSEAS Transactions on Circuits*, **7**, 96-101.

[22] Gajda, Z. and Sekanina, L. (2011) On Evolutionary Synthesis of Compact Polymorphic Combinational Circuits. *Journal of Multiple-Valued Logic and Soft Computing*, **17**, 607-631.

[23] Sekanina, L. (2013) Ubiquity Symposium: Evolutionary Computation and the Processes of Life: Evolutionary Computation in Physical World. *Ubiquity*, **2013**, No. 2, 1-7.

[24] Miller, J.F. and Thompson, P. (2000) Cartesian Genetic Programming. *Proc. of the 3rd European Conference on Genetic Programming* (*EuroGP*'2000), **2000**, 121-132.