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A High Power-Added-Efficiency 2.5-GHz Class-F Power Amplifier Using 0.5 μm GaN on SiC HEMT Technology

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Abstract

This paper proposed the high-frequency, multi-harmonic-controlled, Class-F power amplifier (PA) implemented with 0.5 μm GaN Hetrojunction Electron Mobility Transistor (HEMT). For PA design at high frequencies, parasitics of a transistor significantly increase the difficulty of harmonic manipulation, compared to low-frequency cases. To overcome this issue, we propose a novel design methodology based on a band-reject, low-pass, output matching network, which is realized with passive components. This network provides optimal fundamental impedance and allows harmonic control up to the third order to enable an efficient Class-F behavior. The implemented PA exhibits performance at 2.5 GHz with a 50% PAE, 14 dB gain, and 10 W output power.

Keywords

GaN, High Power, Class-F

1. Introduction

In modern wireless communication systems, RF power amplifiers (PAs) are one of the most important part of the transmitters. Increasing the system efficiency, it is necessary that the PA is highly efficient as it is the most power hungry device. High efficiency of a PA means low power consumption, less cooling requirement, which reduce the overall cost of the RF front-ends as well. The original and novel design methodology schematic of class-F power amplifier is shown in **Figure 1** and **Figure 2**. When the waveform of V_{max} is too large, it may cause electric crystal burned limit, greatly reduces our ideas to make the design of the circuit. In order to improve this situation, we made the reinforcement foe class-F power amplifier circuit especially. At the output port, a $\lambda/4$ microstrip lines were used which operating frequency ω_0 as **Figure 1** shown. This schematic allows the odd-order harmonic signals are retained in the drain terminal, and even order harmonics signals were shorted to ground, and this design allows the drain terminal of the voltage waveform is adjusted to a square wave, avoid V_{max} impact caused by too much.

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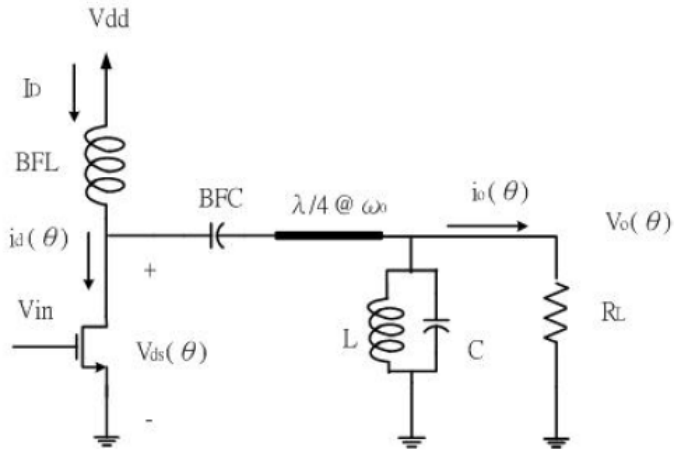

Figure 1. Original design methodology schematic of class-F power amplifier.

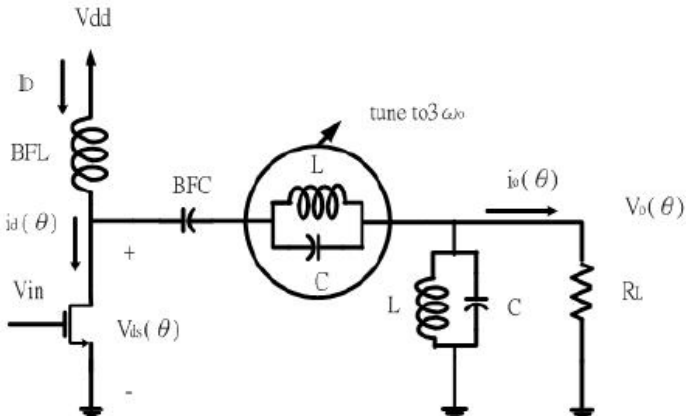

Figure 2. Novel design methodology schematic of class-F power amplifier.

The principle of class-F power amplifier is retained by an infinite number of odd-order harmonics signal waveform reshape using to produce the desired square-wave to improve the drain terminal of the voltage waveform, that if you do not use the microstrip line to achieve this result, there are other ways to solve. **Figure 2** shows an important answer, that is to use multiple sets of LC resonant circuit for the output matching network. Which can storage energy at fixed operating frequency, will affect the larger signal waveform reservations. As for the other less important signals are ignored on the power loss less area and the resonant circuit. For example, in **Figure 2**, this circuit only adds a LC resonant at $3\omega_0$, and in **Figure 3**, though the wave drain terminal voltage waveform has a little difference compare to the ideal square wave, but in inhibition of drain terminal V_{max} has significant performance. From this, when the odd harmonic signals richer, more connected composite waveform approximates a square wave, and the more conversion efficiency. In theory, more than the increase in the output of $5\omega_0$ even $7\omega_0$ resonant circuit, will contribute to better performance characteristics of the class-F power amplifier.

2. Circuit Design

The chip photograph is shown in **Figure 4**, only including input matching network where the passive components were arranged on the chip with dc and rf pads. And full schematic is shown in **Figure 5**. We used RC resonant to solving low frequency oscillation in rf input matching. The complete device small/large-signal modeling for HEMTs and passive components had been built for circuit simulation. The size of the chip is 1500 × 1000 μm^2, and the gate width for M is 12 × 100 μm^2. And the output matching network is on PCB with wire

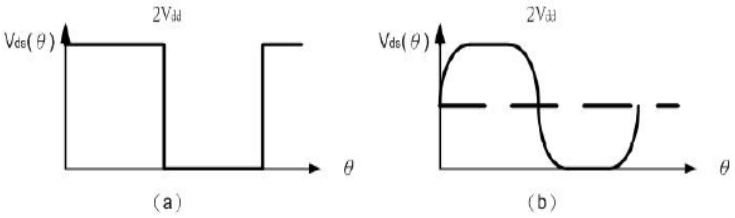

Figure 3. Waveform of class-F power amplifier.

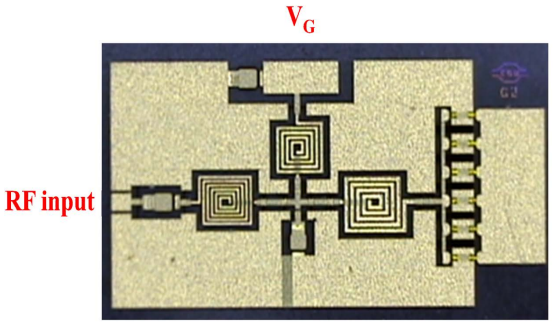

Figure 4. Chip photograph of the proposed PA.

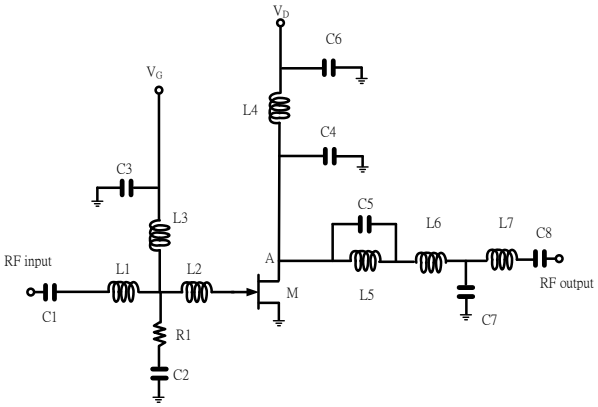

Figure 5. Schematic of the class-F power amplifier.

bonding as **Figure 6** shown. It presents that is used LC band-reject structure $3f_0$ and low-pass filter for f_0, that in order to reducing the loss from the effect of dc load. In the measurement setup, a off-chip inductor to be rf choke was used through bonding wire at the output port.

3. Experiment Result

The dc biases for first-stage amplifier are V_D = 28 V and V_G = −2.5 V. **Figure 7** shows the result measured and simulated small-signal return loss curves. The signal source for large-signal performance measurement was generated by Agilent E8257D Signal Generator. The output signal of the PA was measured by Agilent E4440A spectrum analyzer. We made S22 return loss at higher about 500 MHz than S11. Because when V_D = 28 V and V_G = −2.5 V, the transistor is on cutoff region. And when at the signal source for large-signal, the transistor will be into saturation. Then the output port will occur parasitics capacitance, it will make the return loss close to the lower frequency. **Figure 8** shows the curves of output power, power gain and PAE as a function of the input power at the frequency of 2.5 GHz. The maximum output of 40 dBm with PAE of 62% can be achieved in simulation. And the measured output power was limited with lower PAE performance about 50%. **Figure 9** exhibits the curves of saturated output power and gain versus frequency for measurement.

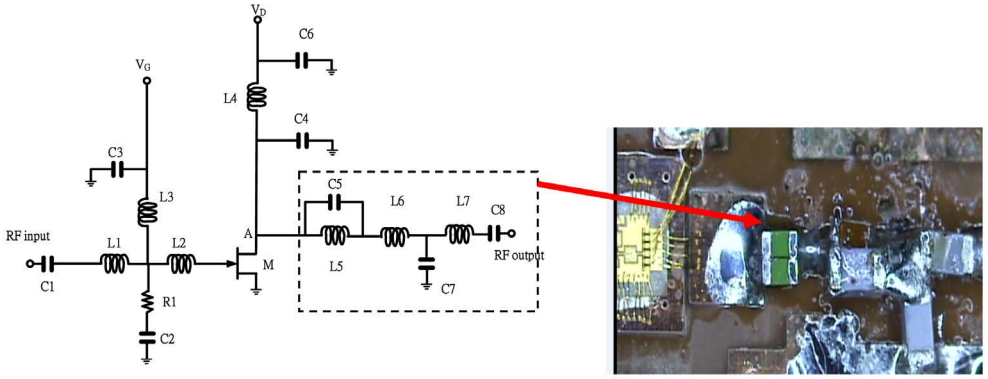

Figure 6. Output matching network of the class-F power amplifier.

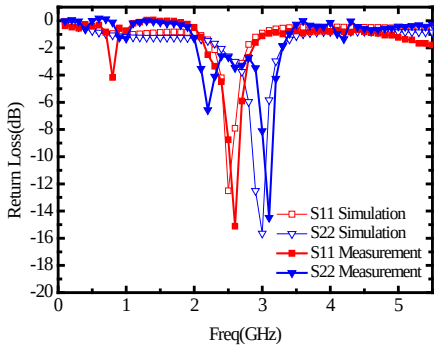

Figure 7. Return loss of the proposed class-F power amplifier.

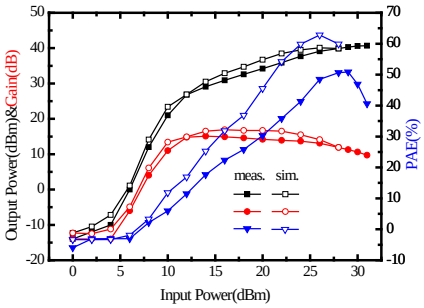

Figure 8. Large-signal performance of the proposed class-F power amplifier.

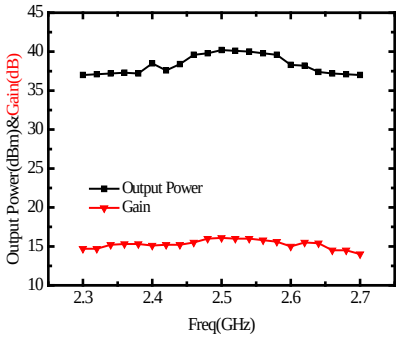

Figure 9. Saturation output power and gain as a function of frequency.

Table 1. Performance comparison of reported power amplifiers using a GAN device.

Refs	Class	Freq (GHz)	Gain (dB)	Pout (dBm)	PAE (%)
[1]	F	3.1	15	40	82
[2]	F^{-1}	3.37	14	39	76.9
[3]	F	2	12.7	40.7	70
[4]	EF	2.2	9.2	39.5	80
This work	F	2.5	14	40	50

4. Conclusion

This paper proposed class-F power amplifier in 0.5 μm GaN HEMT process. The input matching was designed on-chip to reduce the PA module size. The measurement of power amplifier has a high power performance from 2.3 GHz to 2.7 GHz. The chip size is 1.5 × 1 mm^2. The proposed power amplifier can be used for *S*-band communication system application. And the performance comparison is shown in **Table 1**.

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