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Fault Tolerance Limits and Input Stimulus Selection Using an Implemented FPGA-Based Testing System

Papakostas K. Dimitrios, Pouros P. Sotirios, Vassios D. Vassilios

Department of Electronic Engineering T.E, Alexander Technological & Educational Institute of Thessaloniki, Thessaloniki, Greece
Email: dpapakos@el.teithe.gr

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Abstract

In this paper, the selection of fault tolerance limits and input stimulus using an implemented adaptive FPGA-based testing system based on a method utilizing wavelet transformation of the current waveforms is presented. The testing scheme is innovative because it offers the ability of applying different input stimulus signals with respect to the requirements of the examined circuit. Moreover, the method used is simple, offers a single-point test measurement solution and may easily be adapted to test various other analog and mixed-signal systems. Experimental results are presented showing the advantages of the proposed testing scheme.

Keywords

Fault Detection, External Testing System

1. Introduction

Testing of analog and mixed-signal circuits has been an active research topic. Supply current testing methods, due to their simplicity and ease of application to a circuit under test (CUT), no matter how complex it is, have been investigated for several years and various approaches have emerged [1]-[4]. Methods based on the use of the wavelet transform, which resolves a signal in both time and frequency simultaneously [5]-[7], give an approximation of a transient current waveform for a certain frequency of the signal.

In this paper, the application of a fault detection method, based on the energy metric of the wavelet transform of the measured current waveforms of circuits (like the power supply current IPS or the output current IL), is used for the selection of input stimulus and fault tolerance limits.

A brief introduction to wavelets is outlined in the next section and the testing algorithm is described in Section 3. The description of the implemented FPGA-based testing system and details are given regarding the block diagram of the system. Experimental results and procedures are presented in Section 5. Discussions and directions for further work are concluding the paper.

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2. Wavelets Transform

The wavelet transform [8]-[10] is a transform that provides both time and frequency representation. It passes the time-domain signal from high pass and low pass filters, which filter out either high frequency or low frequency portions of the signal. This procedure is repeated every time some portion of the signal, corresponding to some frequencies, is being removed from the signal. The procedure is called decomposition. The decomposition is repeated to a predefined decomposition level. Next, a set of signals is produced which actually represents the original signal. The continuous wavelet transform (CWT) of a function $x(t)$ is defined as follows in Equation (1):

$$\mathrm{CWT}_{\psi}^{\chi}(\tau,s)=\Psi_{\psi}^{\chi}(\tau,s)=\frac{1}{\sqrt{|s|}}\int_{-\infty}^{\infty}x(\tau)\psi^{*}\left(\frac{t-\tau}{s}\right)dt \tag{1}$$

The transformed signal is a function of two variables, τ and s, the translation and scale parameters, respectively. $\Psi(t)$ is the transforming function, and it represents the mother wavelet. The variable τ represents the time shift (translation) while the variable s represents the amount of time scaling or dilation. The mother wavelet is a prototype for generating the other window functions. The used mother wavelet is called the Haar wavelet. The Haar wavelet is a step function taking values 1 and −1, on $[0,\ 1/2\ ]$ and $[\,1/2\ ,\ 1]$, respectively, as shown in **Figure 1**. The Haar mother wavelet is the simplest form of a wavelet and it is also proposed in literature [11] as an effective wavelet for mixed-signal test applications.

For sampled signals (as in our case) the Discrete Wavelet Transform (DWT) is used. The main idea remains the same as with the CWT. The Haar transform decomposes a discrete signal into two subsignals of half its length. One subsignal is a running average or trend; the other subsignal is a running difference or fluctuation *d*.

Since the energy of the trend subsignal *T* accounts for a large percentage of the energy of the transformed signal, in the following, the energy is computed by considering only the trend coefficients T_{1j} of the first decomposition level (Equation (2)):

$$E_{T1}=\sum_{j=1}^{n}T_{1j}{}^{2} \tag{2}$$

3. Testing Algorithm Based on Wavelets

The test method uses as a metric the energy value E_{T1} of the wavelet transform of the measured current waveforms. For the wavelet energy computation, the trend coefficients of the first decomposition level are considered. Since we are dealing with measurements on many known fault-free circuits with variations on parameter values, the notion of the nominal circuit is replaced by the notion of the reference circuit. The value of a parameter of the nominal circuit is substituted by the mean of the values of all fault-free circuit instances in the reference circuit.

The proposed test method is a two phase process. At the first phase (Initial Phase), the wavelet energy value for the reference circuit is measured and stored. In the second phase (Main Test Phase) the wavelet energy of the CUT is measured and compared with the corresponding value of the reference circuit. The detection of a faulty circuit instance will be successful when its wavelet energy value exceeds certain tolerance limits.

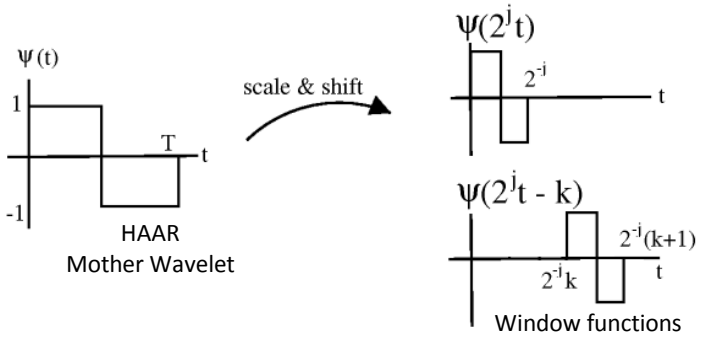


Figure 1. HAAR mother wavelet function.

Initial Phase: Multiple measurements for a number of known fault-free circuits are performed only in this phase, just to determine for the reference circuit: the (mean energy value from the trend $T1$ of the first level decomposition of all fault-free circuit instances) and its tolerance limit $E_{T1,0\text{-lim}}(I) = w \times E_{T1,0}(I)$ where $0 < w < 1$.

Main Test Phase:

For a CUT *t*:

- Measure and store $E_{T1,t}(I)$.
- If $|E_{T1,0}(I) - E_{T1,t}(I)| > E_{T1,0\text{-lim}}(I)$ then declare as faulty the *t* circuit instance using the energy value $E_{T1,t}(I)$ of *I*.

In order to include measurement inaccuracies and circuit parameter deviations, the range of values for the fault-free instances should be set to a properly selected value of *w*. It must be noted that this value of tolerance limit affects correct fault detection and yield loss. In our case, different values of w have been considered for comparison purposes.

4. The Implemented FPGA-Based Testing System

The load current (I_L) as well as the current of power supply lines (I_{PS+}, I_{PS-}) of the CUT are measured by the system and the CUT is classified accordingly. The basic block diagram of the procedure is depicted in **Figure 2**.

The current waveform of the CUT is measured and sampled by an external ADC and is driven to the FPGA. The processing of the sampled data initiates in the FPGA. The processed data provide information towards the creation of a signature database. Finally, by comparing signatures, obtained from the "good" circuit signatures, the classification is concluded. Both signatures, the good one and the CUT's, are compared with the help of a distance metric [12].

The sampled data from the ADC travel through a Digital Filter, used for antiallising and denoising purposes, as shown in **Figure 3**. The Signal Processing Unit performs the spectral analysis of the current signature using Fast Fourier Transformation and Discrete Wavelet Transformation algorithm to extract the energy of the signature. The rms and mean values of the current signature can be also calculated in the same unit.

The Digital Stimulus Pattern purpose is to apply the correct digital or analog signal (after a D/A conversion) to the CUT according to the specifications of the CUT. According to the used test method requirements, the pattern generator creates a new input stimulus that provides a different signature signal. This stimulus is created by LUT's, DDS and LFSR. The stimulus can also be user selectable, depending on the CUT.

The importance of the Digital Stimulus Pattern is its integration in an FPGA-based system as an innovative method. The automated or/and user selective mechanism provides the results presented in the next section. In this case, the results are driven by an automated, dynamically selected input stimulus method.

It must be pointed out that all the digital processing, the extracted wavelet energy of the signature, the rms and mean values of the current signature are also implemented inside the FPGA. Finally, the calculated signature is compared to the database signatures for comparing the "good" circuits due to classification purposes.

The FPGA used for the implementation is Virtex-5LXT FPGA from Xilinx. The FPGA is populating onto the XUPV5-LX110T Development Board from Xilinx. The FPGA has I/O pins which can be configured in a vast majority of operation modes among with a powerful Clock Management System for zero clock delay and jitter filtering.

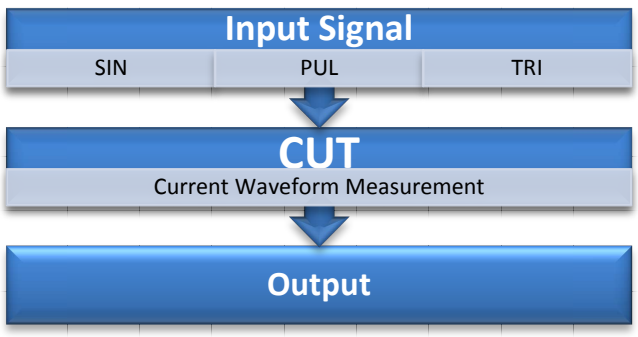


Figure 2. The basic procedure block diagram.

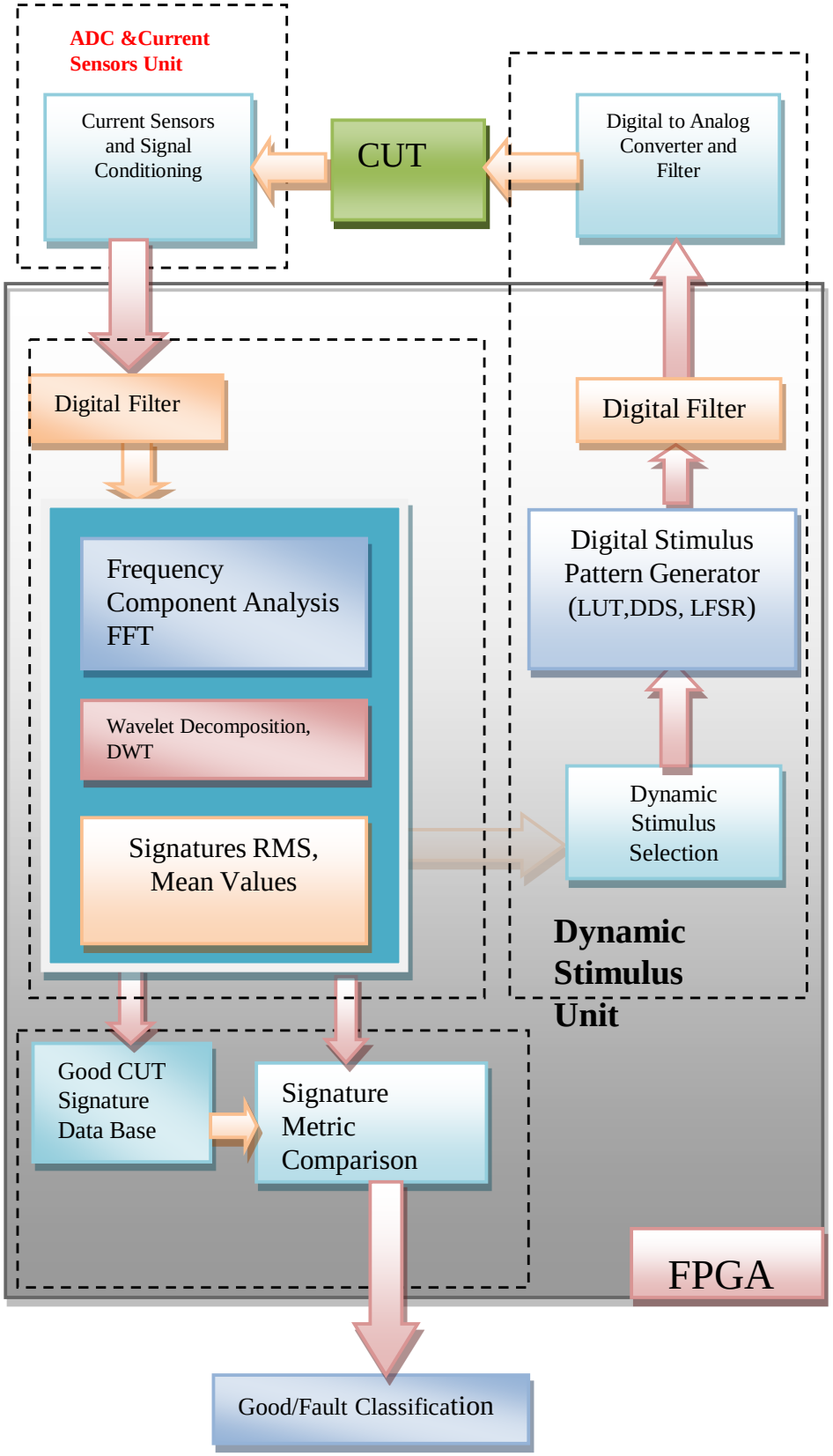


Figure 3. Block diagram of the implemented FPGA-based testing system.

5. Experimental Results

The test method of Section 3 is utilized by the implemented FPGA-based system described in Section 4 for testing various circuits. Results from a typical operational amplifier circuit (741 type) in an inverting amplifier configuration are presented. The circuit has been implemented using discrete components, where opens are implemented by a resistor of 10 M Ohm and shorts by a resistor of 10 Ohm.

The operational amplifier circuit consists of 24 bipolar transistors, one capacitor and 11 resistors. The fault list consists of all hard faults (shorts and opens) on passive components and bipolar transistors. Catastrophic faults include base-emitter, collector-emitter and base-collector short-circuits, resistor and capacitor short-circuits and open-circuits and transistor base open-circuit faults, as described in [13]. Faults, which could physically damage the circuit, were excluded from the fault list. The target fault set formed consists of 128 faulty cases (opens and shorts). With the described FPGA-based testing system, the input stimulus signals are dynamically selected and applied as Vin, from three different input stimulus, using appropriately the dynamic stimulus unit. A sinusoidal (SIN) input, a pulse (PUL) input and a triangular (TRI) input, at the same frequency of 1 KHz with an amplitude of 0.5 V are applied as required. From a set of n = 75 known fault-free circuits, the positive IPS+, the negative IPS− and the load current IL waveforms are measured. The required (Section 2) wavelet energy values are computed by the Signal Processing Unit of the implemented testing system according to the algorithm described in Section 3 and the percentage fault detectabilities for four different values of w (0.1, 0.05, 3σ = 0.036, 1σ = 0.012) are calculated and shown in **Figures 4-7**.

As it was mentioned earlier, the value of the tolerance limit w affects the correct fault detection and also the yield loss. From the data, it is clear that the lower the value of w is, the higher fault detectability value achieved. But when the proposed test method is to be applied to a production line, it is crucial that no faulty products are misclassified as fault-free. In order to do so, a tight bound limit on the value of w (for example w = 1σ) needs to be set. However, the tighter the bounds for w, the larger the percentage of fault-free products classified as faulty. This may result to an unacceptable large yield loss. Therefore, for the value of w some compromises between the above mentioned conflicting constraints need to be made.

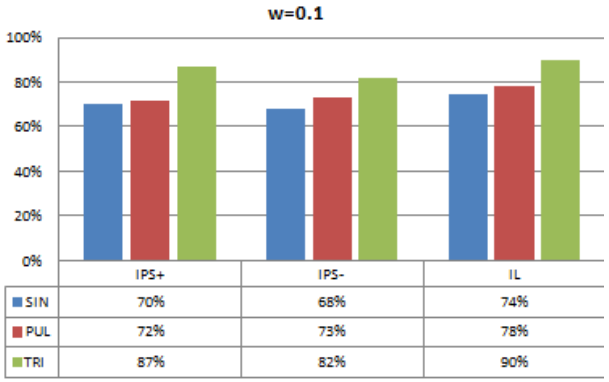


Figure 4. The percentage fault detectability values for w = 0.1.

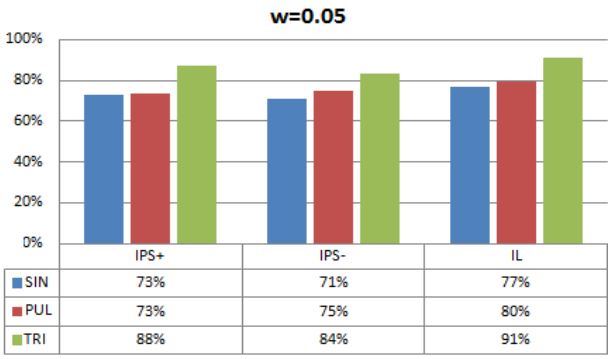
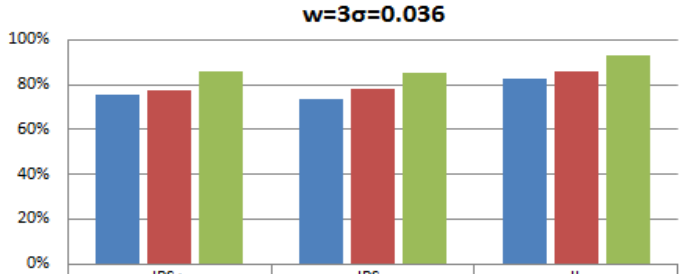
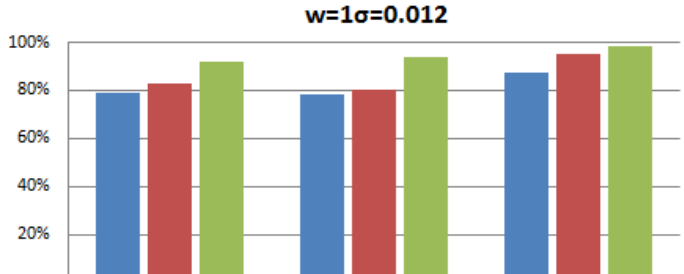


Figure 5. The percentage fault detectability values for w = 0.05.



	IPS+	IPS-	IL
SIN	76%	73%	83%
PUL	77%	78%	86%
TRI	86%	85%	93%

Figure 6. The percentage fault detectability values for w = 3σ = 0.036.



	IPS+	IPS-	IL
SIN	79%	78%	88%
PUL	83%	80%	95%
TRI	92%	94%	98%

Figure 7. The percentage fault detectability values for w = 1σ = 0.012.

The data show that, for all the four different values of *w*, the triangular input stimulus consistently outperforms the pulse input, while sinusoidal input signal follows with the lowest fault percentage detectability. The results also show that the non-linear (pulse or triangular) input stimulus always gives larger fault detectability values than the linear sinusoidal signals.

Another notable feature, depicted is the fact that the load current IL measurement always offers greater fault detection ability than the positive and negative current measurement waveforms. This observation raises a question which needs further study on as to whether it is more preferable, in terms of fault detection, the usage of current measurements on the positive IPS+ or the negative IPS− in a circuit with dual power supply. In such cases, the utilization of the IL measurements for fault detection may prove to be advantageous as it is demonstrated by the presented experimental results.

6. Conclusions and Future Work

Comparison of fault detectability tolerance limit using an adaptive FPGA-based testing system which relies on a method incorporating wavelet transformation of current waveforms is presented. The implemented testing scheme offers the ability of dynamically applying different input stimulus signals and computing the fault detectabilities using different tolerance limit values with respect to the requirements of the examined circuit. The advantages of the method are the simplicity, the measured current signal and the single test point.

An application of the proposed method, for testing an operational amplifier circuit in an inverting configuration, implemented with discrete components, is presented. Concerning the examined circuit case, it is observed that the utilization of the IL current measurements by the proposed test method may result in higher fault coverage than the use of the IPS current. It is also observed that the lower the value of w is, the higher fault detectability value achieved, while the yield loss increases when the method is to be applied to a production line testing. Comparative results from three different input stimuli, using four different tolerance limit values, show that the

non-linear input stimulus always gives larger fault detectability values than the linear sinusoidal signals.

Work is under way to exploit other testing methods using the implemented FPGA-based testing system in order to improve detectability, as well as to apply the presented method for testing other mixed-signal circuits. Also, a selection algorithm for the tolerance limit value *w*, according to fault detectability maximization and yield loss minimization has to be investigated.

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