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Limitations of On-Wafer Calibration and De-Embedding Methods in the Sub-THz Range

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ABSTRACT

This paper investigates frequency limitations of calibration and de-embedding techniques for S parameter measurements. First, the TRL calibration methods are analysed and the error due to the probe movement when measuring the different line lengths is quantified, next the coupling between the probe-heads and the wafer surface is investigated and finally an upper frequency validity limit for the standard Open-Short de-embedding method is given. The measured results have been confirmed thanks to the use of an electro-magnetic simulator.

Keywords: TRL; Open-Short; De-Embedding; Calibration

1. Introduction

The frequency range in electronic applications is continuously increasing during the past few years to reach the range of hundreds of Gigahertz. The associated bipolar and CMOS transistors used as elementary components for these high frequency applications have maximum oscillation frequency reaching the half Terahertz [1]. Hence, characterisation of advanced SiGeC HBT and CMOS devices and their associated passive elements are more and more challenging. First, different calibration techniques of the network analyser such as TRL and SOLT at frequency higher than 50 GHz need to be verified. Moreover, associated device modelling requests accurate characterisation of the intrinsic device, e.g. free of parasitic elements such as pads, vias and interconnects. Hence, conventional de-embedding techniques such as Open-Short need to be refined for higher frequencies. It has already been shown that calibration and de-embedding techniques are less accurate when the frequency increases [2]. Some parasitic effects, formerly negligible, are now strong enough to modify significantly the S-parameters measurement [3,4]. This paper investigates three different errors that can commonly occur in Sub-THz measurements and which are mostly not taken into account: First, a practical limitation of the TRL technique is presented due to the measurements of different line lengths. Then, a second limitation of the calibration technique due to the difference between the calibration substrate and the device under test structure is explored. Finally, a limitation of the conventional de-embedding Open-Short method is highlighted on active and passive elements.

2. Influence of the Probe Movement during Measurement

The TRL calibration method is based on the measurement of three different standards:

- a reflect, which can be an open or a short and need to be as symmetrical as possible
- a short line, (called through in the rest of the paper)
- a long line, (called line in the rest of the paper)

The TRL is based on the measurement of two lines with different lengths [5]. In between the measurements of these lines, one probe is moved as described on the top of the **Figure 1**. When this probe is moved, the measurement environment is altered at high frequency. For example, crosstalk between probes is reduced, the probe contact resistance can be changed and the position of the cable is slightly changed when moving the probe head. Due to these small modifications of the measurement environment the calibration is less accurate at high frequencies. Hence, we expose a method to quantify the error introduced by moving the probe head. A special test structure has been designed using two open structures with different distances between the probes, see **Figure 1**.

First, the impedance of the Open structure "A" is measured. Then, the left probe is moved away along the

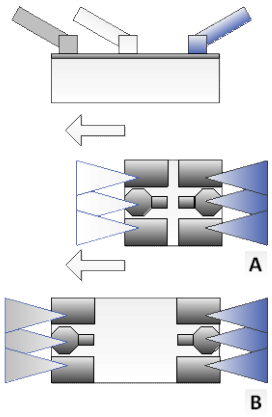

Figure 1. Sketch of the probes movement front (up) and top view (down).

x-axis as shown by the white arrow on **Figure 1**. The Open structure "B" is measured and then the two measurements are compared.

On the **Figure 2**, the admittance (y-parameter) and capacitance for the right probe are shown. This probe is not moved between the two measurements.

The admittance is exactly the same for each measurement and the capacitance has the same behaviour, only an offset is visible.

Figure 3 shows the admittance and capacitance for the left port before (red curve) and after the probe movement (blue curve).

On this figure, the admittance's maximum is shifted to lower frequencies by 15 GHz and raised by 0.5 mS (~50%) between the two measurements. The graph also shows a modification in the behaviour of the test structure's electrical characteristic above 50 GHz. There is a drop in the capacitance value. This result is not-physical because the test structure is still the same!

As a conclusion, above 50 GHz, a probe movement can introduce measurement errors. This can be critical because the line measurement is one of the key-steps during TRL-calibration.

3. Coupling between Probes and Test Structures under the Probes

Due to the cost of the silicon area, test structures are placed as close as possible to each other.

The RF probes are large compared to the pad size, and a part of the probes is right above the neighbouring structures. The structures under the probes make a strong coupling with the RF probes [3]. To quantify this coupling, we carried out the following measurements shown on **Figure 4**. The red and blue triangles are the RF probes in GSG configuration. The cell called "A" does not have any coupling under its left probe. The cell called "C" does not have any coupling under its right probe while the structure "B" is totally symmetric and has a coupling on both sides. The three measured test-structures are identical and symmetrical (open). Consequently, the measured characteristics should be symmetrical (S_{11}

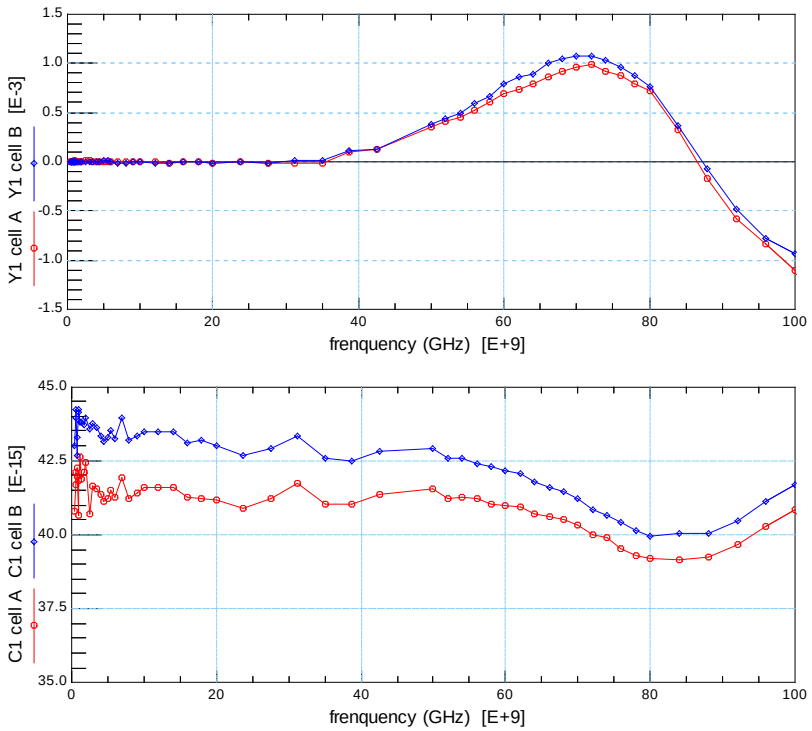

Figure 2. Port 2 admittance (up) and capacitance (down) before and after left probe move.

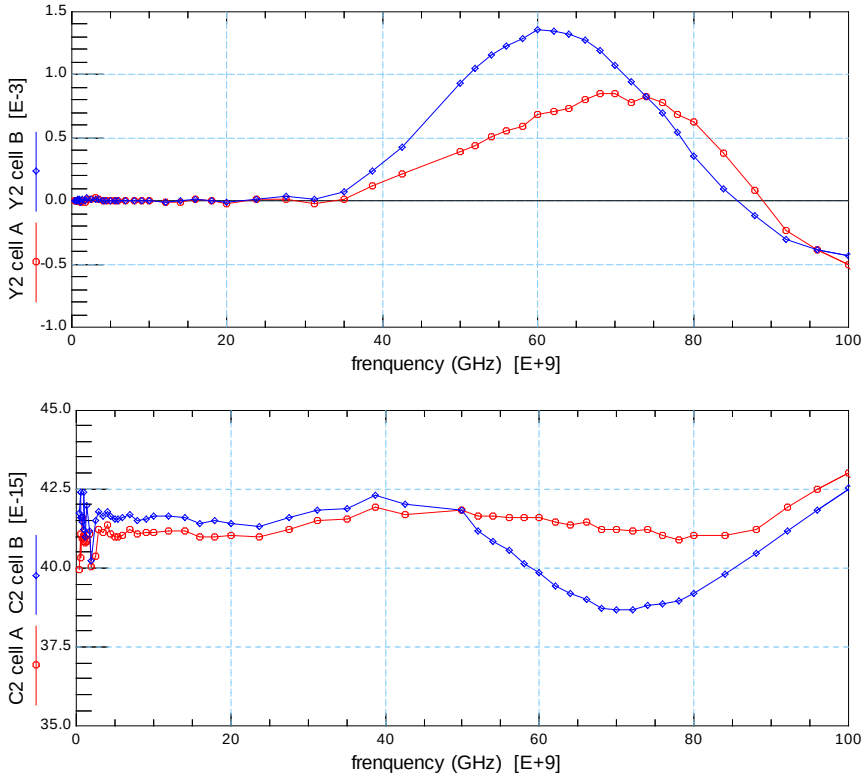

Figure 3. Port 1 admittance (up) and capacitance (down) before and after left probe move.

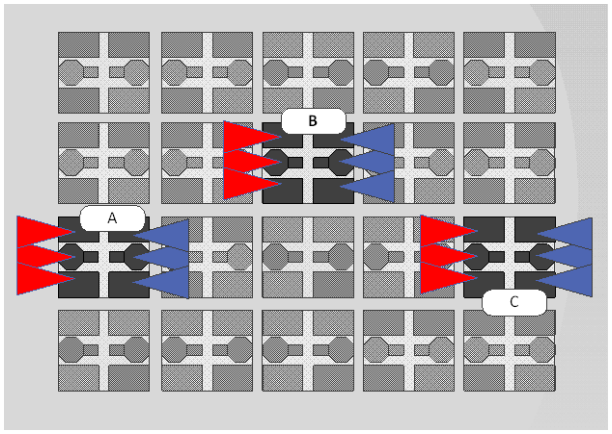

Figure 4. Placement of the measured test structures.

= S_{22}). The difference that we can see is due to the coupling between probe and the neighbour test structures under it.

The middle graph of the **Figure 5** shows the coupling between probes and test structures under it. Thanks to the symmetry of the structure, the behaviour of the two ports of the cell "B" is completely symmetrical (S_{11} = S_{22}).

On the top and bottom graph, we can see that the measurement is no longer symmetrical; this is due to the absence of test structures under the left probe for the first graph and under the right probe for the third one.

For on-wafer measurement, the coupling between

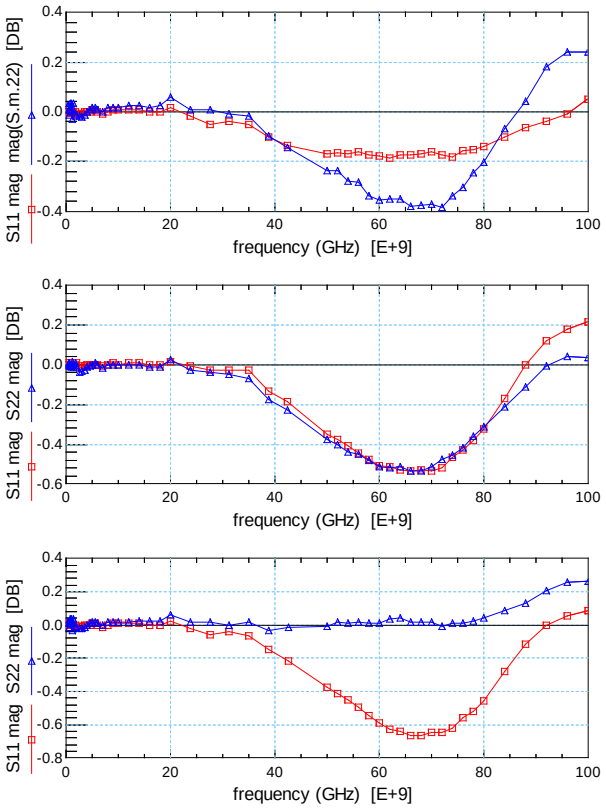

Figure 5. Measurement results for the cell A (up), B (middle), C (down).

probes and test-structures can be controlled by the insertion of dummies on the first and the last column of the chip. E.g. Single port calibration standards can be inserted in those columns.

Another question arises here. Usually the calibration is done with an ISS-standard substrate. The surface of this calibration substrate is completely different compared to the wafer surface and consequently the coupling during calibration is different compared to the measurement. The only solution to correct for the coupling is to use on-wafer calibration structures and no longer use the ISS-standard.

4. Open-Short De-Embedding Limitation

During the high frequency measurement of a large multi-finger transistor (HBT), the S_{11} (**Figure 6**) shows a non-physical behaviour after the de-embedding with the Open-Short methodology (OS).

The impedance (represented by the magnitude of S11) is higher after the de-embedding (red line) because the losses (especially through the pads) are compensated. The **Figure 6** also shows that the de-embedded magnitude is increasing with frequency after 60 GHz which is not physical for the measured input impedance of the HBT. This non-physical behaviour is due to over compensation of the pad capacitance during de-embedding. In order to validate this hypothesis, EM simulation has been carried out. The methodology is explained on **Figure 7**.

First, an inductance is simulated with HFSS without the back-end. From a technical point of view, when using an electromagnetic simulator, it is not possible to define a port near a discontinuity. A work-around was to add a short line, make the simulation of the whole structure and then to remove the short line using the standard de-embedding procedure. This is represented on the first line of the **Figure 7**.

In a second step, the same inductance is simulated with the back-end (see second line of **Figure 7**). A Short and an Open are also simulated and the OS de-embedding is performed. The simulation results are shown on **Figure 8**, upper part: magnitude, lower part: phase.

The simulation results of the inductance without back-end are given by the red curve. The simulation results of the inductance after OS de-embedding are given by the blue curve. Theoretically, a perfect superposition of the red and blue curves is expected, but a large difference appears above 40 GHz, especially for the magnitude. A similar increase of the magnitude in the high frequency range is visible as already before seen during measurements (**Figure 6**, red line). We can conclude that above 60 GHz, the OS de-embedding introduces a non negligible error.

For accurate measurements, a new de-embedding method is needed. The 6 dummies method developed in [2] and [6] is highly recommended in this frequency range.

5. Conclusions

High frequency calibration and de-embedding techniques have been analyzed and their validity range has been checked: 1) the TRL calibration need the measurements of two different line lengths introducing the movement of the probe-heads for on wafer-measurements. This movement can introduce errors and make the calibration less precise above 40 GHz. 2) the coupling between the probe-heads and the underlying wafer-surface introduces an error when the structures on the wafer that are under the probe-heads are not identical. A work around is to pay particular attention when designing the test-structures to take this effect into account.

The most widely used de-embedding technique (Open-Short) introduces major errors in measurement above 60 GHz. The 6 dummies method developed in [6] is highly recommended above this frequency range.

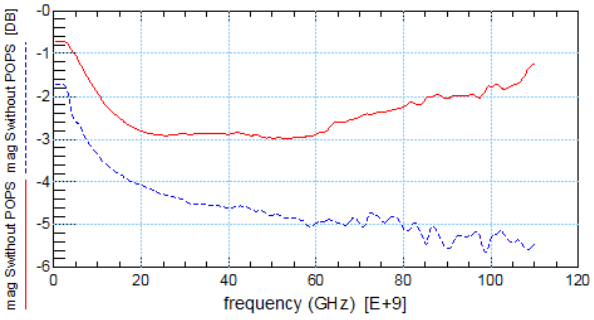

Figure 6. Magnitude (up) of a transistor S11 without OS (blue line) and after OS (red line).

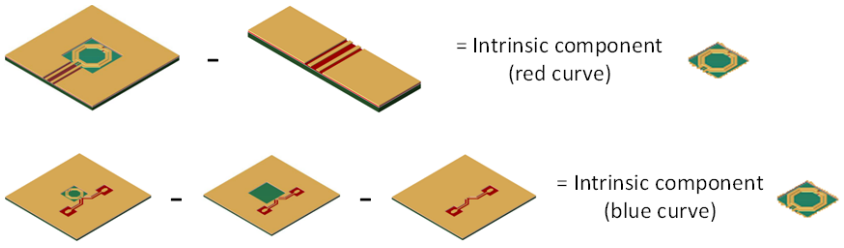

Figure 7. The five structures simulated with HFSS and the two methods of extraction.

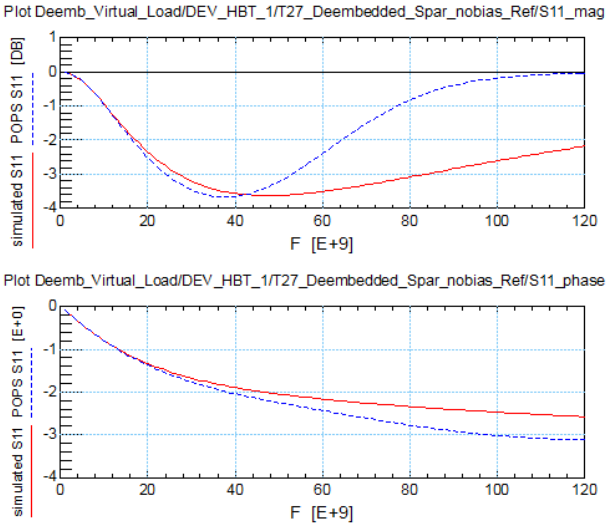

Figure 8. Simulation magnitude (up) and phase (down) of an inductance; intrinsic (red) and extracted with OS de-embedding (blue).

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