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Design of low-offset low-power CMOS amplifier for biosensor application

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ABSTRACT

A compacted and low-offset low-power CMOS amplifier for biosensor application is presented in this paper. It includes a low offset Op-Amp and a high precision current reference. With a novel continuous-time DC offset rejection scheme, the IC achieves lower offset voltage and lower power consumption compared to previous designs. This configuration rejects large DC offset and drift that exist at the skin-electrode interface without the need of external components. The proposed amplifier has been implemented in SMIC 0.18-μm 1P6M CMOS technology, with an active silicon area of 100 μm by 120 μm. The back-annotated simulation results demonstrated the circuit features the systematic offset voltage less than 80 μV, the offset drift about 0.27 μV/℃ for temperature ranging from –30℃ to 100℃ and the total power dissipation consumed as low as 37.8 μW from a 1.8 V single supply. It dedicated to monitor low amplitude biomedical signals recording.

Keywords: Biomedical Integrated Circuit; CMOS Amplifier; Low-Offset and Low-Power; DC Offset Rejection; Biomedical Sensor

1. INTRODUCTION

Recently, there is increasing demand for portable and wearable devices to continuously monitor vital signals such as electroencephalography (EEG) and electrocardiography (ECG), blood pressure, etc. [1]. These devices usually contain various types of biosensors. CMOS amplifier is a crucial block at the front-end of these sensors, because most biomedical signals are characterized by their relative weak amplitude and low frequency, usually of few mV or less and the frequency below 1 kHz [2]. Meanwhile, these signals are often accompanied by large DC offset caused by skin-electrode interface. Therefore, amplifying such weak signals requires an amplifier with low-offset and low-offset drift, which is quite challenging without using any trimmed components.

There are some techniques have been developed to deal with the design challenges. Alternatively, auto-zeroing (AZ), correlated double sampling (CDS) and chopper stabilization techniques (CHS) [3,4,5,6] are utilized in sensor amplifier design to obtain DC offset rejection and high noise performance. However, these circuits have some disadvantages such as the employment of large capacitors, either off-chip or on-chip. Furthermore, these circuits add many CMOS switches that inevitably introduce switching noise, thermal noise, residual nonlinear switch errors and the CHS circuit consumes more power as circuit working in the chopping frequency. In fact these circuits were optimized for low flicker noise at the cost of higher bandwidth and worse thermal noise performance [7]. Trimming amplifier's components is another skill, but performance of this circuit is strongly related to the on-chip components matching and it increases the cost.

As a result, we turned to the CMOS amplifier design using continuous-time technique for high performance and low-cost solution. In this paper, an integrated continuous-time CMOS amplifier with low-offset voltage and low-power consumption was designed to meet the required biosensor. The proposed amplifier, designed in SMIC 0.18-μm CMOS technology, achieved less than 80 μV offset voltage and consumed only 37.8 μW under a 1.8 V supply. It is a good candidate for biosensor application.

2. CIRCUIT IMPLEMENTATION

Amplifier is an important block at the front-end of the biosensor system as in [8]. **Figure 1** shows the architecture of the integrated CMOS amplifier. It consists basically of three blocks, which are current reference, bias generator and low-offset amplifier core. A high precision

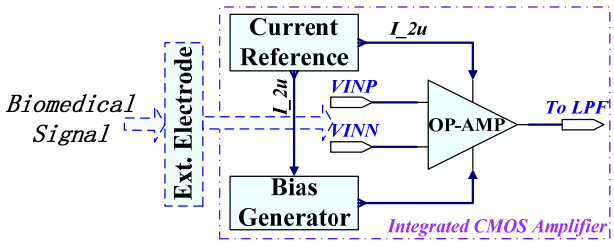

Figure 1. Architecture of the proposed integrated CMOS amplifier.

current reference was integrated in this design, it generated multiple branches of 2 μA temperature and supply independent current and were used to bias the amplifier and the bias generator. The complete schematic diagram of the proposed integrated CMOS amplifier is depicted in **Figure 2**.

2.1. Current Reference/Bias Generator

Minimizing the variation of the reference current and bias voltage for amplifier is crucial as well as achieving high performance in sensor systems. A novel compensation scheme for supply and temperature dependency of MOSFET-only current reference was presented in this design [9]. The complete schematic of the reference is shown in **Figure 2**. It includes start up circuit, self-based current generator, supply and temperature compensation circuit.

The operation principle is that if two current outputs having the same dependency on supply voltage and temperature are subtracted with proper weighting, the compensation output would be obtained. As demonstrated in **Figure 3**, two self-biased current references generated I_{out1} and I_{out2}, respectively.

$$I_{out1,2} = \frac{2}{\mu_p C_{ox} (W/L)_p} \cdot \frac{1}{R_s^2} \cdot (1 - \frac{1}{\sqrt{K_{1,2}}})^2 \quad (1)$$

Two current mirrors are adopted in this circuit to copy the currents I_{out1} and I_{out2} to get I_{m1} and I_{m2}. The size of the transistors and the resistance R_S are determined so the two current outputs I_{m1} and I_{m2} have the same supply dependency and different magnitude. Then, by subtracting I_{m2} from I_{m1}, the supply independent output current I_S could be obtained, but it is still a function of temperature. Through a simple analysis, the supply compensated output current I_S was given by:

$$I_{out1,2} = \frac{2}{\mu_p C_{ox} (W/L)_p} \cdot \frac{1}{R_s^2} \cdot \left[(1 - \frac{1}{\sqrt{K_1}})^2 - (1 - \frac{1}{\sqrt{K_2}})^2 \right] \quad (2)$$

For the negative temperature coefficients of resistor R_S and μ_P, the supply independent current I_S has a proportional-to-absolute-temperature (PTAT) characteristic. The drain current of PMOSFET, I_T, its temperature coefficient is also positive. Then the temperature compensated output current I_{REF} could be obtained by subtracting I_T from I_S. In bias circuit, the master biasing current and voltage of the complete amplifier were derived from the supply and temperature independent current reference.

2.2. Low-Offset Operational Amplifier

Offset in operational amplifier originates in both random and systematic manner [10]. The random offset comes from imperfect fabrication of identical devices. The systematic offset can be considered as errors in the design, it occurs due to the channel length modulation of transistors and the magnitudes of the offset voltages are different according to the input and output common-mode voltages [11]. In this design, a continuous-time asymmetrical differential input structure with active DC offset rejection circuit was implemented to minimize the systematic offset of the amplifier [12,13].

The principle of the active DC offset rejection technique is illustrated in **Figure 4**, considering the amplifier connected as a unity gain following configuration, where the input swing is nearly equal to the output swing. The common-mode level of the input and the output could be detected and amplified by the DC offset rejection circuit, and changed to the feedback signals for current sinks of the amplifier. This is a negative feedback network. By adjusting the current of the current sinks, the input and the output common-mode voltage would be maintained in same level to minimize the systematic offset.

As depicted in **Figure 2**, the circuit of low-offset

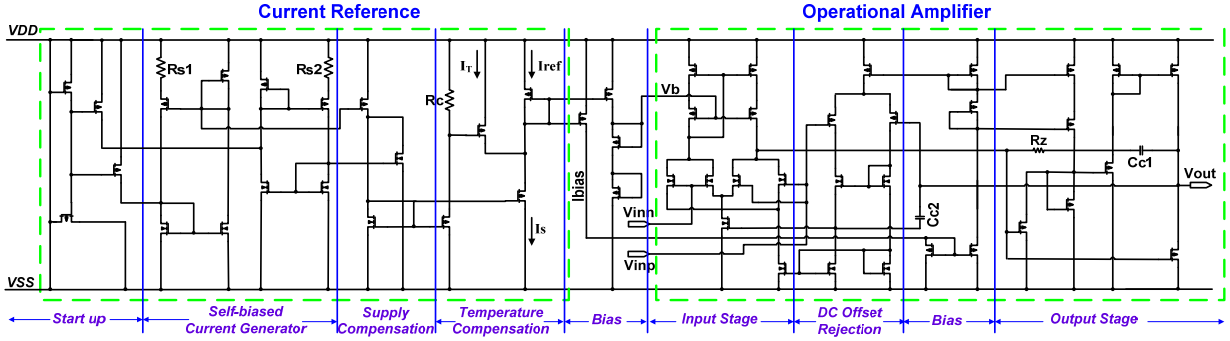

Figure 2. Complete schematic diagram of the integrated CMOS amplifier.

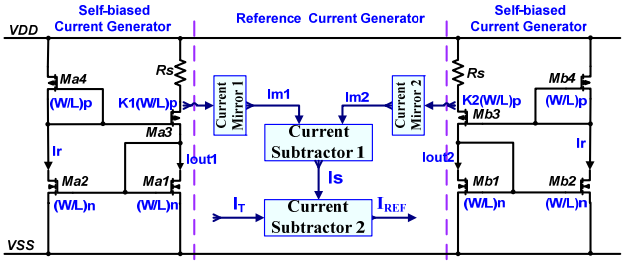

Figure 3. The basic principle of the current reference.

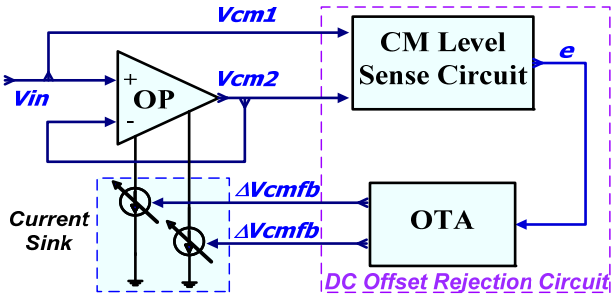

Figure 4. The principle of the DC offset rejection technique.

amplifier is divided into three parts: input stage, DC offset rejection circuit, and output stage. In input stage, the input MOS transistor pairs were designed as asymmetrical differential structure. Besides, the input transistors and active load transistors with appropriate dimensions were used in order to obtain good matching characteristic. In DC offset rejection circuit, a single stage OTA structure was adopted to amplify the difference between input and output common-mode level. Therefore, via cascading the NMOS pairs to obtain the large gain of the OTA. In output stage, the class-AB structure was designed to improve the power efficiency, open-loop gain and driving capability. RC Miller compensation and capacitor compensation techniques were used in this circuit [14].

Finally, a careful layout was planned to reduce process-related random offset: a) the symmetrical layout style was addressed through the entire layout, b) common-centroid cross-coupling layout strategy together with poly guard rings were adopted for critical devices and c) input pairs, active mirror loads and current sources that need to be matched were selectively grouped and arranged with dummies to minimize the effect of spacing-dependent parameter mismatch [15].

3. SIMULATION RESULTS AND DISCUSSIONS

This design has been implemented using the SMIC 0.18-μm CMOS 1P6M technology. **Figure 5** shows the complete layout of the integrated CMOS amplifier, with total silicon area of 100 μm by 120 μm. This chip has sent to be fabricated. We will test it with real-world physiological signals in near future.

3.1. Current Reference

The temperature drifts and supply regulation of the reference current are shown in **Figures 6 (a)** and **(b)**, respectively. The reference offered a current of 2 μA when adjusted to have a zero temperature coefficient at room temperature. It could be observed that an overall temperature coefficient of 0.625nA/°C is obtained between 0°C and 80°C, which corresponds to about 2.2% variation. The response of it is better for temperature from

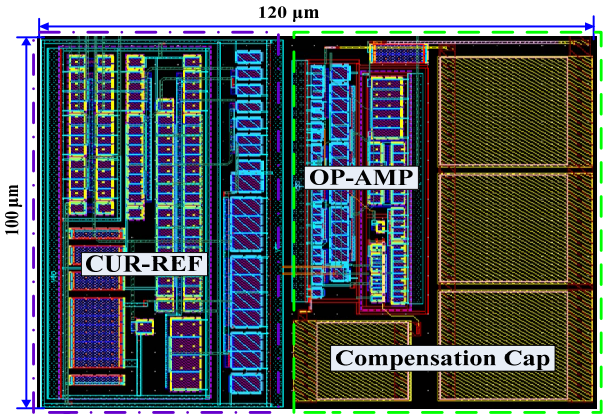

Figure 5. Layout view of the integrated CMOS amplifier.

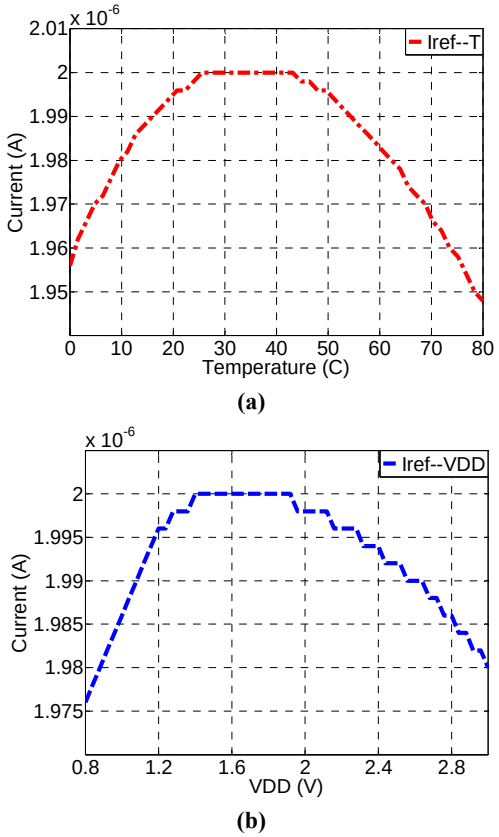

Figure 6. Layout view of the integrated CMOS amplifier Simulated reference current dependence on temperature (a) and supply voltage (b).

20°C to 50°C with a temperature coefficient of 0.13n A/°C. The line regulation of reference current is about 0.55%/V when the supply voltage ranges from 0.8 V to 3 V.

3.2. Low-Offset Operational Amplifier

Figure 7 shows the AC responses of the integrated CMOS amplifier while driving a 3 pF capacitive load. It offered 60 dB open-loop gain, 63.5° phase margin, and 2.82 MHz unity gain bandwidth. DC sweep analysis of the amplifier connected in an inverting unity-gain configuration is shown in **Figure 8**. The simulation results showed good following characteristic between Vin and Vout, and the offset voltage less than 80 µV by averaging. **Figure 9** depicts the offset drifts of the amplifier over a wide temperature range from –30°C to 100°C. The mean offset drift is 0.24 µV/°C, it illustrated the integrated CMOS amplifier was able to sustain low offset voltage over a wide temperature range.

The performance achieved in this design was compared with other state-of-the-art designs for biomedical application. As listed in **Table 1**, it could be seen that our design offered comparable performances. The proposed

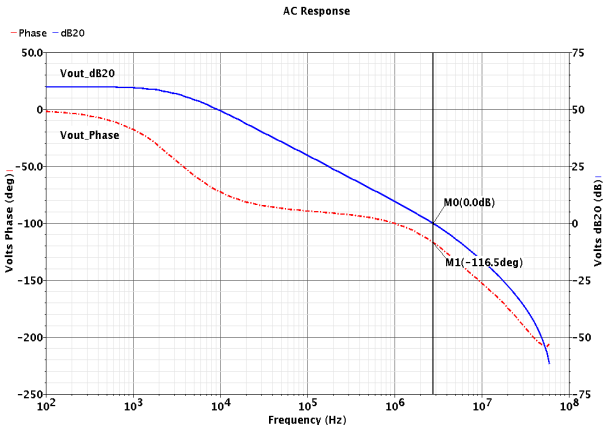

Figure 7. AC simulation results of the integrated CMOS amplifier.

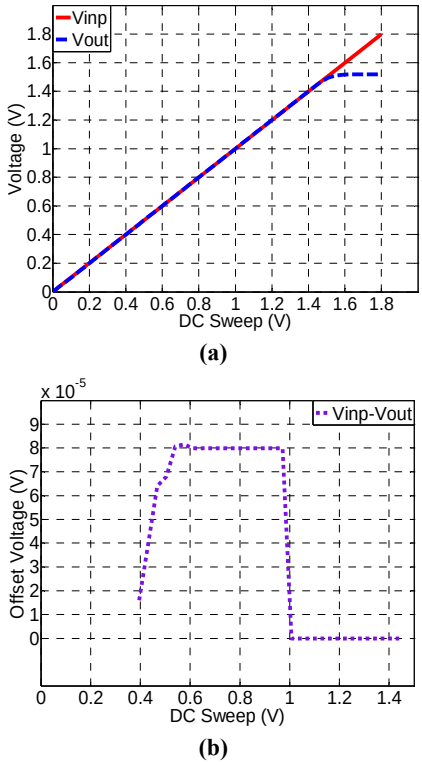

Figure 8. The simulation results of the following characteristic (a)and offset tunning range (b).

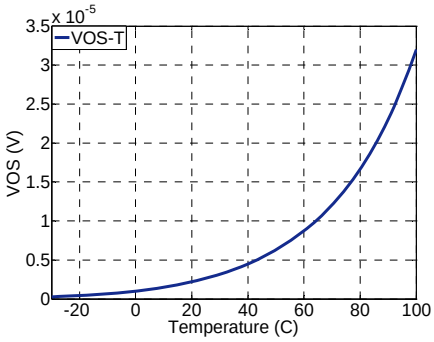

Figure 9. The offset variation with temperature.

Table 1. Performance comparison with other publications. (*instrumentation amplifier)

Parameter	Ref [5] 2002	Ref [16] 2004	Ref [17]* 2005	Ref [18] 2007	This work
CMOS Technology	0.7-µm	1.5-µm	0.35-µm	0.18-µm	0.18-µm
Supply	5 V	3 V	3~4 V	1 V	1.8 V (Typical)
Gain	60.6 dB	39.3 dB	56 dB	14 dB	60 dB
Phase Margin	—	—	—	—	63.5°
Unity Gain Bandwidth	5.5 kHz	2.7 KHz	130 KHz	2.7 KHz	2.82 MHz
CMRR	137 dB	—	100 dB (@60 Hz)	—	>85 dB (@DC-100kHz)
PSRR	—	50 dB	—	50 dB	>100 dB (@DC-10kHz)
Positive Slew Rate	—	0.64 V/µs	50 mV/µs	10 mV/µs	3.45 V/µs
Negative Slew Rate	—	0.64 V/µs	50 mV/µs	10 mV/µs	1.67 V/µs
Input Offset Voltage	88.7 µV	~811 µV	0.3 mV	1.7 mV	80 µV (max)
Offset Drift	—	—	—	—	0.27 µV/℃
Power Dissipation	11 mW	114.8 µW	72.6 µW	3.15 µW	37.8 µW
Core Area	5 mm^2	0.107 mm^2	0.2 mm^2	0.056 mm^2	0.012 mm^2

CMOS amplifier performed technical merits of low-offset voltage, reasonable low-power and with relative small die size, confirming the effectiveness and robustness of the proposed circuit architecture when using both circuit design technique and careful layout technique.

4. CONCLUSIONS

A low-offset low-power and compacted CMOS amplifier with continues-time active DC offset rejection design technique for biosensor applications is presented on-chip in this paper, without the need of trimming. To improve circuitry robustness over power supply and temperature, a high precision current reference was integrated in this design. The whole circuit occupies an area of 100 μm by 120 μm. The back-annotated simulation results suggested that this integrated CMOS amplifier can offer significantly enhanced metrics, in terms of the low-offset less than 80μV, the offset drift about 0.27 μV/℃ for temperature ranging from –30℃ to 100℃, and the total power dissipation approximately 37.8 μW at a single 1.8 V power supply. This integrated CMOS amplifier is particularly useful for a wide range of biosensor applications where a front-end preamplifier is required.

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