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A spatiotemporal signal processing technique for wafer-scale IC thermomechanical stress monitoring by an infrared camera

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ABSTRACT

In this paper, we describe a new silicon-die thermal monitoring approach using spatiotemporal signal processing technique for Wafer-Scale IC thermomechanical stress monitoring. It is proposed in the context of a wafer-scale-based (WaferIC™) rapid prototyping platform for electronic systems. This technique will be embedded into the structure of the WaferIC, and will be used as a preventive measure to protect the wafer from possible damages that can be caused by excessive thermomechanical stress. The paper also presents spatial and spatiotemporal algorithms and the experimental results from an IR images collection campaign conducted using an IR camera.

Keywords: Thermal Monitoring; Ring Oscillator (RO); Spatial; Spatiotemporal; Thermo-Mechanical Stress; Temperature Sensor; Thermal Analysis; WaferIC; Wafer-Scale System

1. INTRODUCTION

An innovative reconfigurable Wafer-Scale Integrated Circuit (WaferIC) for rapid electronic systems prototyping has been introduced [1-3]. Electronic components can be placed anywhere at the smart active surface of the WaferIC. Then those components can be detected, powered and interconnected through a complex but regular reconfigurable network laid over the surface of the WaferIC. As power consumption depends on user chips location and power pins distribution, it is not evenly distributed throughout the surface of the silicon wafer. In many cases, it is unpredictable and variable as power consumption of programmable or dynamic components (e.g. microcontrollers) depends on their activities. Therefore, managing thermomechanical stress is a real challenge and it may need to be monitored at all time in high performance applications.

Thermal monitoring is essential in high performance integrated structures implemented as multilayer structures composed of different materials. An increase of the internal temperature of some circuits can lead to significant thermal and thermo-mechanical problems. Understanding thermal phenomena occurring on a micro-scale level is essential for SoC and MEMS-based applications. Thus, measurement techniques are needed to validate models predicting thermal behavior of integrated structures. In particular, measurement techniques are needed to obtain surface temperature distributions of large integrated structures.

Due to technology scaling, power density of high performance integrated structures has increased drastically. For example, the power density of high performance microprocessors has already reached 50 W/cm^2 at 100 nm technology and was forecasted to reach 100 W/cm^2 at 20 nm technology. Meanwhile, to mitigate the overall power consumption, many low power techniques have been proposed [4-10]. These techniques, though helpful to reduce the overall power consumption, may cause significant on-chip thermal gradients and local hot spots due to different clock/power gating activities and varying voltage scaling. It has been reported in [11] that temperature variations of 30˚C can occur in a high performance microprocessor design. The magnitude of thermal gradients and associated thermo-mechanical stress is expected to increase further as VLSI designs move into nanometer processes and multi-GHz frequencies.

The WaferIC is a LAIC (Large Area Integrated Circuit). As a LAIC the increase of the power consumption and uIC disposition on the surface of the WaferIC will cause decrease in the wafer performance and the latency. In addition, 50% of the failure in the electronic device is due to the increase of the internal temperature of the chip [12]. However, the WaferIC must be able to support a large temperature differential at its surface [13]. Therefore, in this paper we propose a spatiotemporal signal processing technique for Wafer-Scale IC thermomechanical stress monitoring by an infrared camera. The tech-

nique will be integrated into the WaferIC for the purpose of thermomechanical stress monitoring and management using distributed RO thermal-sensor network.

2. STRUCTURE OF THE WAFERIC™ AND SENSOR INTEGRATION PLAN

As **Figure 1** show, the WaferIC is an 8-inche SI wafer and uses a cell-based architecture design. The surface is divided into 76 reticles which use inter-reticle stitching techniques to ensure connections between them. Each reticle is composed of 32 × 32 unit-cells. All of the cells are a clone (photo-repetition) and each of them contain a part of an internal reconfigurable network for interconnection with neighbouring cells and have a 4 × 4 NanoPads on its surface (top metal layer) [2].

In our previews work [13], we introduced, tested on an FPGA and calibrated a Ring Oscillator (RO) for the purpose of temperature measurement with the GDS (Gradient Direction Sensor) technique. For WaferIC implementation, we propose the use a same RO measurement technique at the cell-level. So one RO composed of 17 sensing inverter will be implemented into each cell, for a total of 77824 RO sensors. For each cell, one sensing inverter will be installed under each NanoPad. And each RO sensor will have its own control circuit imbedded into each cell. So a network of embedded temperature sensors is distributed evenly all over the surface of the WaferIC. This configuration will provide a spatiotemporal working space (*x*,*y*,*t*), which allow the reproduction of high fidelity temperature map of the surface of the waferIC (like an integrated thermal camera), and allows the use of image and video processing techniques for the monitoring and management of the thermomechanical stress at the surface of the WaferIC™.

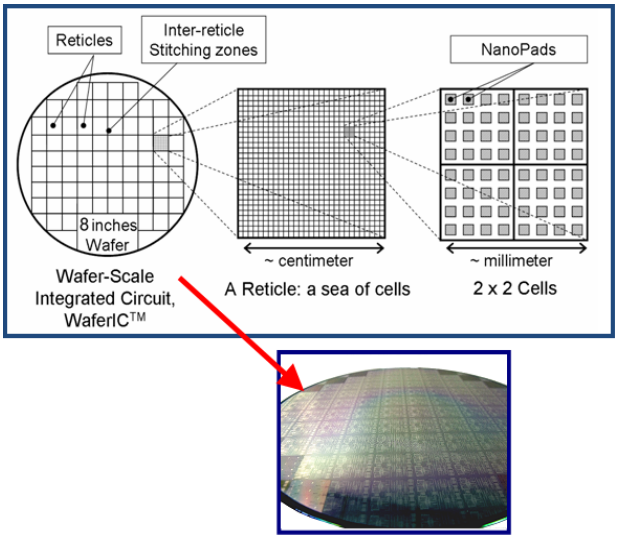


Figure 1. The WaferIC™ architecture.

3. IMAGE PROCESSING AND EXPERIMENTAL RESULTS

In this section, image processing and experiment results on the WaferIC using an Infrared camera (VarioCAM® high resolution inspects 768 from Jenoptik) will be presented. **Figure 2** shows the layout of the experiment, where the IR camera is installed vertically over a dummy WaferIC. The WaferIC is placed on an insulated surface and heated from beneath with a two heat source with a different heat rates. The Camera range is adjusted to measure in 10-bit gray scale (1024 gray-level) temperature between 30˚C and 60˚C for a resolution of 0.117˚C /count. While the WaferIC is heated, a stream of IR pictures has been taken, and 2 of them separated by 60-second apart have been selected to conduct this experiment.

The IR camera has a resolution of 640 × 480 = 307200-Pixel. In order to mimic a spatial workspace produced by an array of 77,824 temperature sensors implemented on a wafer scale integrated circuit, those images has been scaled down. Therefore, a geometric transformation has been used [14].

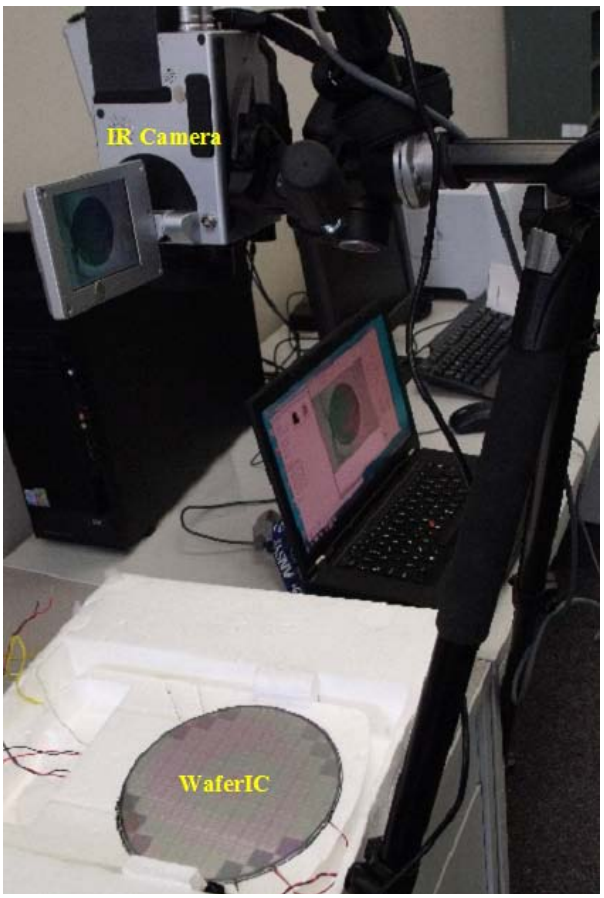


Figure 2. The experiment layout; the IR camera is placed vertically over the WaferIC™, which is heated from beneath by 2 separately controllable heat elements.

$$(x, y) = T\{(v, w)\} \quad (1)$$

where (v, w) are the pixel-coordinates in the original image, (x, y) are the pixel-coordinates of the transformed image, and T is the affine matrix with the following elements,

$$T = \begin{bmatrix} c_x & 0 & 0 \\ 0 & c_y & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

and the scaling equation become,

$$(x, y) = (c_x v, c_y w) \quad (2)$$

With $c_x = (1.98347107438)^{-1}$ and $c_y = (1.98757763975)^{-1}$ we get an array of 242 by 322 or 77924-Pixel. This is the closest as we could get to the aimed value of 77824-pixels. **Figure 3** shows the 3 scaled-down IR pictures used for this experiment.

3.1. Critical Thermomechanical Peaks Identification

For identifying critical thermomechanical peaks stress that could potentially damage the thin layers over the surface of the wafer-scale IC we must identify the surface heat sources that exceed a specific predefined temperature threshold value.

$$D(x, y) = \begin{cases} 0 & if \quad f(x, y) \le T_s \\ 1 & if \quad f(x, y) > T_s \end{cases} \quad (3)$$

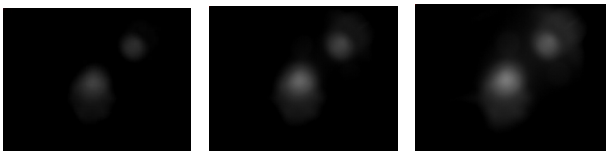
where $D(x, y)$ identify each peak with 1, and T_s is the temperature threshold value. **Figure 4** shows the results of $D(x, y)$ with $T_s = 119$ (maximum value (122) is in picture c). So white dot in **Figure 4(c)**, represent critical temperature values exceeding T_s.

3.2. Temperature Change Velocity

Another important parameter that we tend to measure is the temperature change velocity at each heat source [°C/s].

$$g(x, y, t) = \frac{\partial f(x, y, t)}{\partial t} = f(x, y, t_{n+1}) - f(x, y, t_n) \quad (4)$$

where $g(x, y, t)$ is the temperature change velocity at each sensor.



(a) (b) (c)

Figure 3. IR picture of the WaferIC™ heated from beneath by two heat sources; we can see the evolution of temperature in time over the surface from (a) to (c); pictures are separated by 60-second between.

(a) (b) (c)

Figure 4. Thresholding IR pictures of the WaferIC™ to detect critical hot spots, as we see one spot is detected in (c).

Again $g(x, y, t)$ can be compared to a threshold T_{s1}

$$G(x, y) = \begin{cases} 0 & if \quad g(x, y, t) \le T_{s1} \\ 1 & if \quad g(x, y, t) > T_{s1} \end{cases}$$

where $G(x, y)$ represent only velocities that exceed T_{s1}

Figure 5 shows the resulting of this spatiotemporal operation on pictures from **Figure 3**. As we see, the temperature velocity is stronger at the beginning of the transient mode (picture a).

3.3. Thermal Shock Stress

A thermal shock to the thin layers at the surface of the wafer also needs to be measured and quantified as it can cause a serious damage to the structure if it exceeds a certain limit $L[^\circ\text{C/mm}]$. Thermal shock is closely related to temperature change velocity, but also to maximum temperature gradient value over the surface of the WaferIC. Calculating a spatial gradient can help in evaluating the distribution of temperature over the surface

$$\nabla T = grad(T) = \begin{bmatrix} g_x \\ g_y \end{bmatrix} = \begin{bmatrix} \frac{\partial T}{\partial x} \\ \frac{\partial T}{\partial y} \end{bmatrix}, \quad (5)$$

The direction of the gradient is:

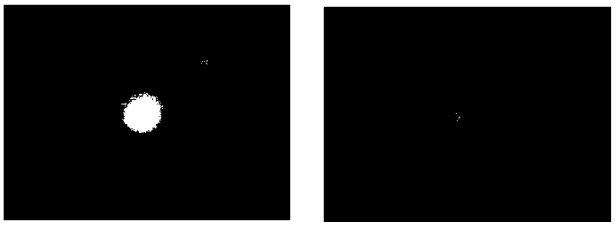
$$\alpha(x, y) = tg^{-1} \begin{bmatrix} g_x \\ g_y \end{bmatrix}, \quad (6)$$

This gradient is perpendicular to the isothermal lines and has a magnitude of

$$M(x, y) = mag(\nabla T) = \sqrt{g_x^2 + g_y^2} \quad (7)$$

To simplify the calculation of the gradient we may need to apply an amplitude thresholding function to the thermal image

$$g(x, y) = \begin{cases} n_0 & if \quad f(x, y) \le T_0 \\ n_1 & if \quad T_0 < f(x, y) \le T1 \\ . & . \\ . & . \\ . & . \\ n_n & if \quad T_{n-m} < f(x, y) \le T_n \end{cases}, \quad (8)$$



(a) (b)

Figure 5. Spatiotemporal derivative of **Figures 3(a)** and **(b)** give (a), then (b); and (c) give (b).

(a) (b) (c)

Figure 6. Isotherm map produced from images of **Figure 3**.

Then applying a median filter to produce homogenous n_n regions

$$m(x, y) = median\{ f(x, y)\} \quad (9)$$

Figure 6, show same images, thresholded with 16 gray-level, 7 × 7 box median filter is applied to generate homogenous regions, then a Laplacien is used (which is an isotropic second order derivative operator) to generate a temperature isotherm map for each picture (from **Figure 3**). The variation of temperature from 30˚C to 60˚C has been quantified into 16 levels (or isotherms). So each level up represents a 1.875˚C temperature increase.

4. CONCLUSIONS

This paper has introduced a methodology to evaluate and predict possible thermal stress in large VLSI circuits using an infrared camera. Important factors contributing to LAIC circuit thermal heating were presented. The proposed monitoring approach can be applied to produce a thermal map of the surface of the WaferIC. Then a spatial and spatiotemporal approach has been presented to extract from successive thermal images a relevant data which will help to prevent thermomechanical stress from damaging the WaferIC.

Results reported in this paper are encouraging and provide a good insight into the issues that will be useful to the process of defining an automated and embedded method for detection and management of thermomechanical stress in LAICs circuit.

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