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Electrical Instability in Pentacene Transistors with Mylar and PMMA/Mylar Gate Dielectrics Transferred by Lamination Process

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Abstract

This study deals with electrical instability under bias stress in pentacene-based transistors with gate dielectrics deposited by a lamination process. Mylar film is laminated onto a polyethylene terephthalate (PET) substrate, on which aluminum (Al) gate is deposited, followed by evaporation of organic semiconductor and gold (Au) source/drain contacts in bottom gate top contact configuration (Device 1). In order to compare the influence of the semiconductor/dielectric interface, a second organic transistor (Device 2) which is different from the Device 1 by the deposition of an intermediate layer of polymethyl methacrylate (PMMA) onto the laminated Mylar dielectric and before evaporating pentacene layer is fabricated. The critical device parameters such as threshold voltage (V_T), subthreshold slope (S), mobility (μ), onset voltage (V_{on}) and I_{on}/I_{off} ratio have been studied. The results showed that the recorded hysteresis depend on the pentacene morphology. Moreover, after bias stress application, the electrical parameters are highly modified for both devices according to the regimes in which the transistors are operating. In ON state regime, Device 1 showed a pronounced threshold voltage shift associated to charge trapping, while keeping the μ, I_{off} current and S minimally affected. Regardless of whether Device 2 exhibited better electrical performances and stability in ON state, we observed a bias stress-induced increase of depletion current and subthreshold slope in subthreshold region, a sign of defect creation. Both devices showed onset voltage shift in opposite direction.

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Keywords

Organic Transistor, Mylar, Lamination, Pentacene, Bias Stress

1. Introduction

Organic semiconductors have enabled the emergence of new exciting research field called organic electronics. This enthusiasm for devices based on organic materials is partly driven by the increased interest in both academic and industry thanks to a low manufacturing cost, mass production, compatibility with flexible substrates compared to their equivalent inorganic materials. Transistor remains unambiguously a key element of electronics devices and is especially present in most new technologies. The considerable development of organic field effect transistors (OFETs)—in which the active layer is organic semiconductor, enables to foresee applications in fields such as flat display driving, radio frequency identification (RFID) tag and sensors [1]-[4].

Many interesting techniques had been used for fabrication of organic transistor devices, and each of them showed advantages and disadvantages. Although organic semiconductor can be processed on flexible substrate they generally do not withstand conventional lithography techniques. This gives rise the development of alternative deposition and patterning methods leading to the concept of soft lithography which is introduced in the end of the 1990s [5] and since highly used. Among these different techniques we could mention soft contact lamination which was applied to organic light emitting diodes [6] and OFETs [7]. Another method such as microcontact printing has been used for patterning organic FETs [8]. Other transfer methods have been reported in the literature as electrode peeling transfer [9] [10] or metal transfer printing [11]. The lamination technique was proposed to transfer an organic semiconductor active layer previously deposited on a donor layer onto a receiver layer acting as the gate insulator [12]. Previous works have shown that Mylar foil can be successfully laminated serving as dielectric [13] and some studies use it both as substrate and dielectric to fabricate transistors [14]-[16].

However, a major drawback of OFETs is the lack of stability making them a critical issue that must be addressed before their commercialization. Hysteresis is an instability that can be frequently observed during device operation. It appears as a difference in the source-drain current values observed during forward and backward scans of the gate or drain voltages. Therefore, minimizing the hysteresis effect is a priority in electronic circuits.

It was also reported that a prolonged polarization of gate electrode named bias stress tends to shift the threshold voltage, degrades the subthreshold parameters [17] reducing the reliability. This complex bias stress phenomenon has been a subject of intense research during several years and remains poorly understood. Under gate bias-stress, the drain current decreases with time due to charge trappings. Several authors considered these traps located at the semiconductor/dielectric interface, or in the gate dielectric, or within the semiconductor active layer [18]-[20]. The bias stress is highly dependent on the involved materials, the device geometry and configuration, the polarization conditions, the gate dielectric and semiconductor deposition temperatures, and the atmosphere in which the device is operating.

In this paper, we report on electrical instabilities in pentacene-based transistors with Mylar and PMMA/Mylar gate dielectrics transferred by a lamination process in ambient environment. Special emphasis is given on comparing the two types of devices in ON state and subthreshold regions under gate bias stress. Device with PMMA/Mylar dielectric exhibited good performances and stability in ON state, while in depletion regime, the subthreshold parameters were degraded. In contrast, the device using only Mylar as dielectric has an opposite behavior. In addition, both devices showed onset voltage shifts in opposite direction.

2. Experimental Details

The substrate was a 175 nm thick PET foil (DuPont Melinex ST 504) thoroughly sonically cleaned. The different transistor fabrication steps are described in **Figure 1(b)**. **Figure 1(a)** is a photograph of transistors realized on PET substrate. Two different types of devices in bottom gate configurations were processed; Device 1 and Device 2. A 70 nm thick Al gate was first deposited by vacuum evaporation and patterned. Then a 900 nm thick Mylar foil (DuPont) was stacked on the patterned substrate and pressed between two hot plates. The quality of the transfer was observed to be strongly relying on both the temperature (in the range of 70˚C - 110˚C) and the pressure. This Mylar is a thin polyethylene terephthalate sheet with dielectric constant close to silicon oxide.

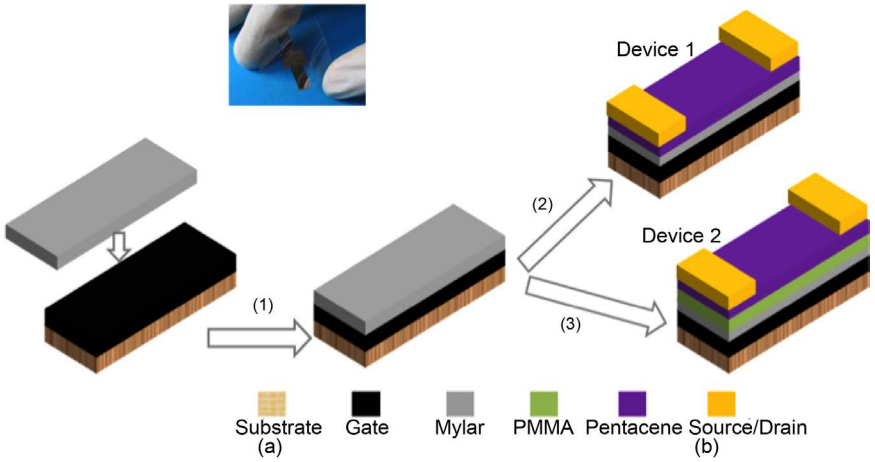

Figure 1. Schematic illustration of Mylar lamination for transistor fabrication: (a) photograph of electrical devices, (b) Pro- cess flow of transistor devices fabricated on a PET substrate, on which Al gate was deposited. (1) Mylar was then pressed; (2) Device 1 obtained after pentacene and source/drain evaporation; (3) PMMA was spun on the top of the laminated Mylar dielectric, Device 2 is completed by evaporating pentacene and source and drain contacts.

After pressure release, a 70 nm pentacene film is evaporated onto the Mylar foil at a substrate temperature and a deposition rate of 70˚C and 0.02 nm/respectively. The device is completed by the deposition of Au source and drain electrodes through a shadow mask. The channel width and length were, respectively, 2 mm and 50 µm. Device 2 is different to Device 1 by spin coating 80 nm thick PMMA layer on the top of the transferred Mylar foil. PMMA was annealed in air for 20 min at 120˚C. Pentacene was then deposited on PMMA followed by the evaporation of top Au source and drain contacts. PMMA is also expected to slightly planarize the Mylar surface and thus lead to a smoother surface. The process flow Mylar lamination for transistors fabrication is represented in **Figure 1**. Current—voltage characteristics were obtained at room temperature in air and in the dark with a probe station and two Keithley 2400 sourcemeter under LABVIEW® environment. The mobility was μ_{sat} extracted from the saturation region of the transfer curves with the equation:

$$I_{D,sat} = \frac{W}{2L}\mu_{sat}C\left(V_G - V_T\right)^2$$

where $I_{D,sat}$ is drain current in the saturation regime; W/L is the width to length ratio; C is the capacitance per unit area; V_G the gate voltage and V_T the threshold voltage.

The morphology of the pentacene thin films was studied in an Amplitude Modulation mode Atomic Force Microscopy (AM-AFM) using the AFM Solver P-7, "stand alone" Smena-B (NT-MDT, Russia), with typical spring constant k of 22 N/m and tip radius of 10 nm. This mode was shown to be more appropriate than the contact mode to image soft materials such as polymers, functionalized surface and biological objects, in air.

3. Results and Discussion

3.1. Electrical Characterization and Pentacene Morphology

Bottom-Gate/Top-Contact (BG/TC) thin-film transistors were fabricated as described in the experimental part. All measurements were performed in air at room temperature and in the dark. For all two devices, the organic transistors operate in the accumulation mode since the gate electrode is biased negatively with respect to the grounded source electrode. Drain current (I_D) is almost linear with drain voltage at low V_D, whereas it tends to saturate at higher drain voltage due to the pinch off of the accumulation layer. **Figure 2(a)** and **Figure 2(b)** show typical output characteristics curves of Device 1 and Device 2 with well-defined linear and saturation regimes.

To study the electrical instability related to hysteresis, we performed electrical measurements in forward and back scans. As we can see, Device 1 exhibits a hysteresis in forward and reverse characteristics (**Figure 2(a)**) while for Device 2 no hysteresis is recorded. The Mylar film is a low-k (dielectric constant) polymer dielectric—with k = 3.25 at 1 kHz and the molecular structure shows that it is non-polar—the observed hysteresis could be attributed to: 1) impurities present in the semiconductor or at the dielectric interface, such as water

molecules diffusing through grain boundaries [21] (small grains of pentacene were observed during the growth on Mylar) or 2) structural defects initially present on the Mylar surface. Indeed, when Mylar foil was pressed on the aluminum gate, the mechanical stress made the surface rougher. These structural defects and a rough surface constitute a prosperous environment for charge trapping. Drain current in forward is higher than in reverse for the same gate voltage, a sign of hole trapping. The lack of hysteresis observed for Device 2 confirms a good interface between PMMA and pentacene as observed by several authors [22] [23]. The electrical performance parameters are summarized in **Table 1**. A key parameter that assesses the interface quality is the subthreshold slope (S); it is extracted from the transfer characteristic in logarithmic scale in saturation regime. The values are 19 V/decade and 8 V/decade respectively for Device 1 and Device 2. The highest S value is attributed to the device with Mylar dielectric, which is a confirmation of poor interface. Threshold voltage, I_{on}/I_{off} ratio and mobility are −25 V, 1.3×10^2 and 4.1×10^{-3} $cm^2 \cdot V^{-1} \cdot s^{-1}$ respectively for Device 1 while Device 2 exhibited −20 V, 5×10^3 and 5.1×10^{-2} $cm^2 \cdot V^{-1} \cdot s^{-1}$ respectively for the threshold voltage, I_{on}/I_{off} ratio and mobility.

To better understand this difference, AFM images were performed in order to identify the morphology of pentacene layer that can explain the relation between they nanostructures and the charges carriers mobility.

Figure 3(a) gave AFM image of pentacene on Mylar with a surface roughness about 17 nm and peak-to-valley value up to 200 nm, we also observe small grain sizes (200 - 350 nm) with low connectivity, as consequence,

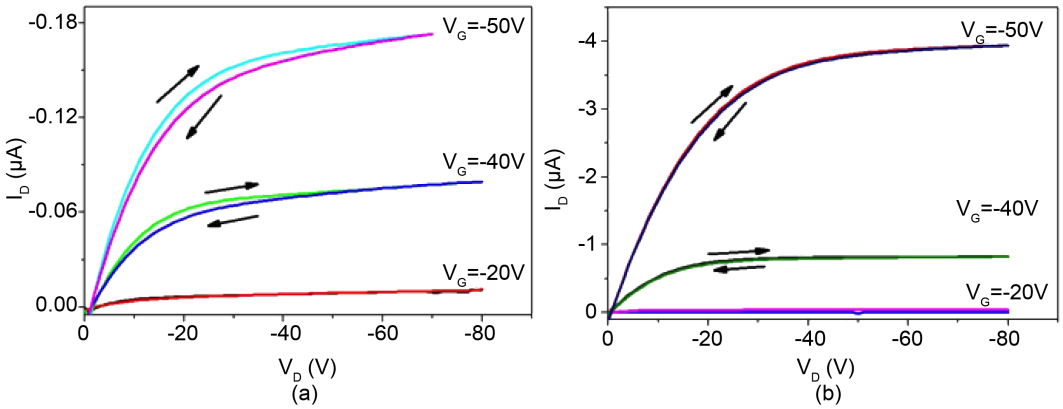

Figure 2. Forward and reverse output characteristics of transistor devices using: (a) Mylar and (b) PMMA/Mylar as dielectrics at different gate voltages.

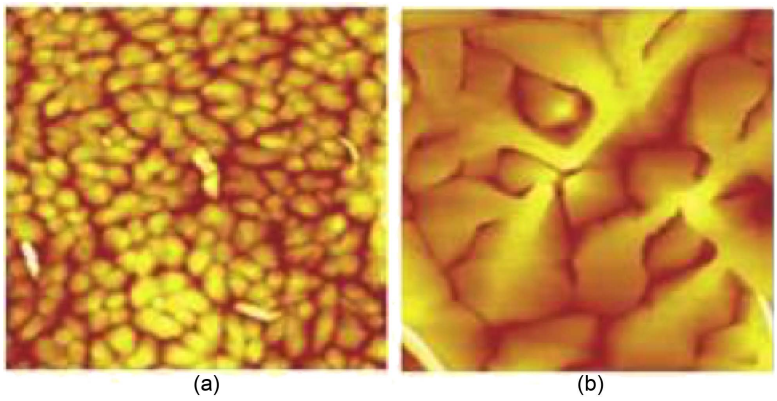

Figure 3. AFM images (4 × 4 μm²) of 70 nm of pentacene film evaporated on (a) Mylar and (b) PMMA/Mylar.

Table 1. Summary of the electrical parameters of Device 1 and 2 before bias stress.

Devices	V_T (V)	μ ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	I_{on}/I_{off}	S (V/decade)
Device 1	−25	4.1×10^{-3}	1.3×10^2	19
Device 2	−20	5.3×10^{-2}	5×10^3	8

the combination of these two effects leads to electrical parameters degradation [24] [25] such as mobility, threshold voltage and I_{on}/I_{off} ratio. It has been reported that, the diffusion of impurities such as polar water molecules into grain boundaries changes the intermolecular interactions in those regions, increasing energy barrier for charge carrier intergrain transport or ions associated with water screen the electric field at the channel and lower the concentration of gate-induced mobile carriers [26]. All of the mechanisms would lead to reduce the performances of Device 1.

In contrast, thanks to the PMMA layer, Device 2 exhibits improved performances. **Figure 3(b)** showed large dendritic grain size (2 - 5 µm) with surface roughness of PMMA/Mylar around 12 nm. The largest grain sizes allow reducing the number of grain boundaries acting as charge traps during the transport. Since the carrier mobility is very sensitive to the molecular ordering of the pentacene and the carrier trapping at grain boundaries, the large grain sizes of pentacene on PMMA give rise to high field-effect mobility [25]. These results clearly point out the highly beneficial PMMA layer on the transport properties in the pentacene channel throughout the ON state regime and as long as bias stress was not applied.

3.2. Bias Stress Effect

To study the bias stress-induced degradation in transistor devices, a constant gate voltage was applied to the organic transistors. To determine the changes in the transfer curves, the applied gate voltage is interrupted at short time intervals by a sweep of the gate. This technique allowed us to obtain the electrical parameters. **Figure 4(a)** shows the square root of transfer characteristics before and after different stress times for Device 1. We observe that the applied stress shifts the transfer characteristics in the negative gate voltage direction (with $\Delta V_T = -10$ V) and the shape does not appreciably change with stress time. From the plot, it is clear that the slope of the linear

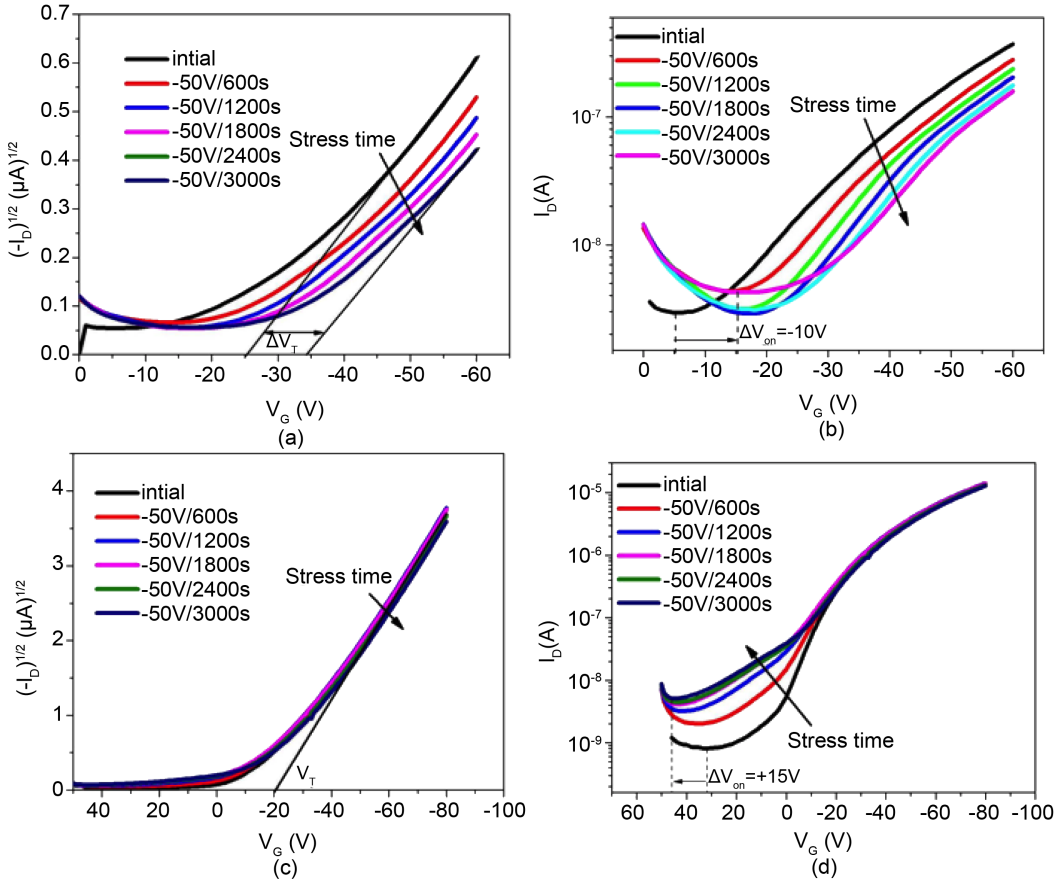

Figure 4. Transfer characteristics of Device 1 and Device 2 before and after bias stress for 3000 s. −50 V was applied on the gate voltage (a) square root for Device 1, (b) logarithmic scale for Device 1, (c) square root for Device 2, (d) logarithmic scale for Device 2. The curves are obtained in saturation regime at $V_D = -70$ V.

part of the curve, which is proportional to the field effect mobility in the saturation regime, is similar for all curves. The extracted mobility remains minimally affected after the application of gate bias stress (−50 V/3000 s).

The negative threshold voltage shift associated to negative gate bias is a consequence of holes being trapped. **Figure 4(b)** is the transfer characteristics in logarithmic scale of Device 1 before and after the bias stress, all curves have a similar shape. It is worth noting that the subthreshold slope of the device does not change even after the device has undergone bias stressing. This indicates that no additional interface states are created at the channel/dielectric interface after the device was stressed; however, a slight increase of I_{off} current was recorded with noticeable onset voltage shift.

Regarding the transistor with PMMA/Mylar as dielectric, both mobility and threshold voltage remain unchanged after negative bias stress of −50 V for 3000 s as it was operating in ON state (**Figure 4(c)**). A clear difference appears between the device using Mylar as dielectric and that with PMMA/Mylar under bias stress in ON state.

The grain boundaries play a crucial role in the bias stress effect [26] [27], and it was shown that in pentacene-based OTFTs the charge trapping was found to occur preferentially in intergrain regions of organic thin film [28]. One plausible explanation results from the difference of morphologies as observed by AFM images. Pentacene morphology on Mylar being less ordered with small grain size, leads to increase the amount of grain boundaries.

These latter are synonyms of traps, a prolonged polarization of the gate electrode permanently creates a constant electric field, which promotes a continuous charge trapping. However, the large grain sizes (less grain boundaries) on PMMA/Mylar reduce the number of traps, accordingly, the charge trappings decrease.

Figure 4(d) is the transfer characteristics of Device 2 in logarithmic scale after several stresses. As long as bias stress was applied, the electrical parameters in subthreshold region were degraded. As can be seen, I_{off} current increases nearly by one order of magnitude and the S is increased from 8 V/decade to 20 V/decade (while for Device 1, S remains unchanged with a slight increase of I_{off} current). The degradation of subthreshold slope as well as the subthreshold current increase can be explained by interface state creation. The I_{off} current increase cannot be attributed to the gate leakage as it was enough thick in both Device 1 and Device 2; moreover all devices were characterized in air with constant humidity rate. These different behaviors observed in subthreshold region for both devices might be the bias-assisted moisture/oxygen diffusion [17]. The combination of moisture and bias stress leads to increase the depletion current and the subthreshold slope; this is exactly what we observe in **Figure 4(d)**.

Another key parameter that must be addressed is the onset voltage V_{on} which is critically influenced by the semiconductor/dielectric interface. The onset voltage is determined as the minimum of the drain courant versus gate voltage in logarithmic scale and it is highly desirable to get a near-zero V_{on} in circuitry. After bias stress the onset voltage of Device 2 is shifted towards positive gate values with $\Delta V_{on} = +15$ V, while for Device 1 it is negatively shifted and $\Delta V_{on} = -10$ V after 3000 s under bias stress, showing an opposite behavior. The onset voltage shift of Device 1 is exactly similar to the threshold voltage shift $\Delta V_{on} = \Delta V_T = -10$ V. According to Knipp *et al.* [29], the threshold voltage shift could be attributed to donor states. Water molecules were shown to be localized between pentacene molecules and create trap states in the band gap [30], and the orientation of water dipoles changes the local polarization of the pentacene monolayers, creating trap states in the band gap [31]. In contrast, Oxygen is known to create deep acceptor levels and to increase the residual doping level of the organic semiconductor, both contributing to a positive shift of the onset voltage [32] [33], this may explain what we observed in Device 2.

4. Conclusion

Electrical performances and instabilities of transistors based on pentacene semiconductor with laminated Mylar and PMMA/Mylar dielectrics have been studied. Hysteresis has been observed with the device using only Mylar as dielectric. In contrast, no hysteresis has been recorded for the device using PMMA/Mylar double layer. Hysteresis apparition was related to the pentacene grain sizes; the large gain of pentacene obtained with PMMA prevent any moisture diffusion compared to pentacene growth on Mylar showing small grain sizes and more grain boundaries. These latter are considered as an ideal environment for charge trapping. Negative bias stress performed in ambient air leads to electrical parameters degradation depending on operating regimes. In ON state the transistor with Mylar exhibited a high threshold voltage shift with a minimal change of mobility and I_{on}/I_{off} ratio after bias stress. However, the transistor using PMMA/Mylar showed good electrical performances in ON

state but in subthreshold regime, the depletion current increased as well as the subthreshold swing due to the doping and bias-assisted moisture/oxygen diffusion leading to defect creation. Both devices showed onset voltage shift in opposite direction. Mylar lamination is a powerful technique for transistor fabrication whether in bottom or top gate configurations for mass fabrication in ambient environment. Our research is in progress to optimize the electrical parameters especially by improving the dielectric lamination and to understand the complex bias stress phenomenon that remains so far poorly understood in order to minimize the transistor instability.

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