

FPGA Implementation of Predictive Hysteresis Current Control for Grid Connected VSI

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ABSTRACT

Grid connected voltage source inverters (VSIs) are essential for the integration of the distributed energy resources. Hysteresis current control (HCC) is a commonly employed method for power control of VSIs. This control method, in contrast with voltage control, provides good dynamics, good stability and implicit over current protection. However, the most important concern of digital implementation of HCC is related with the sampling period of the measured currents. This paper presents a predictive hysteresis current control (HCC) for grid connected voltage source inverter and its FPGA implementation. Simulation and experimental results are provided to verify the validity of the proposed implementation.

KEYWORDS

Distributed Generation (DG); Interconnected Power Systems; Hysteresis Current Control (HCC); Field Programmable Gate Array (FPGA)

1. Introduction

Modern power systems, looking forward to the Smart Grid concept, involve more and more the integration of the Distributed Energy Resources (DER) mainly based on clean energy sources like wind power (WP) and photovoltaic (PV). The integration of these renewable resources to the utility grid becomes essential to improve the reliability and the capability of power systems. In this sense, the green house emissions can be greatly reduced. Voltage source inverters (VSIs) are power electronics circuits widely used to interface the DER with the utility power system.

In general, Grid connected VSIs are normally operated by controlling its output power, and, two possible control schemes can be implemented, either voltage or current control. For the voltage control, the phase angle and amplitude of the output voltage are controlled according to the desired output power while on the current case; the current injected by the inverter is directly controlled to produce the desired output power. Hysteresis Current Control (HCC) was originally implemented as an analog controller and it is often used for grid connected inverters configuration considering its fast transient response, good accuracy, implementation simplicity and inherently over-current protection [1-9].

Classic HCC has two main disadvantages, first the variable switching frequency depending on the load characteristics; and second, the degradation of its accuracy when all digital implementations are required. Several modifications to the classic method have been introduced trying to overcome those problems [4-9]; most of the proposed methods seek for a constant switching frequency offering better performance than classic method. Most of the modified strategies of HCC offer better performances than the classic one when they are implemented using analog logic circuitry. However, when their implementation is made in digital processors like the field programmable gate arrays (FPGAs), without external analog logic, the mean switching frequency is limited by the sampling rate of the analog-to-digital converters (ADCs).

This work presents a predictive hysteresis current con-

trol taking into account the lately increase of FPGAs deployment in real-time measurement and control applications. The HCC method introduced in this paper takes advantage of the real-time estimation of the utility voltage by means of the hardware implemented VF-ADALINE with FLL [10,11]. The estimated signal of the utility voltage is employed to predict with high accuracy the output current of VSI within the sampling period of the measurement system with a higher sampling rate which is defined by the implemented structure of the VF-ADALINE.

The resulting oversampled signal of the VSI output current can then be used to implement, in an FPGA device, the classic or modified HCC strategies with similar performances than the analog implementations.

Simulation and experimental results are presented showing a good accuracy of the all digital implementation of HCC proposed. This predictive HCC has been validated by using a Xilinx FPGA as the digital target and a single phase grid connected VSI as the power electronics application.

2. Hysteresis Current Control

The **Figure 1** shows a simplified circuit diagram of single phase grid connected VSI.

The filter inductor (L_D) voltage can be written as function of the output current using

$$V_L = L_D \frac{\mathrm{d}i_L}{\mathrm{d}t} \square \tag{1}$$

Then, the output current of the VSI can be computed if the inductor voltage (V_L) information is available

$$i_L = \frac{1}{L_D} \int_0^{T_L} V_L \cdot dt \, \Box$$
 (2)

$$i_{L} = \frac{V_{L}}{L_{D}} t \Big|_{0}^{T_{1}} + I_{0}$$
(3)

In the case of grid-connected inverter, the inductor voltage depends on the voltage imposed by the controller $(v_{DC}(t))$ and by the grid voltage $(v_{PCC}(t))$. Using a full bridge single phase inverter with two conduction states



Figure 1. Simplified diagram of a single phase grid connected VSI.

(s1s4 and s2s3), the V_{DC} can be defined by

$$v_{DC}(t) = \begin{cases} +V_{DC} & \text{if } s1s4 \\ -V_{DC} & \text{if } s2s3 \end{cases}$$
(4)

The fundamental grid voltage will be

$$v_{PCC}(t) = V_{PCC} \sin(\omega t) \tag{5}$$

where $\omega = 2 \pi f$ is the fundamental frequency of grid voltage

The inductor voltage when S_1 and S_4 are ON and S_2 and S_3 are OFF can be defined by

$$v_L(t) = V_{DC} - V_{PCC} \sin(\omega t) \tag{6}$$

If the S_1S_4 switching period is delimited by the $T_{14_{ON}}$ and $T_{14_{OFF}}$ instants. The inductor current at the end of the switching period (at $T_{14_{OFF}}$) can be obtained by using

$$i_{L}(T_{14_{OFF}}) = \frac{1}{L_{D}} \int_{T_{0}}^{T_{14_{OFF}}} v_{L}(t) \cdot dt$$
(7)

$$i_{L}\left(T_{1_{4_{OFF}}}\right) = \frac{V_{DC}}{L_{D}}\left(T_{1_{4_{OFF}}} - T_{0}\right)$$

$$+ \frac{V_{PCC}}{\omega L_{D}}\left[\cos\left(\omega T_{1_{4_{OFF}}}\right) - \cos\left(\omega T_{0}\right)\right] + i_{T_{0}}$$
(8)

In the same way, if S_2 and S_3 are ON, the expression of the inductor current at the end of the switching period (at $T_{23_{OFF}}$) can be written as

$$i_{L}(T_{23_{OFF}}) = -\frac{V_{DC}}{L_{D}}(T_{23_{OFF}} - T_{0}) + \frac{V_{PCC}}{\omega L_{D}} \Big[\cos(\omega T_{23_{OFF}}) - \cos(\omega T_{0}) \Big] + i_{T_{0}}$$
(9)

If all switches are OFF, the inductor current at the T_R instant ($T_R > T_0$) can be defined as

$$i_{L}(T_{R}) = \frac{V_{PCC}}{\omega L} \Big[\cos(\omega T_{R}) - \cos(\omega T_{0}) \Big] + i_{T_{0}} \quad (10)$$

Considering an ideal sampling period ($T_s \ll 1 \ \mu s$) the switching frequency depends on the grid and DC voltages, on the hysteresis band and on the filter inductor. Under this condition, the output current always remains within the hysteresis band (h).

Figure 2 shows the evolution of the instantaneous switching frequency during an electric period of 120 V/60 Hz grid voltage using different filter inductance (from 8 to 20 mH). The DC voltage is considered constant and set to 200 V. Figure 2(a)) shows the results for a hysteresis band fixed to 0.25 A and Figure 2(b) is fixed to 0.35 A.

When the sampling period is around a few microseconds or tenths of microseconds the current control error increases as the sampling period increases.

Figure 3 shows the evolution of the exceeding current



Figure 2. Effect of the filter inductance on the instantaneous switching frequency during an electric period of 12 V/60 Hz grid voltage, a) hysteresis band = 0.25 A and b) hysteresis band = 0.35 A. DC voltage V_{DC} = 200 V. Case of ideal sampling period.

tracking error, during a half electric cycle (8.33 ms), considering different filter inductor and different sampling period. Here, the exceeding current tracking error is computed by using

$$e_{CT}(k) = \frac{|i_{L}(k) - i_{LREF}(k)|}{h} - 1$$
(11)

where iL_{REF} is the desired current and *h* is the hysteresis band. e_{CT} represents the exceeding error compared to the one obtained by using an ideal sampling period.

According to these results, the maximum current error can be very important when a low inductance (filter inductor) and a long sampling period are employed ($T_s > 10 \ \mu s$) two or three times the hysteresis band. It is also to remark that even with a large inductor (see Figures 3(b) and (c)), an exceeding error greater than 0.5 p.u may appears because the sampling and the ideal switching instants do not match.

3. Proposed Hysteresis Current Control

Taking into account that the main drawbacks of a digital







Figure 3. Effect of the filter inductance on the instantaneous current tracking error during a half electric period of 120 V/60 Hz grid voltage. Sampling period a) 5 μ s b) 10 μ s and b) 20 μ s. DC voltage $V_{DC} = 200$ V, hysteresis band = 0.25 A.

implementation of HCC are related with the frequency jitter and the random tracking error which highly depends on the sampling frequency of measurement system, the proposed implementation seeks to solve this problem.

The proposed method uses the oversampled estimation of the utility voltage by means of the variable frequency ADALINE with frequency locked loop (VF-ADALINE & FLL). In fact, the VF-ADALINE&FLL runs at a sampling rate imposed by the direct digital synthesis module VF-DDS (T_{DDS}) which is higher than the one of the ADCs (T_s). Figure 4 shows a simplified diagram of the VF-ADALINE with FLL as proposed in [11].

It is important to highlight that the estimation of the voltage signal is made by adjusting, online, the frequency of the VF-DDS, this feature warrants a very high accuracy of the online utility voltage tracking.

The estimated signal of voltage $(v_{PCC-E}(k))$ is then employed to predict the output current of the inverter by using

$$i_{L-E}(k) = \begin{cases} i_{L-M}(k) & \text{if } \uparrow T_{S} \\ i_{L-E}(k-1) + m(k) \cdot T_{DDS} & \text{if } \uparrow T_{DDS} \end{cases}$$
(12)

where the –E subscript correspond to the estimated signals and the–M ones to the measured signals; $\uparrow T_S$ is the rising edge of the clock signal of the measurement system (ADC clock); $\uparrow T_{DDS}$ is the rising edge of the clock signal of the VF-ADALINE which is also employed as a clock signal for the current controller; and m(k) is the current slope which is defined by

$$m(k) = \begin{cases} \frac{v_{DC}(k) - v_{PCC-E}(k)}{L_D} & \text{if } S_{14} \\ \frac{-v_{DC}(k) - v_{PCC-E}(k)}{L_D} & \text{if } S_{23} \\ \frac{-v_{PCC-E}(k)}{L_D} & \text{Otherwise} \end{cases}$$
(13)

where $v_{DC}(k)$ is the DC voltage of the inverter, and L_D is the filter inductor which are known values. S_{14} and S_{23} signals correspond to the gating pulses ON state.

As shown in **Figure 5**, the proposed current control scheme takes into account the effect of the dead time added to the gating signals and as illustrated, h is considered as an input signal. The proposed control scheme can be used with fixed or with variable hysteresis band.

4. Hardware in the Loop Co-Simulation

The Figures 4 and 5 schemes have been implemented for



Figure 4. Simplified diagram of VF-ADALINE with FLL for real-time signal estimation [11]. f_{Vpcc-E} : Estimated frequency.



Figure 5. Simplified diagram of of the proposed current control scheme.

the Xilinx Virtex-II-Pro (xc2vp30-7ff896) FPGA by using System Generator and MATLAB/Simulink. Also a single phase grid connected VSI has been implemented in order to simulate the behavior of the proposed method and compare it to the classic method.

Further, some hardware-in-the-loop (HIL) co-simulations have been carried out as a preliminary validation of the proposed scheme. For these tests, the controller runs step-by-step in the FPGA and the model of the electric system (model of measurement, power electronics, utility source, etc.) runs on the MATLAB/Simulink. The main characteristics of the system are presented in Appendix.

Figure 6 shows a comparison, during 3 ms, of the cosimulation results of the classic HCC and the proposed predictive HCC. In this case, the filter inductance is L_D = 12 mH, the voltage and current signals are sampled with T_S = 10 µs and the VF-ADALINE works at T_{DDS} = 1 µs. It is evident the improvement of the current tracking with the predictive method which keeps the current tracking error inside the defined hysteresis band.

Several simulations have been carried out using different filter inductances, and then the total harmonic distortion (THD) of the VSI current has been computed for each case. The results are summarized in **Table 1**, showing the advantage of the proposed control scheme as the current THD is improved.

It is important to highlight that a large filter inductor permits a low current distortion (THD < 6%) using the classic HCC. IEEE standards recommend that the harmonic current injection at the point of common coupling of the distributed energy resources with utility must be under 5% [12]. On the other hand, it is well known that a large filter inductor limits the dynamics of VSI and the maximum output power of VSI [13].

5. Experimental Results

In order to evaluate the predictive current control method, the power control scheme proposed in [10] has been



Figure 6. Comparison of the co-simulation results of the current tracking of grid connected VSI using a) classic HCC and b) predictive HCC. Utility voltage is 120 V/60 Hz, Sampling period $T_S = 10 \ \mu$ s, DC voltage $V_{DC} = 195 \ V$, $h = 0.3 \ A$.

 Table 1. Total harmonic distortion of VSI output current

 when the hysteresis band is fixed to 0.3A and the output

 power is set to 500 W.

Filter Inductance (mH)	THD (%)	
	Classic HCC	Proposed HCC
8	6.6	3.5
10	6.0	4.5
12	6.1	4.0
14	5.5	3.7
16	5.3	3.7
18	5.2	4.1
20	5.1	3.8

modified including the proposed current predictor and the VF-ADALINE with FLL [11]. Then, the resulting power control scheme has been implemented in a Xilinx xc2vp30-7ff896 FPGA device.

The power control scheme has been implemented considering both the classic and the proposed hysteresis current controllers in order to compare them.

Several tests have been carried out using a single phase

grid connected VSI with the same characteristics used in simulation (see Appendix). The J-TAG link of the Xilinx development system has been employed (programmed) to send the information of the measured and the reference currents and the measured voltage to the MATLAB/ Simulink user interface as proposed in [10]. The output buffers have been programmed to send the information of each wave with a sampling period of 10 μ s. Then, the results are post-processed to plot the corresponding figures.

Figure 7 shows the comparison of the experimental results of current tracking by using the classic and the predictive HCC methods. In this tests, the nominal utility voltage is 120 V/60 Hz, the sampling period is $T_s = 10 \,\mu$ s, the DC link voltage is 195 V, the hysteresis band is fixed at h = 0.3 A, and the output power of the VSI is set to 500 W. One cycle of the measured utility voltage is plotted in **Figure 8**.

The trajectories when the classic method is employed are presented in Figures 7(a) and (b) shows the results with the predictive method.



Figure 7. Comparison of current waves obtained experimentally by using a) the classic and b) the predictive HCC methods with fixed hysteresis band (h = 0.3 A).



Figure 8. One cycle of the measured utility voltage.

It is evident that the current tracking is better achieved when the predictive method is employed, and as expected the classic HCC allows a higher error in the current tracking compared to the predictive method (zoomed zones of Figure 7(a)). This behavior is not suitable because produces low frequency components in the output current which are difficult to filter and can also produce resonance if LC or LCL filters are employed.

Figure 9 shows the current waves obtained experimentally by means of a digital oscilloscope; Figure 9(a) shows the results with the classic HCC and Figure 9(b) the results with the predictive method. The spectrum of these current waves have been obtained and plotted in Figure 10. The two spectrum plots have been superposed in the same figure.

These experimental results confirm the expected and simulated behavior of predictive HCC; in fact the current spectrums show that the low frequency components are better attenuated with the predictive method. The spectral distribution, which is highly spread in the classic HCC, shows a dominant high frequency in the predictive method like in a constant switching frequency PWM.

It is important to remark that in the experimental tests carried out in this work, the DC link voltage has not been measured and it is supposed to be constant during the test. This assumption is done in order to compare the two control schemes in similar hardware conditions. It is then expected that better results could be obtained if the V_{DC} measure is introduced in the predictive HCC controller.

6. Conclusions

This paper proposes a new predictive hysteresis current control scheme for grid connected VSI and its hardware implementation using FPGA.

This new approach is based on the oversampled estimation of the utility voltage by means of the variable frequency ADALINE with frequency locked loop (VF-ADALINE & FLL) and the prediction of the VSI output current within a sampling period of the measured signal with a higher sampling rate. The predicted current is used



Figure 9. Comparison of current waves obtained experimentally by using a) classic and b) predictive HCC methods with fixed hysteresis band (h = 0.3 A). Measurement conversion ratio 5 A/V.



Figure 10. Comparison of current spectrum obtained experimentally by using classic and predictive HCC methods with fixed hysteresis band (h = 0.3 A).

to generate the gating pulses of VSI instead of the measured signal, which is employed as protection and to adjust the predictor online.

Some advantages of the proposed scheme are the inherent over current protection, the possibility of all digital implementation without external circuitry, the possibility of fixed or variable hysteresis band operation in order to control the mean switching frequency.

The proposed scheme has been validated by simulation and by experiments using a single phase grid connected VSI and Xilinx FPGA device for the control implementation.

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Appendix

1) Simulation and experimental setup parameters

AC Power Source: 120 VAC/60 Hz. Measurement system: Sampling period: $T_s = 10 \ \mu s$, Resolution = 12 bits FPGA system: Main clock period: $T_{FPGA} = 10 \ ns$ Multipliers input/output resolution 18 bits/35 bits VF-ADALINE and FLL: $T_{DDS} = 1 \ \mu s$. Single-Phase Full-Bridge Inverters," *IET Power Electronics*, Vol.2, No.5, 2009, pp. 585-594. http://dx.doi.org/10.1049/iet-pel.2008.0143

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Learning factor = 0.1 Harmonics order = 32 ROM sine table length: $2^{P} = 215$ Fundamental frequency: $f_{0} = 60$ Hz FLL gain = 3 FLL updating period = 10 µs **2) Power electronics converter** Voltage Source Inverter: 16A, 600V IGBT full bridge (IRAMX16UP60A) Filter inductor and capacitor: $L_{D} = 12$ mH, $C_{0} = 2$ µF. DC source voltage: $V_{DC} = 195$ V.