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Research on the Topology and Control Scheme of an Innovative Modular Multilevel Converter*

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ABSTRACT

This paper presents a new modular multilevel converter (MMC) topology. Compared to conventional multilevel converters, MMC has much lower switching frequency (50 Hz) resulting in lower switching losses, and consequently, lower total losses of the transmission system. The fundamental concept and the applied control scheme are introduced in detail. A modified multilevel fundamental switching modulation scheme adopting the multicarrier pulse width modulation concept is presented. A capacitor voltage balancing technique is proposed. With the established simulation model of the 11-level MMC, the modulation and balancing strategy presented are confirmed by MATLAB/SIMULINK simulations. The multicarrier pulse width modulation converter strategy enhances the fundamental output voltage and reduces total harmonic distortion. This new type of converter is suitable for high-voltage drive systems and power system applications such as high voltage dc (HVDC) transmission, reactive power compensation equipment and so on.

Keywords: Sub-Modular; Modular Multilevel Converter; Fundamental Switching Modulation; Topology; CAPACITOR Voltage Balancing

1. Introduction

Nowadays, multilevel converter is an emerging and highly attractive topology for medium-voltage (MV) and high-voltage applications [1,2]. There are three major multilevel converter topologies [3]: 1) the neutral-point-clamped converter (NPC), 2) flying capacitor converter (FC), and 3) cascaded H-bridge converter (CHB). The three-level NPC is probably the most widely used topology for medium-voltage AC motor drives and PWM active rectifiers. The NPC suffers from the problem of voltage imbalance of the dc link capacitors; this problem increases complexity with an increasing number of levels. The FC also consists of a series connection of identical commutation cells-the number of voltage levels in the line-to-line voltage depends on the number of commutation cells. One particular challenge is balancing the capacitor voltages, which is accomplished by the choice of the converter switching states. The main drawback is the fact that CHB needs an isolated dc-source, usually provided by a three-phase rectifier fed by a transformer. Hence, for a three-phase five-level inverter, a three-phase transformer with six secondary three-phase windings and the corresponding diode bridges are necessary, increasing the volume and cost of the converter.

To solve the aforementioned problems, a modular multilevel converter (MMC) topology has been proposed [4,5]. The MMC features the following advantages: 1) distributed location of capacitive energy storages; 2) modular construction; 3) simple voltage scaling by a series connection of cells;4) Lower switching frequencies (50 Hz) make the overall converter losses closer to the thyristor technology. Due to its interesting characteristics, the MMC topology is very attractive for high-voltage dc transmission and MV converters.

This paper presents a MMC topology. The fundamental concept and the applied control scheme are introduced. A modified multilevel fundamental switching modulation scheme adopting the multicarrier pulse width modulation concept is presented. A capacitor voltage balancing technique is proposed. Finally, simulation model of the 11-level MMC is established. The modulation and balancing strategy presented are confirmed by MATLAB/SIMULINK simulations. The multicarrier pulse width modulation converter strategy enhances the fundamental output voltage and reduces total harmonic distortion. This new type of converter is suitable for high-voltage drive systems and power system applications such as high voltage dc (HVDC) transmission, reactive power compensation equipment and so on.

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2. The Modular Multilevel Converter

2.1. Topology of MMC

A basic structure of a MMC is shown in **Figure 1**. MMC is composed of many series-connected sub-modules (SMs) and the primary function of SMs provides many separate DC sources for synthesizing the desired voltage. The number of output voltage levels in MMC is N+1, where N is the number of SMs in per upper or lower arm of a single phase. Seen from the AC side, all SMs of a single phase are connected in series. So its AC output voltage is the sum of all SMs' output. By switching SMs in the upper and lower arm, the voltage U_{dc} is adjusted. In a similar manner, the voltage U_{jo} (j=a, b, c) can be adjusted to a desired value if U_{dc} is fix. No additional external connection or energy transmission to the SMs is needed, for full 4-quadrant operation of the converter system.

The arm inductor is in series with the distributed energy storage capacitors, so the effects of faults arising inside or outside the converter can be reduced substantially by the arm inductor such as a short circuit between the DC terminals of the converter. These faults are swiftly detected, and due to the low current rise rates, the switching devices can be turned off at absolutely uncritical current levels. Consequently, this feature provides very effective and reliable protection of the system. In addition, the three-phase modules of the converter are connected in parallel at the DC side. Since the three generated DC voltages of the phase modules cannot be exactly equal, balancing currents occur between the individual phase units. The converter reactors damp these balancing currents to a very low level and make them controllable.

2.2. Basic Operating Principle of SM

A suitable and simple realization of the SM is given in **Figure 2**. The interface of the SM is composed solely of two electrical terminals and one bi-directional fiber-optic interface. **Table 1** summarises the switch states of a cell and their resultant influence on associated capacitor voltages. When the switching device S_m is on and S_c is off, output voltage V_O=0; when the switching device S_m is off and S_c is on, voltage V_O=V_{dc}.

No V_O=-V_{dc} is possible. Output voltage of SM is unipolar. By switching a number of the N SMs in the upper and lower arm, the voltages in each arm can be synthesized. So the voltage U_{dc} and voltages U_{jo} (j=a, b, c) can be adjusted independently.

Figure 3 illustrates single phase topology diagram of a MMC. Assuming the capacitor voltage is V_{dc}, output voltage of each SM can take on one of two different voltage levels. With S_c on state, it is equal to V_{dc}, and when S_m is on, is zero. Therefore, it is possible to selectively and separately control each of the individual SMs to provide a voltage which is either V_{dc} or zero. The switches of the SMs are operated so that the individual voltages from each SM add up to form a multilevel, near-sinusoidal stepped waveform at the converter terminals. The number of output voltage levels in MMC is N+1, where N is the number of SMs in per upper or lower arm of a single phase. The number of capacitors in charging and discharging state is N. The number of S_c in the on state in the upper and lower arm is M and L. Then the following equations can be obtained.

$$M+L=N \tag{1}$$

In the upper arm, the number is M of the switching device S_c and S_m in on and off state; in the lower arm, the number is M of the switching device S_m and S_c in off and on state. Then, control state of the SMs in the upper and lower arm is fully symmetrical, i.e., control scheme of the SMs in the upper and lower arm is the same. The relationship among the dc-link voltage U_{dc} and the capacitor voltage V_{dc} is given by

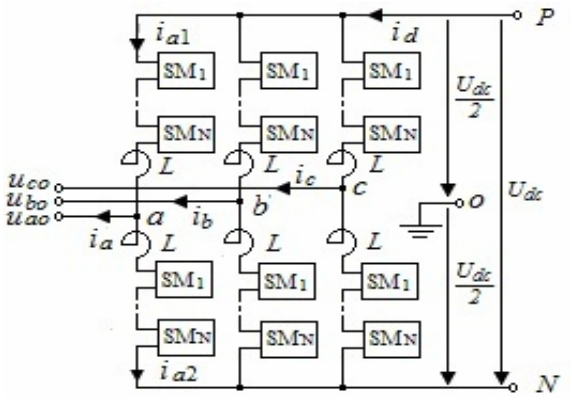


Figure 1. Three-phase topology diagram of a MMC.

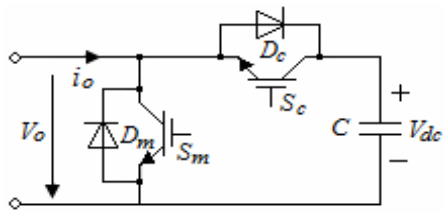


Figure 2. Structure of a SM.

Table 1. Commonly control states of a sub-modular.

Mode	S_m	S_C	i_O	V_O	Power path	C
1	on	off	>0	0	S_m	unchanged
2	on	off	<0	0	D_m	unchanged
3	off	on	>0	V_{dc}	D_c	charging
4	off	on	<0	V_{dc}	S_c	discharging

$$V_{dc} = \frac{U_{dc}}{M+L} = \frac{U_{dc}}{N} \tag{2}$$

Synthesis of phase output voltage of an 11-level MMC is shown in **Table 2**. Here, u_{a1} and u_{a2} are output voltage of the upper and lower arm of phase a; u_{ao} is output voltage of phase a.

3. Control Scheme

3.1. Multicarrier Fundamental Switching Modulation Strategy

Fundamental switching modulation is that the switches in the converters only need to be switched on and off once during one fundamental cycle; thus, the switching loss of the devices is reduced to minimum. The typical technology is staircase synthesis principle, i.e., it uses a staircase waveform to approximate the desired sinusoidal waveform. Staircase synthesis principle of multicarrier modulation is given by **Figure 5** with triangular carrier and sinusoidal reference waveform. It shows an 11-level converter's output phase voltage waveform. The goal is to choose the switching angles $0 \le \theta 1 < \theta 2 < \ldots < \theta 5 \le 90°$ so as to make the staircase waveform approximately equal to the given desired fundamental voltage u_{ao}. For 'N' level converter 'N-1' carriers are used. Interaction of particular carrier and reference is used to generate gating signal for particular complementary pair of switches in MMC.

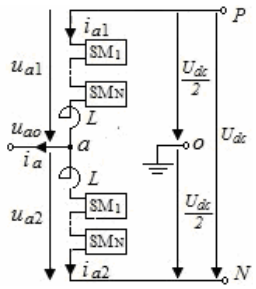


Figure 3. Single phase topology diagram of a MMC.

Table 2. Synthesis of phase output voltage.

M	L	u_{a1}	u_{a2}	u_{ao}
5	5	5 V_{dc}	$5V_{dc}$	0
4	6	$4V_{dc}$	$6V_{dc}$	V_{dc}
3	7	$3V_{dc}$	$7V_{dc}$	$2V_{dc}$
2	8	$2V_{dc}$	$8V_{dc}$	$3V_{dc}$
1	9	V_{dc}	$9V_{dc}$	$4V_{dc}$
0	10	0	$10V_{dc}$	$5V_{dc}$
6	4	$6V_{dc}$	4 V_{dc}	$-V_{dc}$
7	3	$7V_{dc}$	$3V_{dc}$	$-2V_{dc}$
8	2	$8V_{dc}$	$2V_{dc}$	$-3V_{dc}$
9	1	$9V_{dc}$	V_{dc}	$-4V_{dc}$
10	0	$10V_{dc}$	0	$-5V_{dc}$

By **Figure 4** we can get the desired sinusoidal waveform which is odd quarter-wave symmetric. In quarter of period, the upper triangular carrier waveform can be expressed as,

$$y_k = -\frac{2}{\pi}\omega t + k \quad 0 \le \omega t \le \frac{\pi}{2}, \quad k = 1, 2, \cdots 5 \tag{3}$$

Sinusoidal reference waveform is described by

$$y_{ref} = 5\sin\omega t \quad 0 \le \omega t \le \frac{\pi}{2} \tag{4}$$

Based on (3) and (4), we can get the switching angles for an 11-level converter as follows. $\theta_1 = 10.21°$, $\theta_2 = 20.74°$, $\theta_3 = 31.96°$, $\theta_4 = 44.54°$, $\theta_5 = 60.09°$.

For the modular 11-level converter, If we get output phase voltage waveform at AC side, we must make submodular switches S_c of the upper and lower leg (phase a) to be triggered with switching angles by **Figure 5**. Among the SMs, gate signal generation of S_m is opposite to S_c of corresponding SM. The advantage of this modulation method is that with the increase of voltage steps, staircase voltage gradation is finer and finer. Thus, the approximation becomes more and more accurate.

3.2. Selection of SMs and Capacitor Voltage Balancing

The capacitor voltages of the individual SMs must be monitored and kept equal. The voltages of the capacitors are periodically measured with a typical sampling-rate in the millisecond-range. According to their voltage, the capacitors are sorted in descending order by software. The modulation strategy determines the number of SMs that should be on in the upper and lower arms of the MMC (i.e., $\boldsymbol{S_c}$). Capacitor voltage values and also the direction of the arm currents are used to select $\boldsymbol{S_c}$ of the SMs in the upper (lower) arm and to determine which

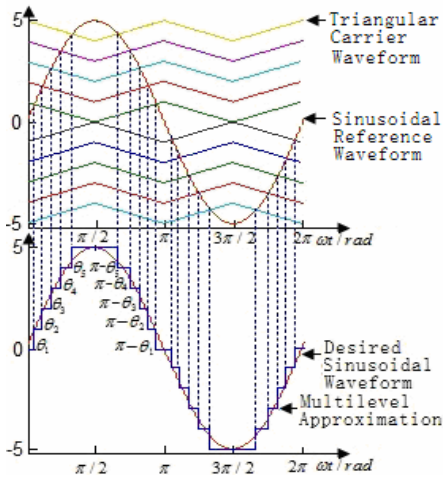
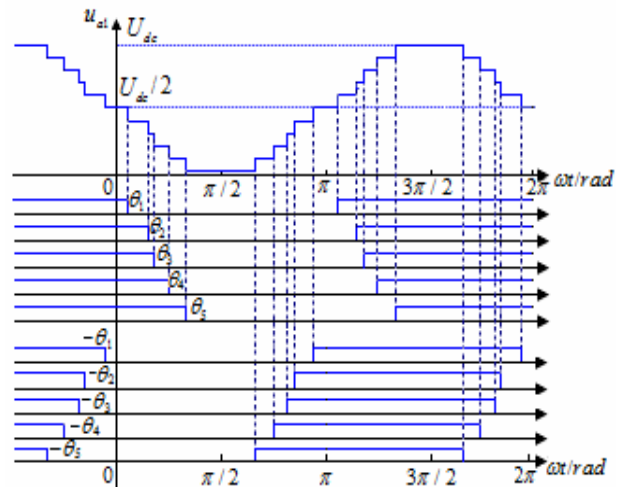
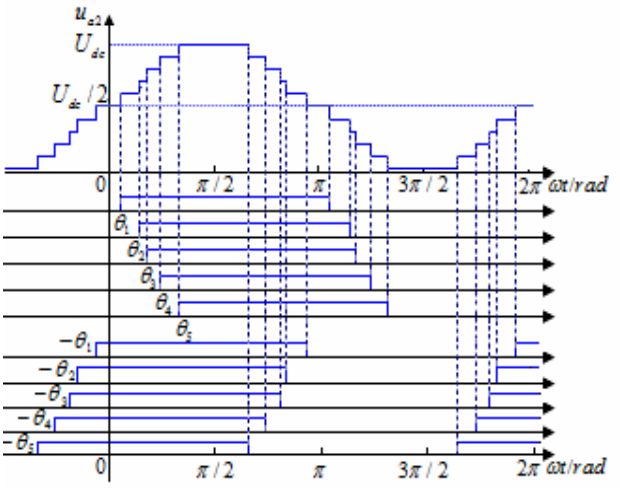


Figure 4. Staircase synthesis principle of multicarrier modulation.



(a) Gate signals generation of S_c in the upper leg (phase a)



(b) Gate signals generation of S_c in the lower leg (phase a)

Figure 5. Three-phase topology diagram of a MMC.

SMs should be switched on. When the current in the upper (lower) arm is positive, in order to impress the desired arm voltage, the required SMs with the lowest voltages are switched on. When the current in the upper (lower) arm is negative, in order to impress the desired arm voltage, the demanded number of SMs with the highest voltages is selected. Regardless of the direction of the upper (lower) arm current, if $\boldsymbol{S_c}$ of the SM is off, the corresponding capacitor will be bypassed and its voltage remains unchanged. By this method, continuous balancing of the capacitor voltages is achieved. Additionally, the power losses can be kept low by switching SMs solely, when a change of the output state is requested.

4. Simulation Validation

To validate the correctness and feasible of the staircase waveform modulation technology, an 11-level modular converter is constructed on MATLAB/SIMULINK. The upper (lower) arm of every phase is composed of ten identical SM. There is no additional central capacitive energy storage connected to the DC-bus bar. DC-link voltage U_{dc} is 20 kV and the capacitance C installed in each SM is 3000uF. The values of load resistance and inductance are 100 Ω and 500 mL. The relevant voltage waveforms and phase current waveforms of this 11-level topology are shown as **Figures 6-8**. **Figure 9** shows the capacitor voltages of the ten SMs of the upper arm of phase a. Simulation waveforms have demonstrated a good performance of the MMC concept and verified the correctness and feasible of the model.

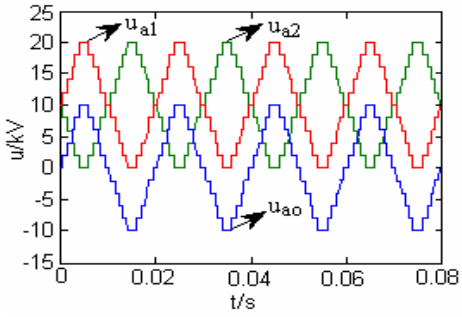


Figure 6. Upper and lower phase leg voltages u_{a1} and u_{a2} of phase a, phase voltage u_{ao}.

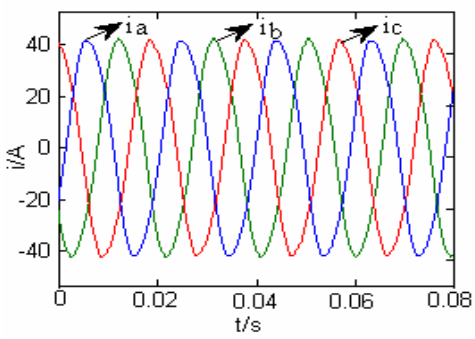


Figure 7. Phase currents.

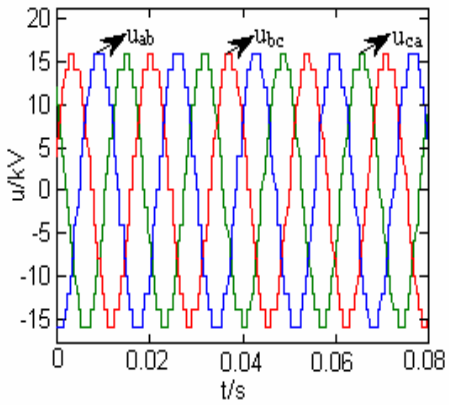


Figure 8. Line-to-line voltages.

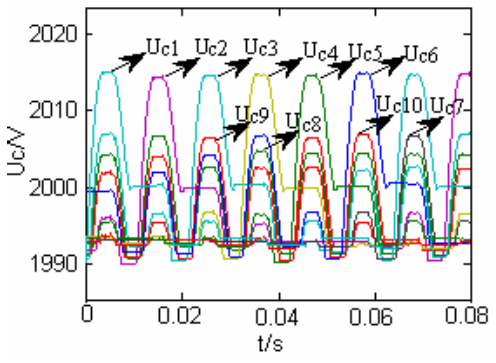


Figure 9. Upper phase leg capacitor voltages of phase a.

5. Conclusions

This paper introduced the topology of the new modular multilevel converter and its modulation control scheme. The staircase waveform modulation technology is discussed in detail, very convenient and suitable for multilevel converters. It turns out to be more and more outstanding with the increase of voltage levels. The output AC voltages can be adjusted in very fine increments. The proposed modulation technology makes the individual switching devices have much lower switching frequency (50 Hz) resulting in lower switching losses compared to a conventional VSC. Therefore, total system losses are relatively small and efficiency is consequently increased. Due to its interesting characteristics, the topology is very attractive for high-voltage dc transmission and MV converters.

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