

An Analysis of Buck Converter Efficiency in PWM/PFM Mode with Simulink

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ABSTRACT

This technical paper takes a study into efficiency comparison between PWM and PFM control modes in DC-DC buck converters. Matlab Simulink Models are built to facilitate the analysis of various effects on power loss and converting efficiency, including different load conditions, gate switching frequency, setting of voltage and current thresholds, etc. From efficiency vs. load graph, a best switching frequency is found to achieve a good efficiency throughout the wide load range. This simulation point is then compared to theoretical predictions, justifying the effectiveness of computer based simulation. Efficiencies at two different control modes are compared to verify the improvement of PFM scheme.

Keywords: PFM; PWM; Buck Converter; Efficiency

1. Buck Converter Background

For a buck converter, by varying the duty cycle of the switch, a desired average voltage output can be achieved. **Figure 1** shows a typical buck converter.

A typical synchronous buck circuit using MOSFETs as a switch is shown in **Figure 2**.

Power Width Modulation (PWM) signal is the most typical control signal applied on a switch in switching DC converters. It is usually a signal with fixed frequency. Inside one period, the signal is high for a specific percentage of the period (duty cycle) and then turns off; one would intuitively predict that the output voltage would

have a relation with input shown below:

$$V_{out} = V_{in}D, \text{ where } D \text{ is the duty cycle.}$$

PWM Switching Frequency Selection

Frequency is directly related to output ripple. Note that with the output voltage ripple assumed to be much smaller than its average value, most of the inductor current ripple must go through the capacitor. The output voltage ripple can be determined by the following equation.

$$\frac{\Delta V_{OUT}}{V_{OUT}} = \frac{(1-D)T_{sw}^2}{8LC}$$

where T_{sw} is the switching period and $f_{sw} = 1/T_{sw}$.

Normally the switching frequency should be set much higher than frequency of other LC components, ranging from 250 kHz to 1.5 MHz with feedback loop's ac characteristics in consideration [1-3]. International Rectifier uses 600 kHz for their IR 3840 regulator [6]; National Semiconductor uses 3 MHz fixed frequency for their LM3677 DC converter [4]. For simulation in this study: $V_{in} = 3.6 \text{ V}$, $V_{out} = 1.8 \text{ V}$, $C = 10 \text{ uF}$, $L = 1 \text{ uH}$. Output ripple = 0.014 V (with output voltage being 1.8 V), we can have the switching frequency equal to 894.42 kHz. Further simulation study shows that this is not the optimized frequency to achieve the best conversion efficiency. In the next section it is found that when frequency equals to 1600 kHz the PWM converter achieved the highest efficiency, with a ripple of 0.05 V. So it is a tradeoff between voltage ripples and efficiency in con-

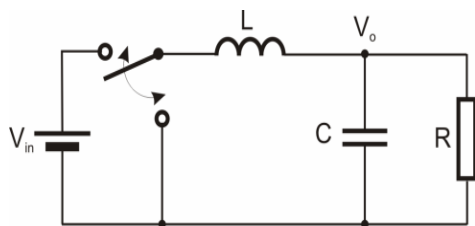


Figure 1. A typical buck converter.

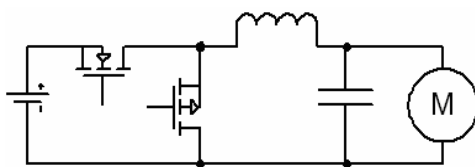


Figure 2. Buck converter with MOSFETs implementing switches.

clusion.

2. PWM Power Loss Analysis

In a DC-DC converter, the losses can be classified into two types: load dependent conduction losses and frequency dependent switching losses. The recent work in power loss analysis can be seen in literature [7,8].

2.1. Conduction Losses

During the continuous conduction mode (meaning inductor current won't reach down to zero) where the load current is relatively large, the main contribution of power losses are the conduction loss of the on-resistance of high-side (R_{on_PFET}) and low-side (R_{on_NFET}) switches and the series resistance of the inductor and capacitor (R_L , R_{ESR}).

2.1.1. Conduction Loss on Switches

When in operation the upper path and lower path switches are turned on and off depending on the duty cycle. Hence, the average resistance for these switches can be expressed as the on resistance multiplied by the duty cycles. The on-resistance in one switching cycle can be written as:

$$R_{switches_on} = R_{on_PFET} \times D + R_{on_NFET} \times (1-D)$$

Then the conduction loss due to on-resistance inside MOSFET can be written as:

$$P_{switches_on} = [R_{on_PFET} \times D + R_{on_NFET} \times (1-D)] \cdot I_{out}^2$$

2.1.2. Conduction Loss on Inductors and Capacitors

Non-ideal inductor has series resistance consuming extra power when passing through current. As mentioned before the average inductor current is also the same as the load current in Steady-state, the conduction loss can then be written as the product of this current squared and the resistance. Industrial experience shows however that current variation of the inductor also contributes to the loss. A more accurate empirical equation of inductive loss is given as follows:

$$P_L = R_L \times (I_{load} + \Delta I_{inductor} \times \sqrt{2})^2,$$

where R_L is the inductive resistance, I_{LOAD} is the load current and $\Delta I_{inductor}$ is the inductive current variation.

$\Delta I_{inductor}$ can be derived as:

$$\Delta I_{inductor} = \frac{V_{in} \cdot D \cdot D' \cdot T_s}{2L}$$

For capacitor, equivalent-series resistance (ESR) is the main cause for power loss. The empirical capacitive loss equation is given as follows

$$P_C = (\Delta I_{inductor} \times \sqrt{3})^2 \times R_{ESR},$$

where R_{ESR} is the capacitive resistance.

2.2. Switching Losses

Switching losses are frequency dependent losses. It can break down into two categories: hard switching loss and soft switching.

2.2.1. Hard Loss (overlap loss)

As the transistor switches on and off, the voltage and the current of the transistor cannot change simultaneously. Thus, the voltage across drain and source of the MOSFET and the current flowing from drain to source would have a time window during which voltage and current are nonzero. Thus, hard switching power loss of a switch can be written as

$$P_{switching} = \frac{1}{2} V_{in} \cdot I_{load} \cdot [t_{off} + t_{on}] \cdot f_s$$

Here t_{off} is the time taken for the current to reach down to zero when ON gate voltage is canceled and V_{DS} goes to high. t_{on} is the time taken for the current to recover when ON gate voltage is applied and V_{DS} goes low again. The losses due to each action are referred to as turn on loss and turn off loss, respectively.

2.2.2. Soft Loss (gate drive loss)

Soft loss is mainly due to the parasitic capacitors at the switching nodes. Since the switch size has to be relatively large to handle the load current with proper on-resistance, the capacitance associated with it at the switching node could be quite significant.

The parasitic capacitance at the switching node, C_{total} can be express as follows:

$$C_{total} = C_{ox} + C_{gb} + C_{ds} + C_{sb} + C_{gd} + C_{gs} + C_{db}$$

Thus, the gate driver loss for each stage can be *intuitively* given by

$$P_{gate_drive} = C_{total} V^2 f_s$$

Under the continuous conduction mode, the most dominate switching loss is due to the hard switching loss, since it is proportional to both current and switching frequency. However, under the light load condition, the most dominated switching loss is due to the gate drive loss since the current is small.

2.3. PWM Loss Simulink Verification

Figure 3 shows the PWM controlled buck converter implemented in Simulink. **Figure 4** shows power loss of this converter. **Figure 5** shows the conversion efficiency versus switching frequency.

3. PFM Control Mode Basic Theory

In order to tackle the dissatisfactory efficiency at low load,

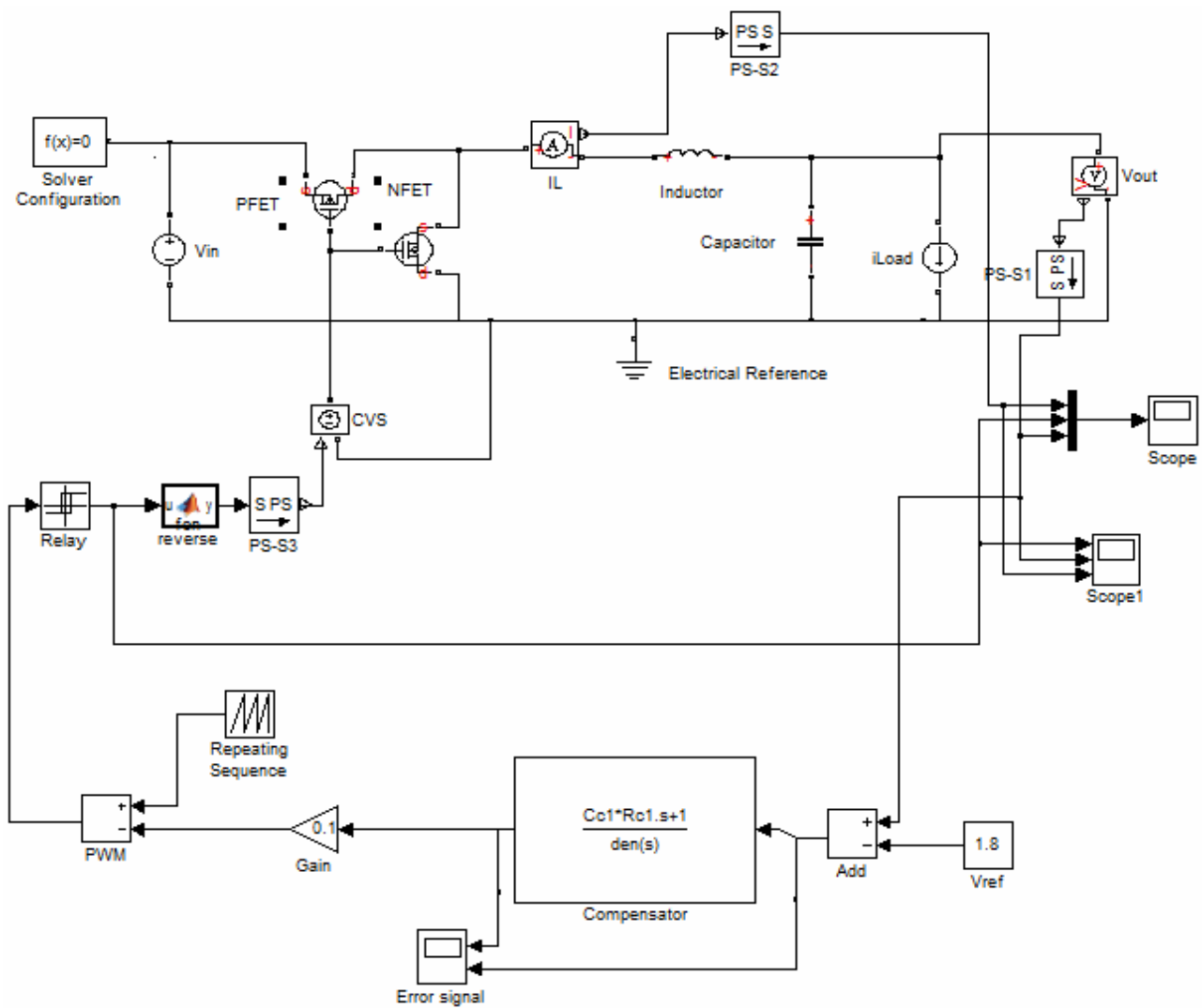


Figure 3. The PWM Buck Converter in Simulink.

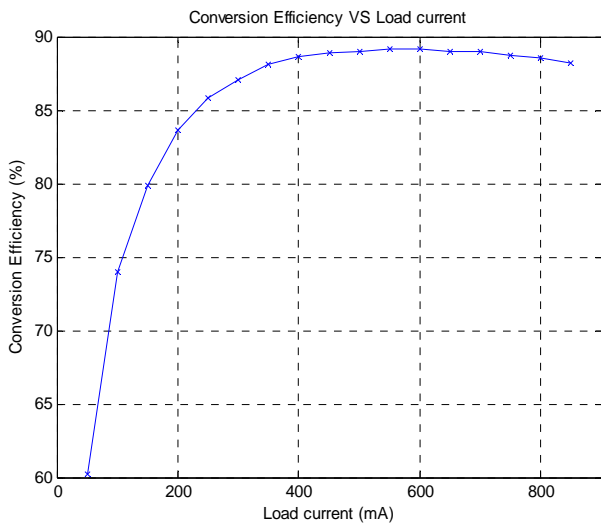


Figure 4. Conversion efficiency in a buck converter in PWM control mod with variant load current.

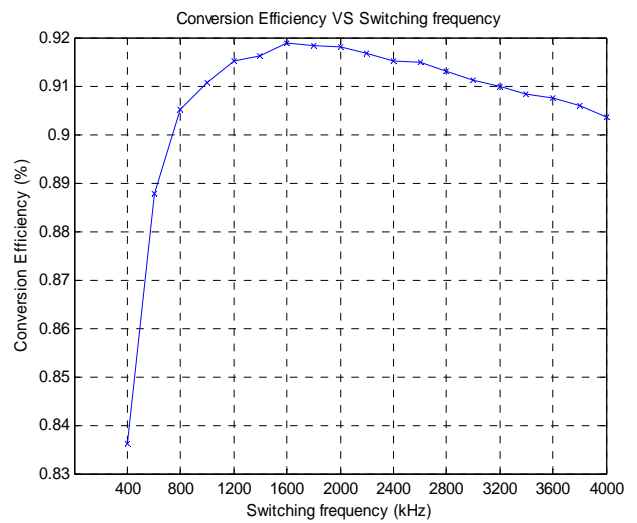


Figure 5. Conversion efficiency in a PWM buck converter vs. switching frequency.

we need a control scheme with lower switching frequency or conduction current. Note also the minimum frequency is needed to maintain a demanded output ripple. Pulse Frequency Modulation (PFM) scheme is designed to sufficiently decrease the switching frequency and conduction current at light load while maintaining required output voltage ripple [5].

3.1. Control Scheme

Unlike PWM where the P gate and N gate is controlled with duty cycle to be on and off, in PFM they are controlled by Thresholds. To be specifically, the thresholds used in PFM control are High V_{out} Threshold, Low V_{out} Threshold, Mode Transit Threshold and Inductor Current Peak Limit. **Figure 6** shows how this control scheme advances in time axis. PFM scheme is designed for light load so when the load current increases beyond a certain point, the output voltage would be drawn below a threshold, which is shown in the figure as “Mode Transit Threshold”. When this happens, the circuit switches back to PWM mode to keep up with the load demand.

3.2. PFM Power Loss Analysis

The reason for loss saving in this control mode is mainly due to the “sleep phase”. During this phase both switches are turned off, the source for output power is all from the capacitor charge, saving all losses could have occurred on switches and the inductor. During the PFM operation, the output is being charged as needed. Thus, the average inductor current and load current would be smaller than the ripple current and the conduction loss would only occur during “pump phase”, resulting in less power loss.

The detail equations are omitted in the paper due to space limitation.

3.3. PFM Loss Simulink Verification

LM3677 is a DC converter from National Semiconductor using PFM/PWM control mode. In this device output voltage thresholds are set between $\sim 0.2\%$ and $\sim 1.8\%$ above nominal PWM output voltage. In order to compare conversion efficiency under same criteria, The PFM mode also has to set the same output ripple the same as the one in PWM (1.77 V to 1.82 V). Also the typical peak current in PFM mode is:

$$I_{peak} = 112mA + V_{in} / 20\Omega$$

In our study, $V_{in} = 3.6$ V. The result is 192 mA. With LM3677 as benchmark, the thresholds of simulation in this study are set to be: High V_{out} Threshold = 1.814 V; Low V_{out} Threshold = 1.809 V; Inductor peak current limit = 200 mA; Mode Transit Threshold = 1.804 V. **Figure 7** shows the PFM controlled buck converter in Simulink.

4. Loss and Efficiency Comparison

The blue curves dotted with x are PWM mode, red curves dotted with o is PFM mode. It's easily seen that the loss in PFM is much lower than that in PWM mode at light load (10 mA - 40 mA), and rapidly increases with the load going high. **Figure 8** shows the loss comparison curves with all losses summed up.

The efficiency is measured with load from 10 mA - 110 mA as shown in **Figure 9**.

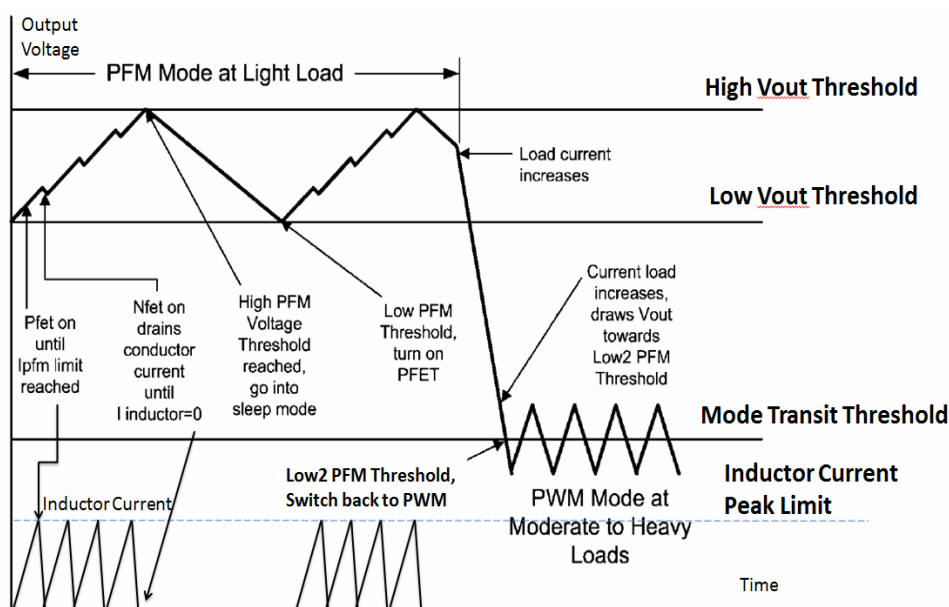


Figure 6. PFM mode operation and transfer to PWM mode.

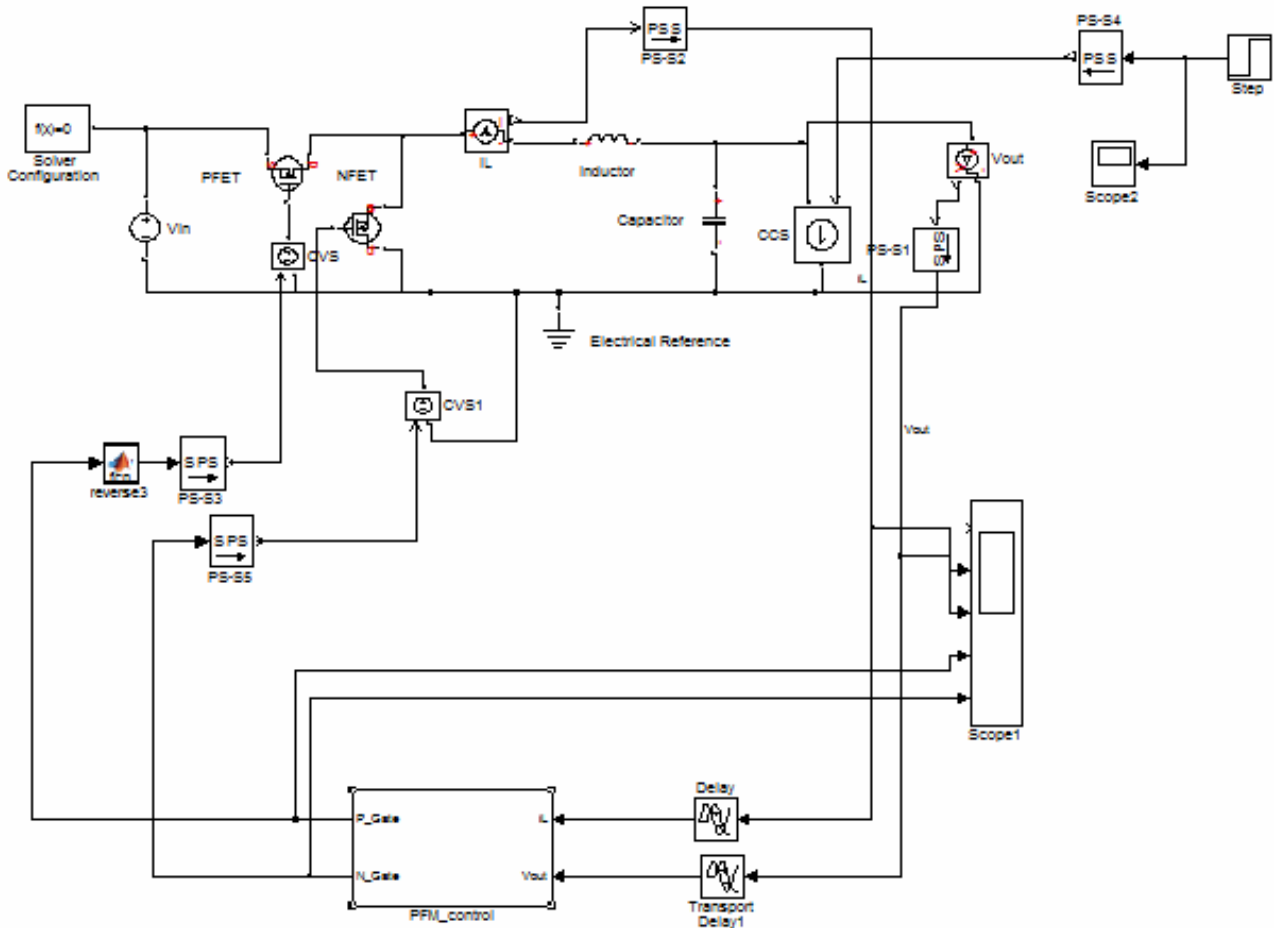


Figure 7. Shows the PFM controlled buck converter in Simulink.

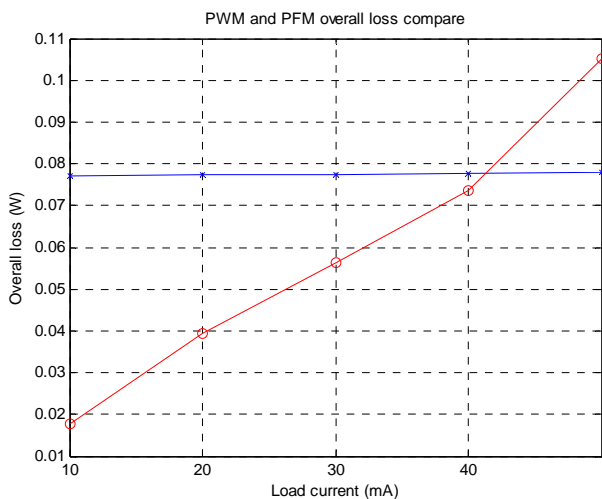


Figure 8. Shows the loss comparison curves with all losses (PWM is indicated by x; PFM is indicated by o).

From the graph we can see that the efficiency improvement at light load varies from 0 - 30%. Note in PWM the frequency has been fine-tuned at 1600 kHz so the improvement is pretty significant.

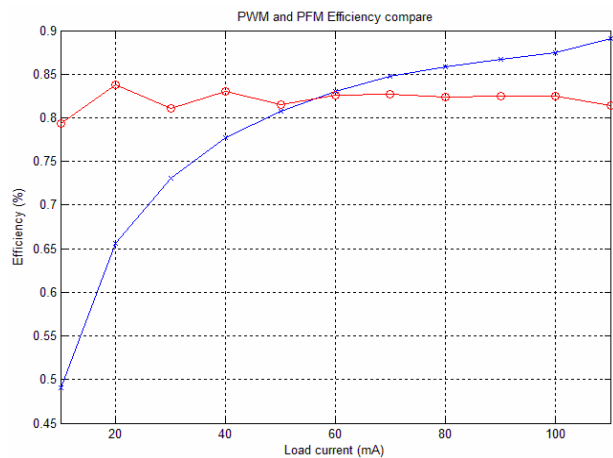


Figure 9. Efficiency comparisons between PWM and PFM mode control. (PWM is indicated by x; PFM is indicated by o).

5. Conclusions

Computer based simulation proved the effectiveness of theoretical prediction on conversion power losses. The proposed PFM control scheme is also verified to have a

significant improvement on conversion efficiency at light load (as high as 30%).

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