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Comparative Simulation Study between Gate Firing Units for HVDC Rectifier Based on CIGRE Benchmark Model

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Abstract

A simulation study between the DQO gate firing unit (GFU) and a proposed GFU for high voltage direct current (HVDC) rectifier based on the CIGRE benchmark model in Matlab/Simulink is carried out. The proposed GFU does not use traditional phase lock loop (PLL) and offers structural simplicity, fast response and immunity to ac system voltage unbalance, harmonics, voltage sag, frequency jump and phase jump etc. Since there is no loop filter, no tuning issues are involved. Advantages of the proposed GFU are confirmed by extensive simulation results.

Keywords: CIGRE HVDC, Phase Lock Loop, Rotating reference Frame, Simulation

1. Introduction

High voltage direct current (HVDC) transmission systems are being increasingly used nowadays. A total of 47.6 GW of long-distance HVDC has been installed worldwide from 1962 to 2009 with 50% of this capacity constructed after the year 2000 and additional 26.5 GW of new long-distance HVDC are under construction [1]. HVDC systems are usually simulated using PSCAD/EMTDC or EMTP. This paper simulates the HVDC rectifier based on the CIGRE benchmark model using Matlab/Simulink. References [2-4] describe simulation studies of different gate firing units (GFU) used in HVDC using EMTP.

The first use of phase lock loops (PLL) for synchronization using a voltage controlled oscillator (VCO) was proposed in [5]. This is referred as the Conventional GFU, based on a VCO and a PLL. The ac system voltage is called as commutating voltage (V_{com}). The main objective of this GFU is to generate a voltage signal V_{sync}, synchronised with V_{com}. In the conventional GFU, the error between these two signals is fed to a VCO to change the frequency and phase of V_{sync} so that error is minimized. V_{sync} is then used to derive equidistant firing pulses for the thyristors of the HVDC rectifier. Since, this GFU has low pass filter (LPF) in the loop to filter out the internally generated 2nd harmonic term; it introduces a compromise between transient response and disturbance rejection. The analysis of this GFU is reported in [2].

Another GFU, trans-vector PLL [3], is widely used now-a-days. The main idea here, is to calculate the difference between the phase angle of V_{com} and V_{sync} and maintain this value to zero by means of a proportional-integral (PI) controller (**Figure 1**). This trans-vector PLL has several deficiencies [6] which are revised in section II.

All PLLs have stability issues because these are closed loop systems. Tuning the PI controller parameter, as in case of conventional PLL with LPF, with a high bandwidth results in a quicker response for transients like phase jumps, voltage sags and swells, etc. However, a high bandwidth is results in poor filtering of noise and harmonics and also, can produce instability. Low bandwidth PI controller is better for noise, harmonics and stability but they have a poor speed of response for transients. Additionally, there is a trade-off in selecting PI controller gains for phase and frequency jumps. Transient response to phase step is better for over-damped system. Transient response can be improved if bandwidth is increased. This leads to filtering problems. Transient response to frequency step is better for under-damped system. For under-damped system the settling time is faster as compared to the over-damped system but with higher over-shoot.

This paper presents a new open loop structure as an alternative to PLLs for synchronization and firing pulse generation. This alternative synchronization and firing

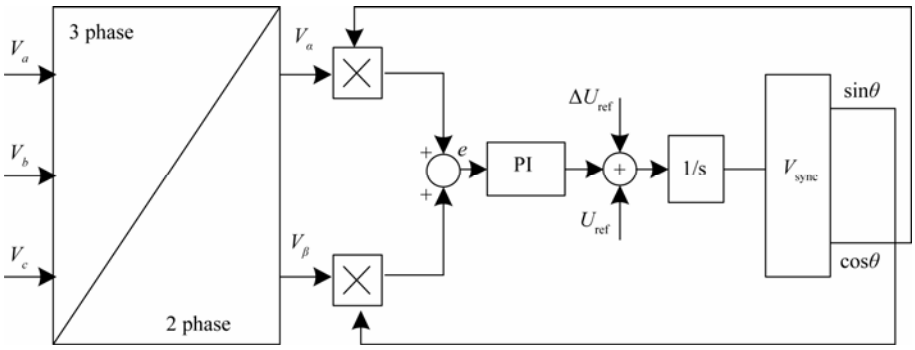

Figure 1. Block diagram of trans-vector PLL GFU.

pulse generation scheme is based on transforming the ac system voltage into rotating reference (dq-reference) frame and generate the fundamental positive and negative sequence component. This scheme can operate under unbalanced, distorted and variable-frequency conditions of the mains voltage. The success of this scheme depends on real time frequency detection algorithm used to track the frequency of the ac system voltage.

The main features of the proposed GFU can be summarized as:

1) It is immune to mains voltage unbalance, harmonics, voltage sag, phase jump, frequency variation etc.

2) There is no stability or tuning issue involved as it is an open loop structure without any filter in the loop.

3) The transient response does not depend on the amplitude of ac system voltage.

4) The time of transient response is always fixed for fixed frequency applications. For variable frequency applications, this depends on the frequency detection algorithm, to track frequency during the transient. The faster the frequency lock, faster is the response.

5) This method offers structural simplicity which can be easily implemented both in hardware and software environments.

The model used here is a 6-pulse HVDC rectifier system similar to the one considered in [3].

2. Trans-Vector PLL

The ac system voltages V_a, V_b and V_c are first transformed to the stationary reference frame using (1):

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 2 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{1}$$

The error signal, e, is given as:

$$e = \left(V_\alpha \cos\theta + V_\beta \sin\theta\right) \tag{2}$$

The error signal is fed through a PI controller to generate a reference frequency for the VCO. The center frequency of the VCO is set at 50 Hz. The output of the PI controller can change the frequency output of the VCO accordingly. The output of the VCO is a signal proportional to phase angle. This signal is used to generate the Sine-Cosine waveforms which are fed back to the multipliers to generate the error signal. Under steady state, this error is reduced to zero and output V_{sync} will be in synchronism with V_{com}.

The closed loop transfer function from **Figure 2** is:

$$H(s) = \frac{V_m K_p \frac{1+s\tau}{s\tau} \times \frac{1}{s}}{1 + V_m K_p \frac{1+s\tau}{s\tau} \times \frac{1}{s}} \tag{3}$$

$H(s)$ can be rewritten the form:

$$H(s) = \frac{2s\xi\omega_n + \omega_n^2}{s^2 + 2s\xi\omega_n + \omega_n^2} \tag{4}$$

where $\omega_n = \sqrt{\frac{K_P V_m}{\tau}}$ and $\xi = \frac{\omega_n}{2}\tau = \frac{K_P V_m}{2\omega_n}$

A well designed PLL for power system applications should meet the following criteria:

1) Damping factor, $\xi = 1$ for optimum phase and frequency jump transient response.

2) Narrow bandwidth (low ω_n) for immunity against unbalance, harmonics and noise.

Phase margin (*Pm*) is a very useful parameter used to specify the control system performance of the PLL because it is related with ξ [7]:

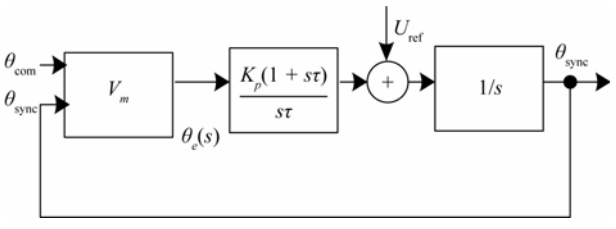

Figure 2. Closed loop transfer function of trans-vector PLL GFU.

$$Pm = \tan^{-1} 2\xi\sqrt{2\xi^2 + \sqrt{4\xi^4 + 1}} \quad (5)$$

A PLL is stable if its *Pm* is positive and unstable if its *Pm* is negative. *Pm* also gives a qualitative indication of the loop damping. Since smaller damping is rarely wanted, *Pm* below 50˚ is usually not recommended *i.e.* ξ less than 0.5 is avoided. In [3] the recommended value of *Pm* is given as: 60˚ and $\omega_n \cong 40$ Hz. These two selections give a good compromise between a fast response and a small synchronising error. Simulation results for trans-vector PLL under different conditions is presented next for $V_m = 230V_{\text{rms}}$, $\xi = 0.6$ and $\omega_n = 2\pi$ (40) rad/s. K_P = 1.31 and τ = 4.77 ms are calculated from (4).

The simulation results show: Line voltages V_a, V_b, V_c (in Volts), Phase angle, θ_{sync} (in Radians), V_{sync} (pu) and error signal, *e* (in Volts). The x-axis represents time (in seconds).

2.1. Under Ideal V_{com}

As seen from **Figure 3**, the trans-vector PLL has a good performance with ξ = 0.6 and $\omega_n = 2\pi$ (40) rad/s when V_{com} is balanced and without any harmonics.

2.2. Under Presence of Harmonics in V_{com}

Figure 4 shows that when V_{com} gets corrupted with harmonics, PLL fails to obtain the correct angular position

2.3. Under Presence of Voltage Unbalance V_{com}

Similarly, when V_{com} has unbalance, PLL again fails to obtain the correct angular position (**Figure 5**).

2.4. Under Loss of V_{com} for Few Cycles

Two different cases are simulated for loss of V_{com}.

2.4.1. Ideal V_{com}

If there is a loss of V_{com}, the response of PLL depends on the harmonics present in V_{com}. **Figure 6** shows that PLL falls to its "free running" mode if V_{com} is ideal.

2.4.2. Distorted V_{com}

Figure 7 shows that if there is a loss of V_{com} when V_{com} is corrupted due to harmonics, PLL fails to obtain correct angular position.

2.5. Under Phase Jump of 20˚ in V_{com} at 0.1 s

As shown in **Figure 8**, under 20˚ phase jump and harmonics in V_{com}, it has a fairly good transient response (around 10 ms).

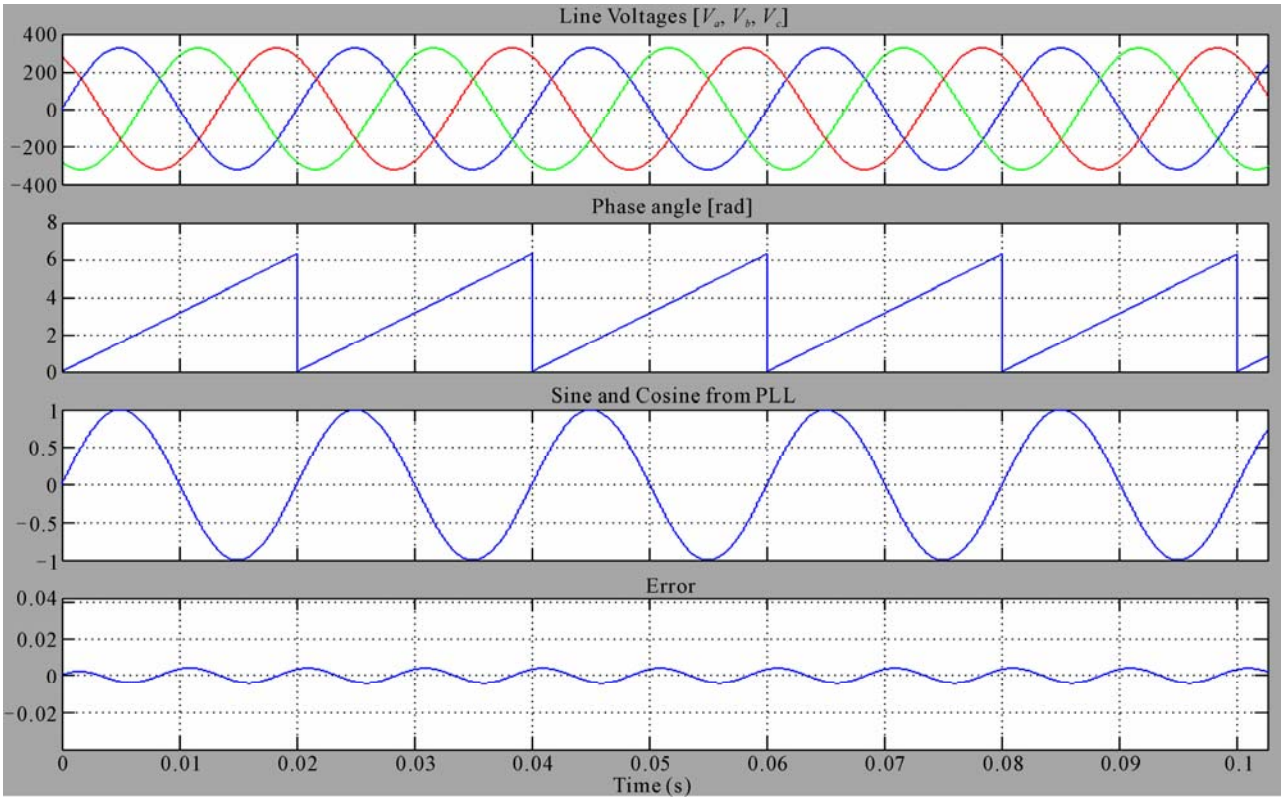

Figure 3. Results of trans-vector PLL GFU under ideal V_{com}.

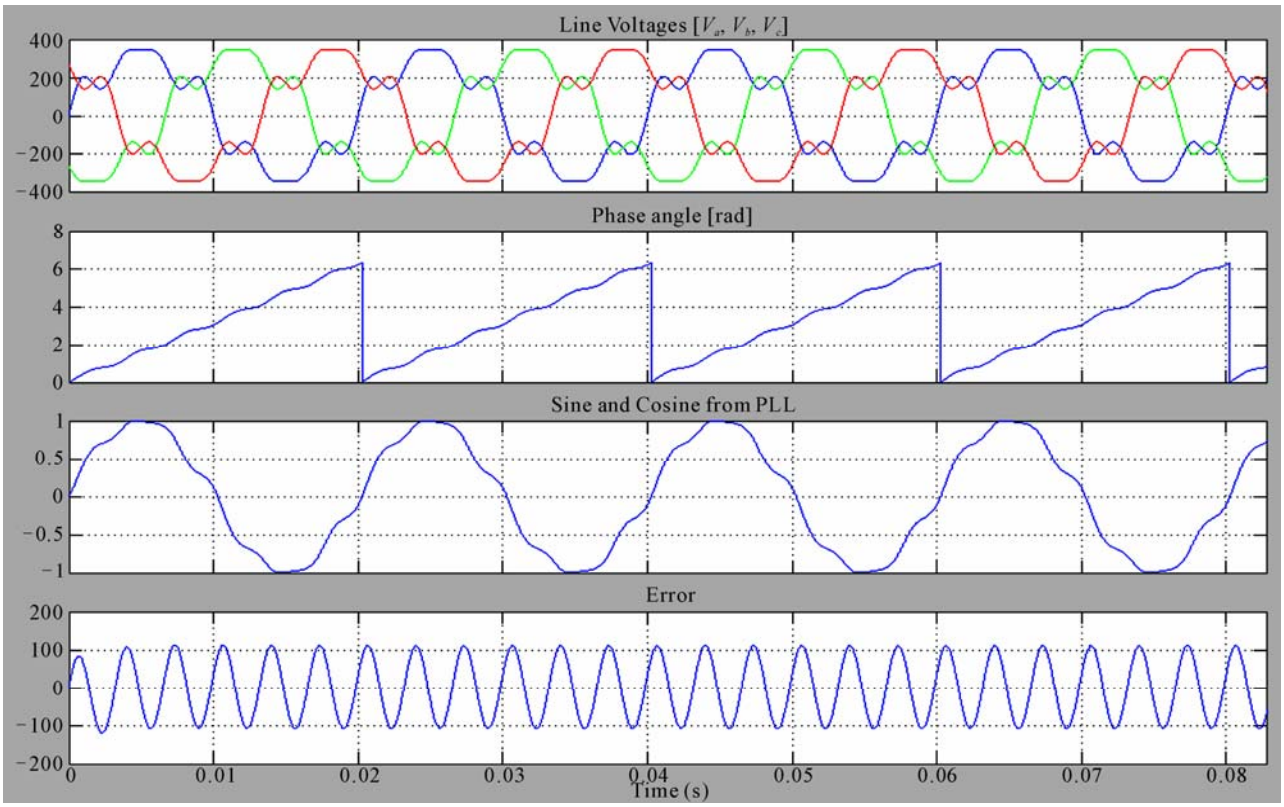

Figure 4. Results of trans-vector PLL GFU for 5th and 7th harmonics in V_{com}.

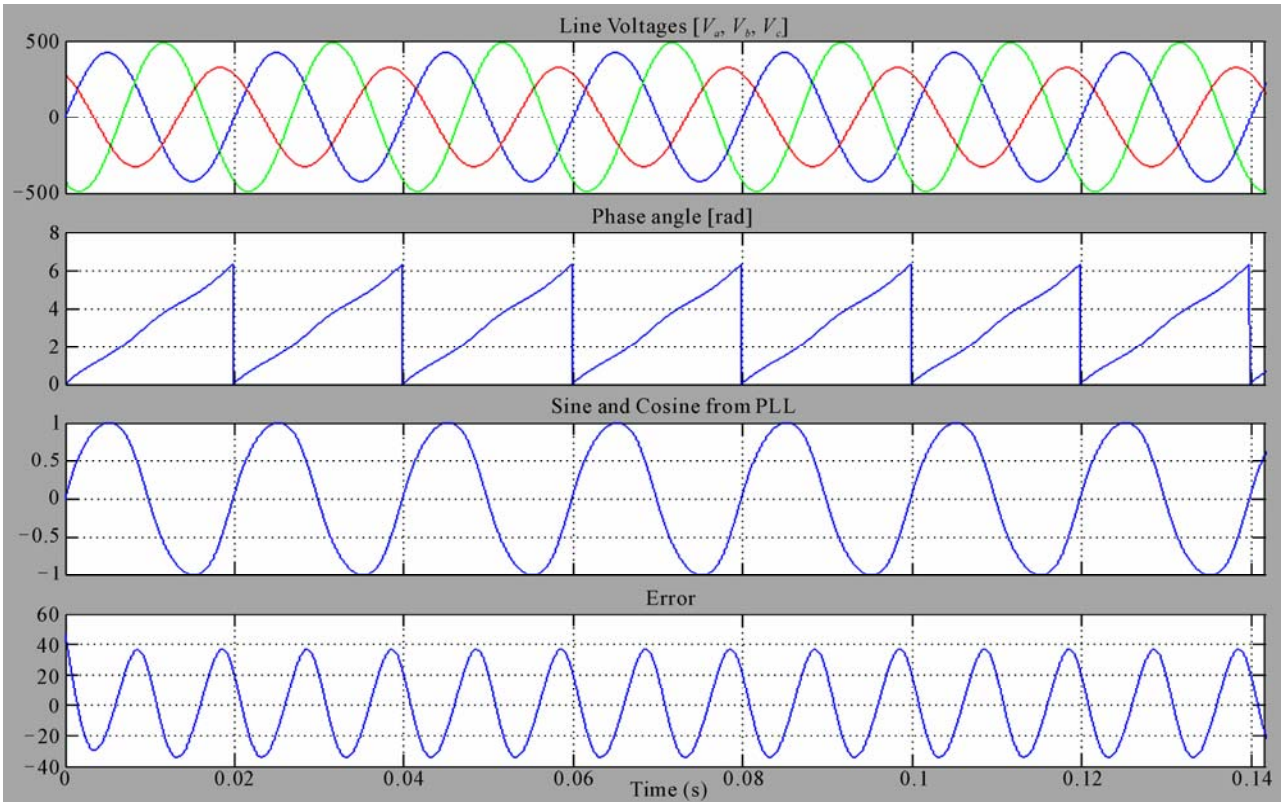

Figure 5. Results of trans-vector PLL GFU for unbalance in V_{com}.

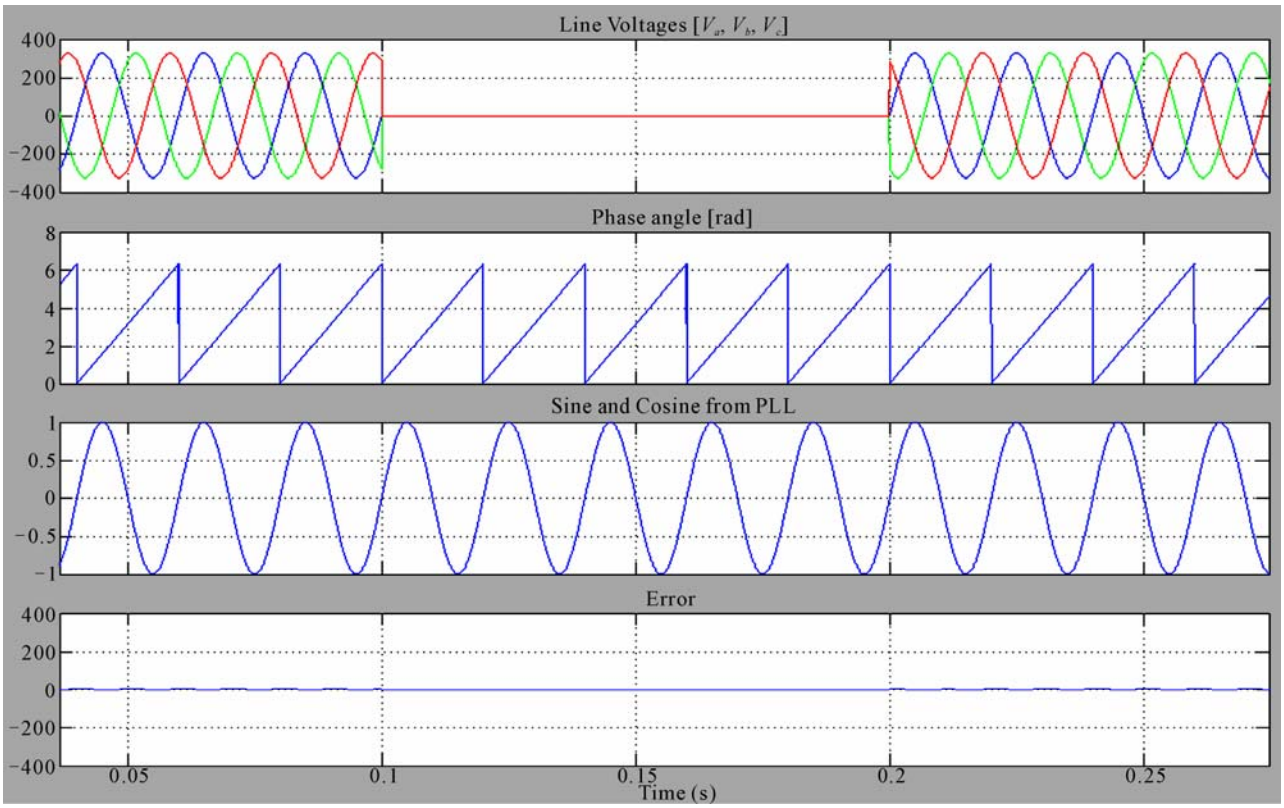

Figure 6. Results of trans-vector PLL GFU for loss of V_{com} from 0.1 s to 0.2 s.

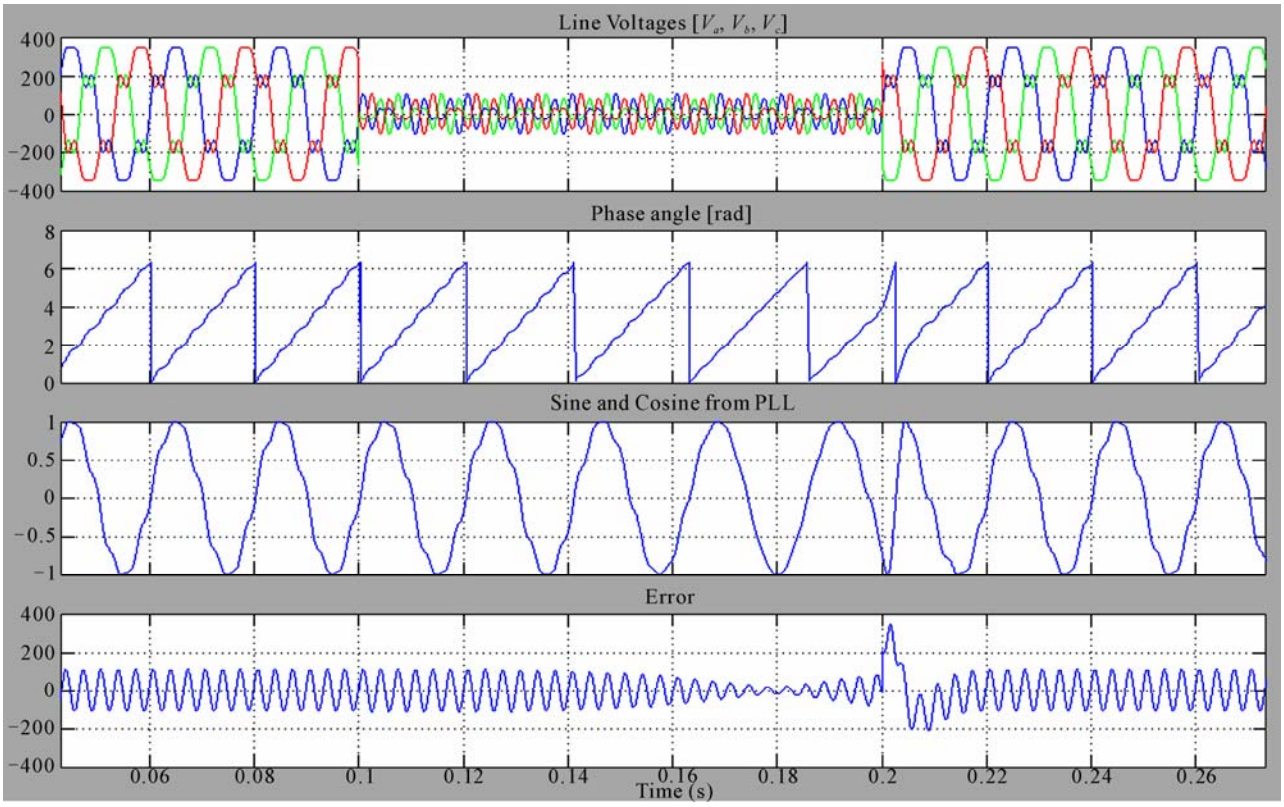

Figure 7. Results of trans-vector PLL GFU loss of V_{com} from 0.1 s to 0.2 s and5th and 7th harmonics in V_{com}.

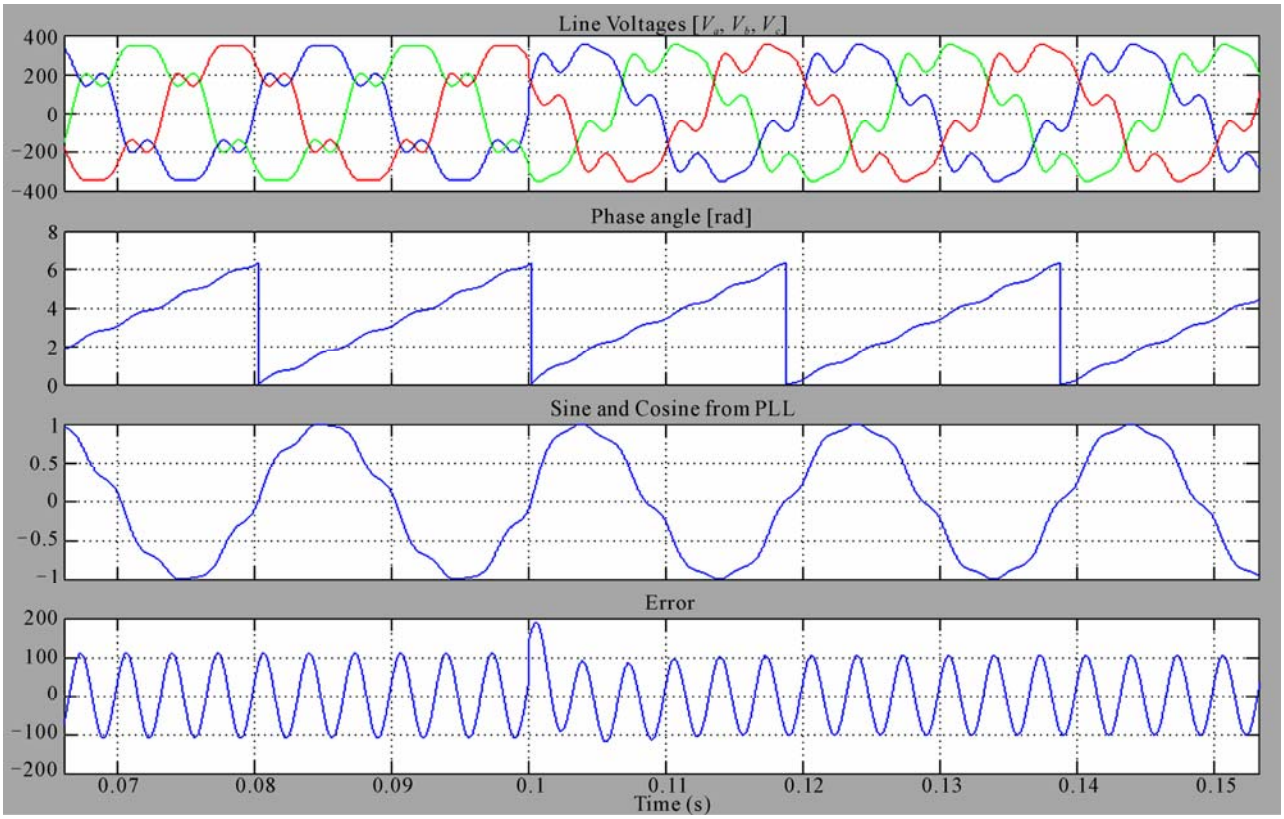

Figure 8. Results of trans-vector PLL GFU for 20° phase jump in V_{com}.

2.6. Under Frequency Jump of 1 Hz at 0.1 s

For frequency jump of 1Hz, transient response is less than 20 ms (**Figure 9**).

The trans-vector PLL does not have the problem of internal second harmonic generation and has fairly good transient responses but, as revised in this section, it is sensitive to disturbances. Phase and frequency jumps also affect the error signal in such a way that it introduces trade-offs. While there have been attempts to solve most of these problems in [8-15], structural and computational complexity has increased with each attempt. Usually, HVDC transmission systems use PI controllers with fixed PI gains. Such controllers work well for a small range of disturbances. However, when the ac system voltage has disturbances greater than this range, the PI controllers may not be able to provide desired response. In that case, tunable PI controllers are required.

3. Proposed GFU

Since higher order harmonics like 21st, 23rd etc. are insignificant for industrial power systems, this method is considered here only up-to the 19th harmonic. This can be extended to higher harmonics also, if needed. In [16], Yao proposed the concept of extracting the fundamental component with a short delay in rotating reference frame. The block diagram is shown in **Figure 10**. Let, $V_{dq}(t)$ represent the voltages in dq-reference frame. Delaying $V_{dq}(t)$ by τ (¼ of the fundamental cycle), $V_{dq}(t-\tau)$ is obtained which is same in amplitude but exactly 180° out of phase. Thus, by adding the delayed signal to the original signal cancellation of negative sequence, 5th harmonic, 7th harmonic etc is obtained. The amplitude is doubled which can be divided by 2 to get the original amplitude. This is a very simple and fast method by which DC components in dq-reference frame is obtained. Higher order harmonics like 11th, 13th etc can also be cancelled by introducing appropriate delays.

The block diagram of the proposed GFU is shown in **Figure 11**. After cancelling out various distortions, the fundamental positive sequence component (V_p) and phase angle (α_p) is obtained.

Once the magnitude of V_p and α_p is obtained, a set of balanced three phase voltages, V_{sync} which are in phase with the positive sequence of the V_{com}, are calculated by adding or subtracting $2\pi/3$ radians. Once the three set of voltages are obtained, the first firing pulse (S_1) is obtained at the zero crossing of phase to phase V_{sync}. The remaining firing pulses are obtained after delaying S_1 by 60° [17]. The delay of 60° is maintained by calculating the time period from the frequency of V_{com}.

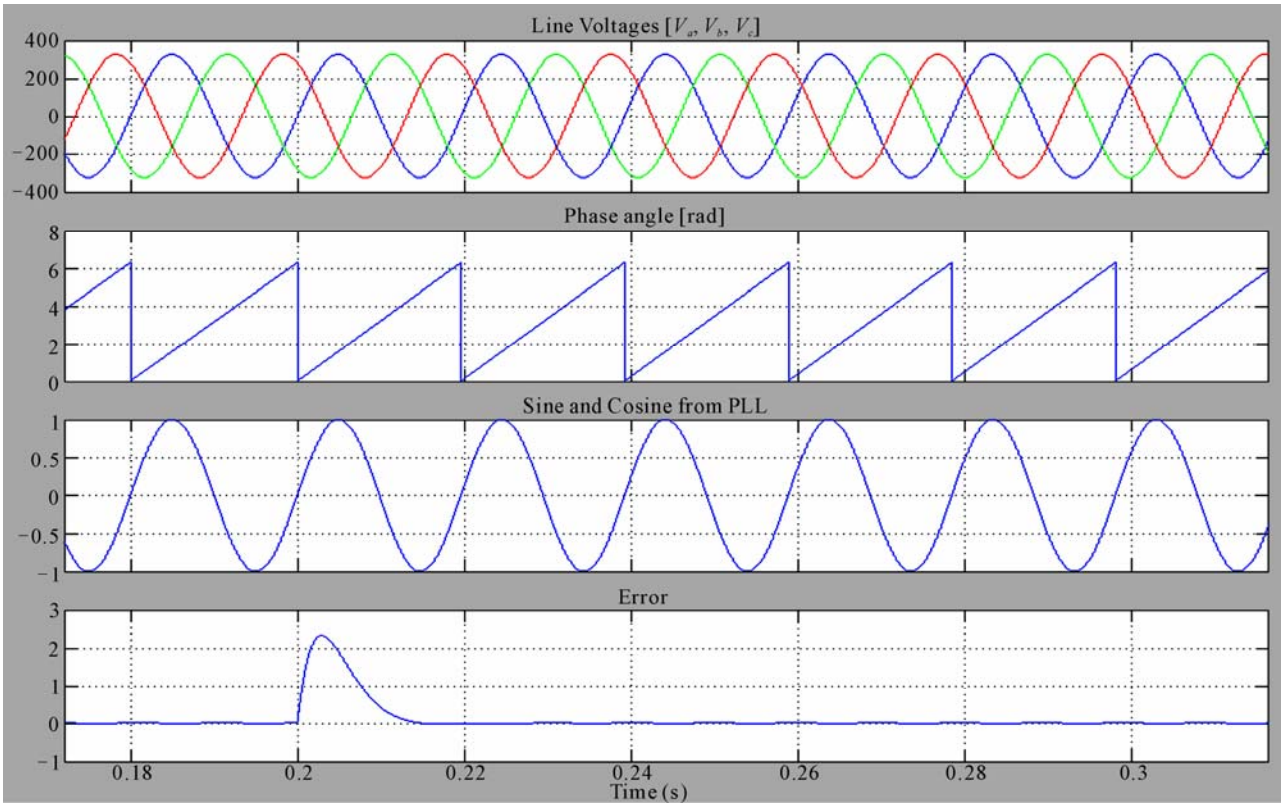

Figure 9. Results of trans-vector PLL GFU for 20˚ phase jump in V_{com}.

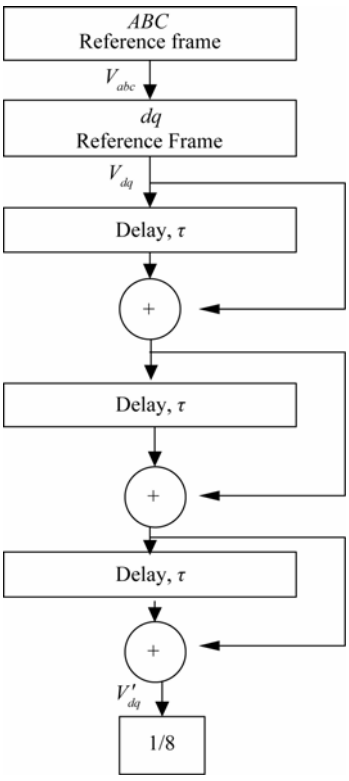

Figure 10. Process of extracting fundamental component using Yao's method.

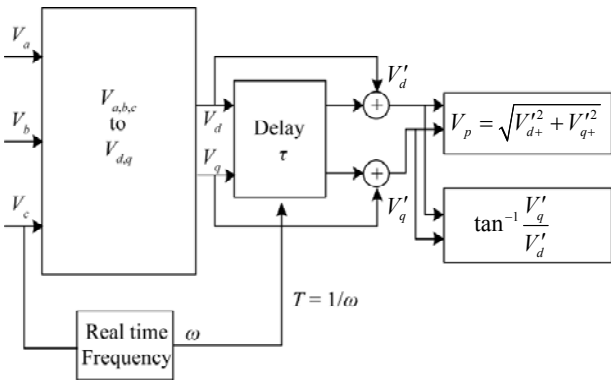

Figure 11. Block diagram of proposed GFU.

This section shows the generation V_{sync} from V_{com} under various corrupting sources such as voltage harmonics, unbalance, sags, phase outage, frequency jump and phase jump. The simulation results show: V_{com}, V_{sync} (phase to ground), V_{sync} (phase to phase) (in Volts), Phase angle, θ_{sync} (in Radians) and firing pulse (S_1) to first thyristor. The x-axis represents time (in seconds).

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3.1. Under Ideal V_{com}

As seen from **Figure 12**, the proposed GFU has a good performance when V_{com} is ideal. V_{sync} is precisely gener-

ated using from V_{com}.

3.2. Under Presence of Harmonics in V_{com}

In this case, 5th and 7th harmonic components are added to V_{com}. From **Figure 13**, it is seen that correct phase angle is obtained for this case also. A firing pulse synchronised at the zero crossing of V_{sync} (phase to phase) and delayed by appropriate firing angle (α) is obtained.

3.3. Under Presence of Voltage Unbalance V_{com}

In **Figure 14**, V_{com} is unbalanced. It is seen that even under unbalance correct phase angle is obtained.

3.4. Under Loss of One Phase of V_{com} for Few Cycles

Loss of phase A is simulated in **Figure 15** from 0.1 s to 0.16 s. Clean V_{sync} is obtained in this situation too. Correct firing pulse can be maintained despite loosing one of the phases of V_{com}.

3.5. Under Phase Jump of 45˚ in V_{com} at 0.1 s

A phase jump of 45˚ at 0.1 s under presence of harmonics in V_{com} is simulated in **Figure 16**. A clean V_{sync} is obtained from the calculated fundamental positive sequence magnitude and phase angle.

3.6. Under Frequency Jump of 1 Hz at 0.1 s

A frequency step of 1Hz at 0.1s is simulated for this case. **Figure 17** shows that after 1 cycle, the new V_{sync} is synthesized.

4. CIGRE Benchmark Model

The HVDC rectifier model [18] based on CIGRE benchmark model is shown in **Figure 18**. The steady state output voltage V_{dc} is:

$$V_{dc} = B\left(1.35V_{L-L_{\text{sec}}}\cos\alpha - \frac{3\omega L_c}{\pi}I_{dc}\right) \quad (6)$$

where B: number of bridges in the converter, $V_{L\text{-}Lsec}$: line-line RMS ac voltage of transformer secondary, ωL_c: equivalent transformer and line reactance at fundamental frequency, I_{dc}: output direct current, α: firing angle. Only a 6-pulse system, without ac filter, is considered here. The ratings for the DC side are:

V_{dc} = 250 kV, I_{dc} = 1 kA, P_{dc} = 250 MW, R_L = 250 Ω.

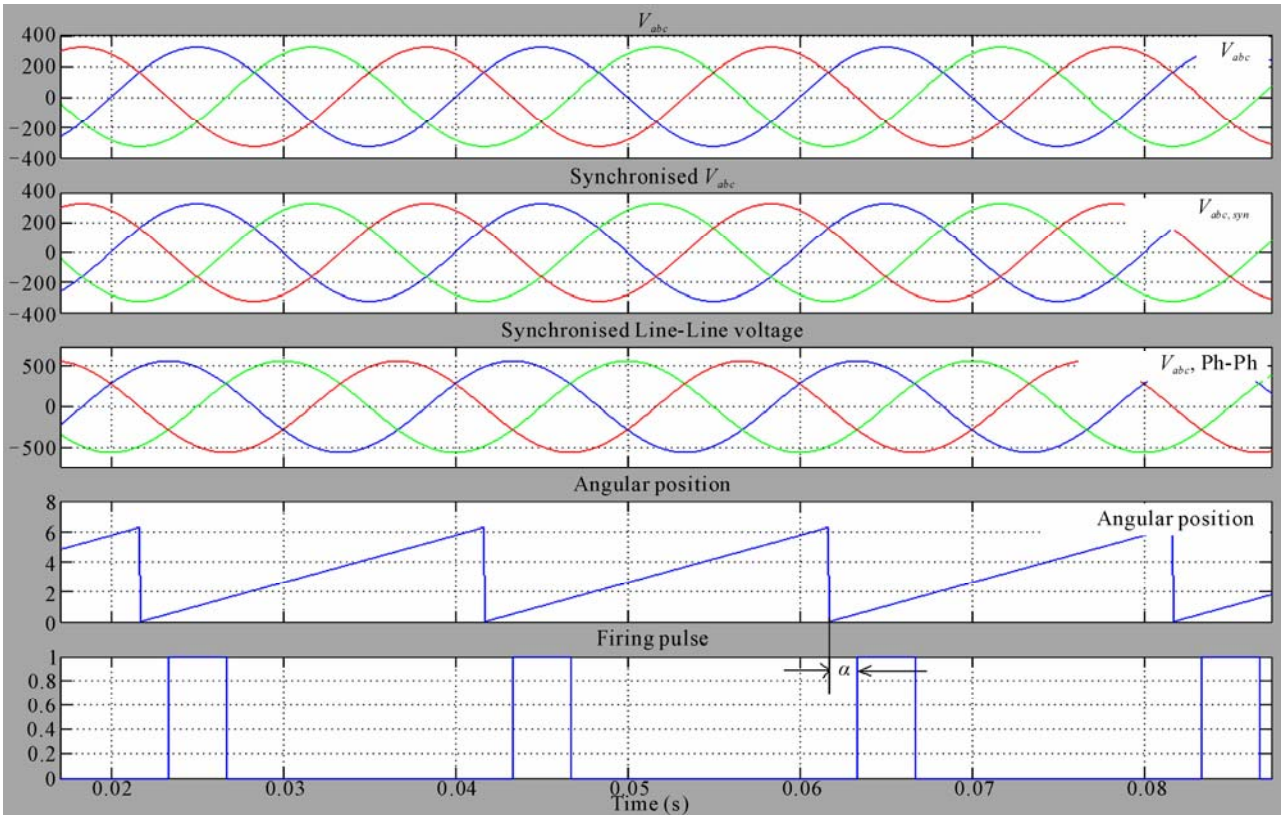

Figure 12. Results of proposed GFU under ideal V_{com}.

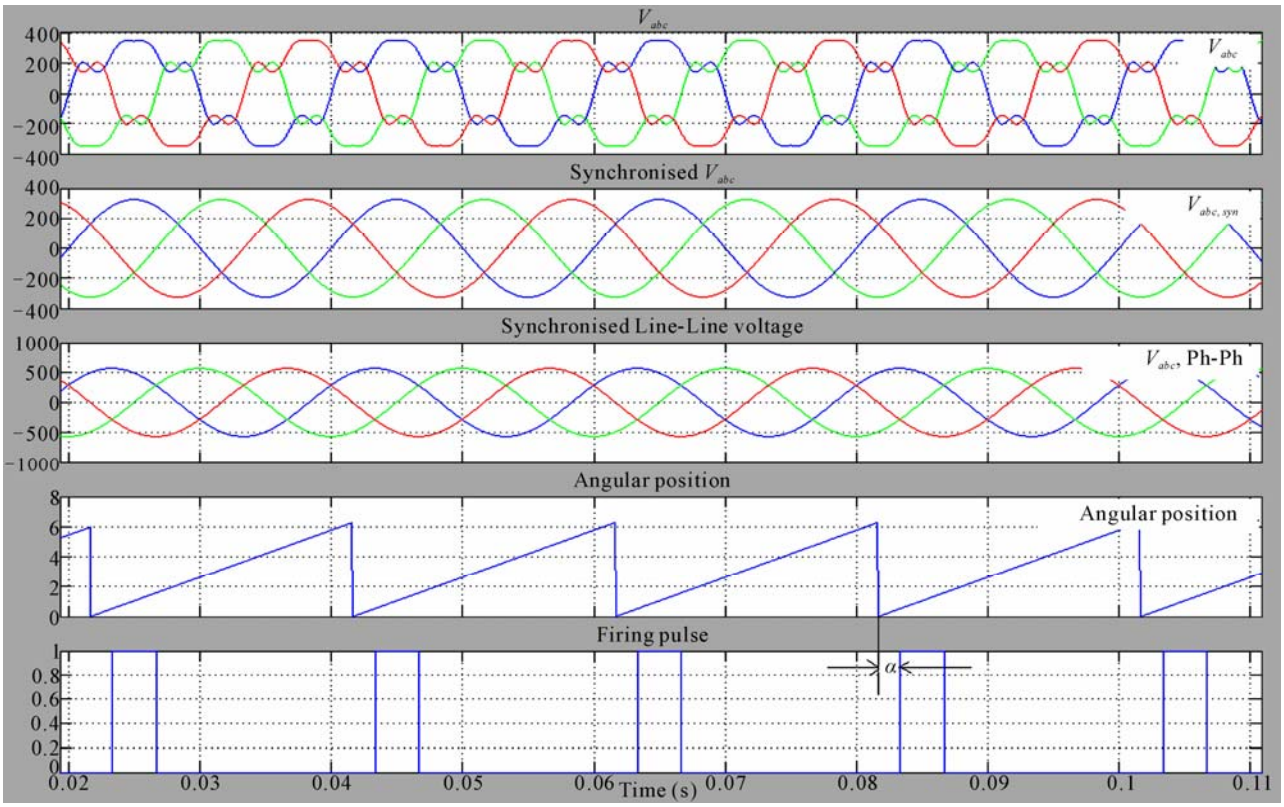

Figure 13. Results of proposed GFU for 5th and 7th harmonics in V_{com}.

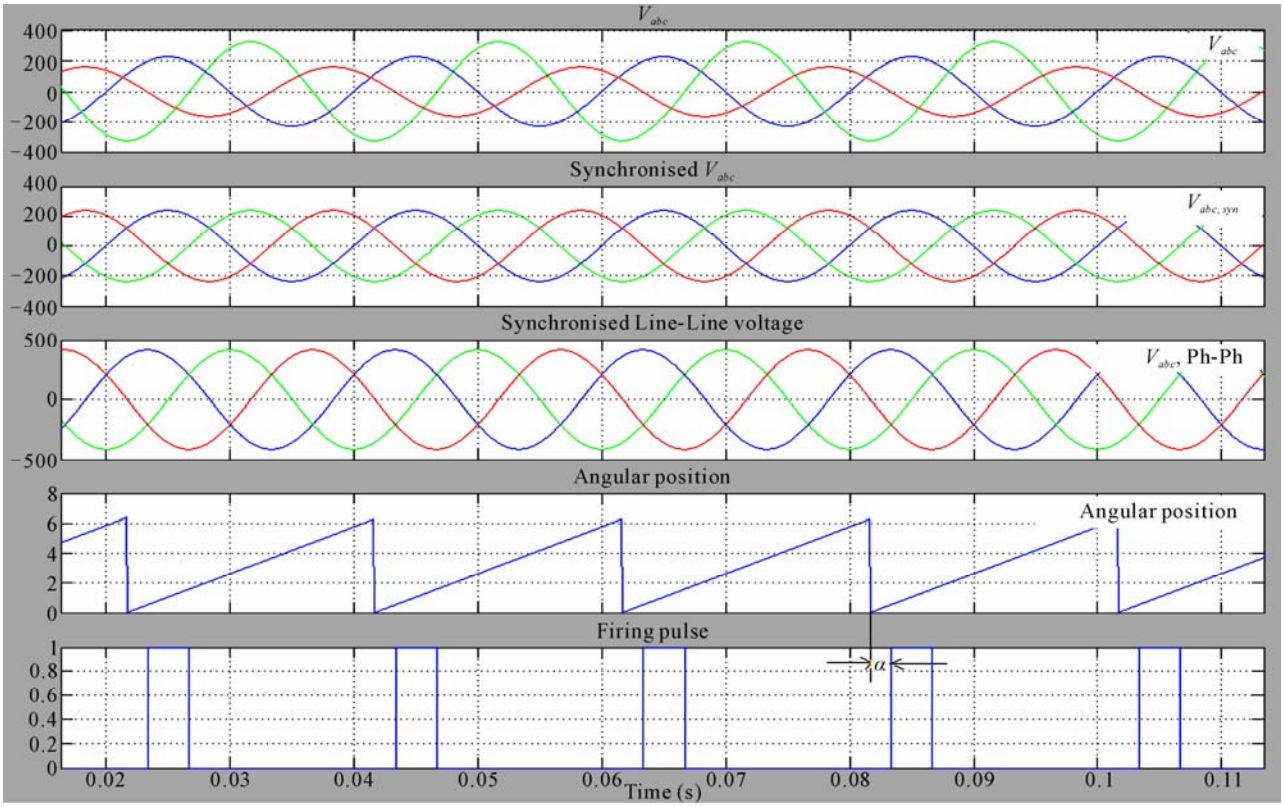

Figure 14. Results of proposed GFU for unbalance in V_{com}.

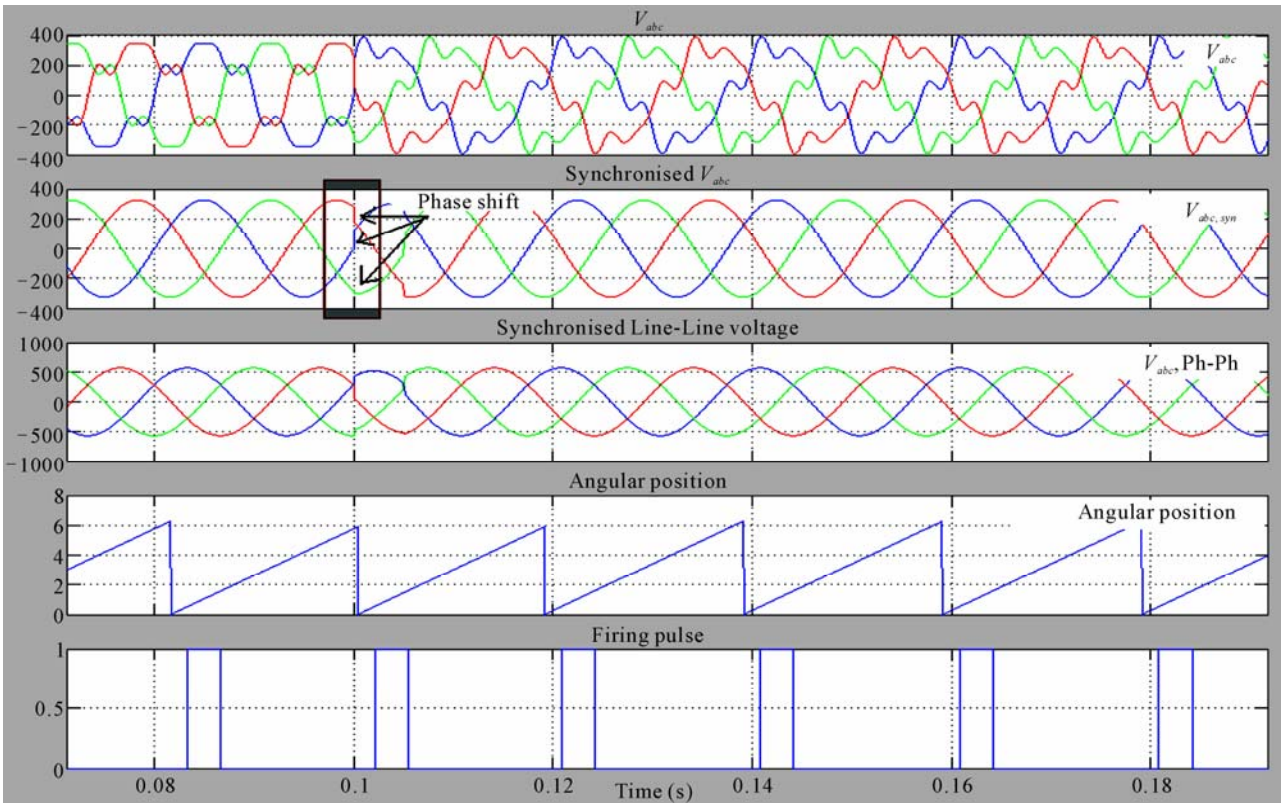

Figure 15. Results of proposed GFU for loss of V_{com} from 0.1 s to 0.2 s.

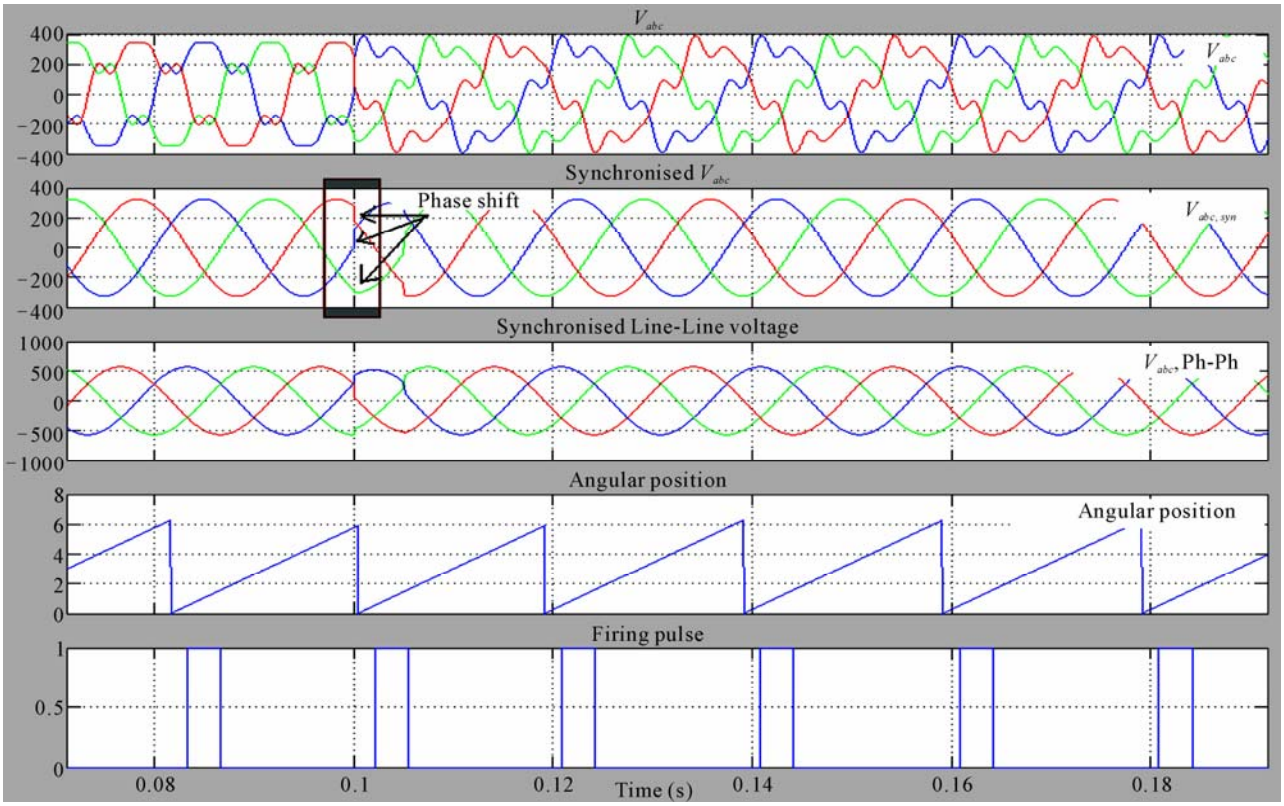

Figure 16. Results of proposed GFU for 45˚ phase jump in V_{com}.

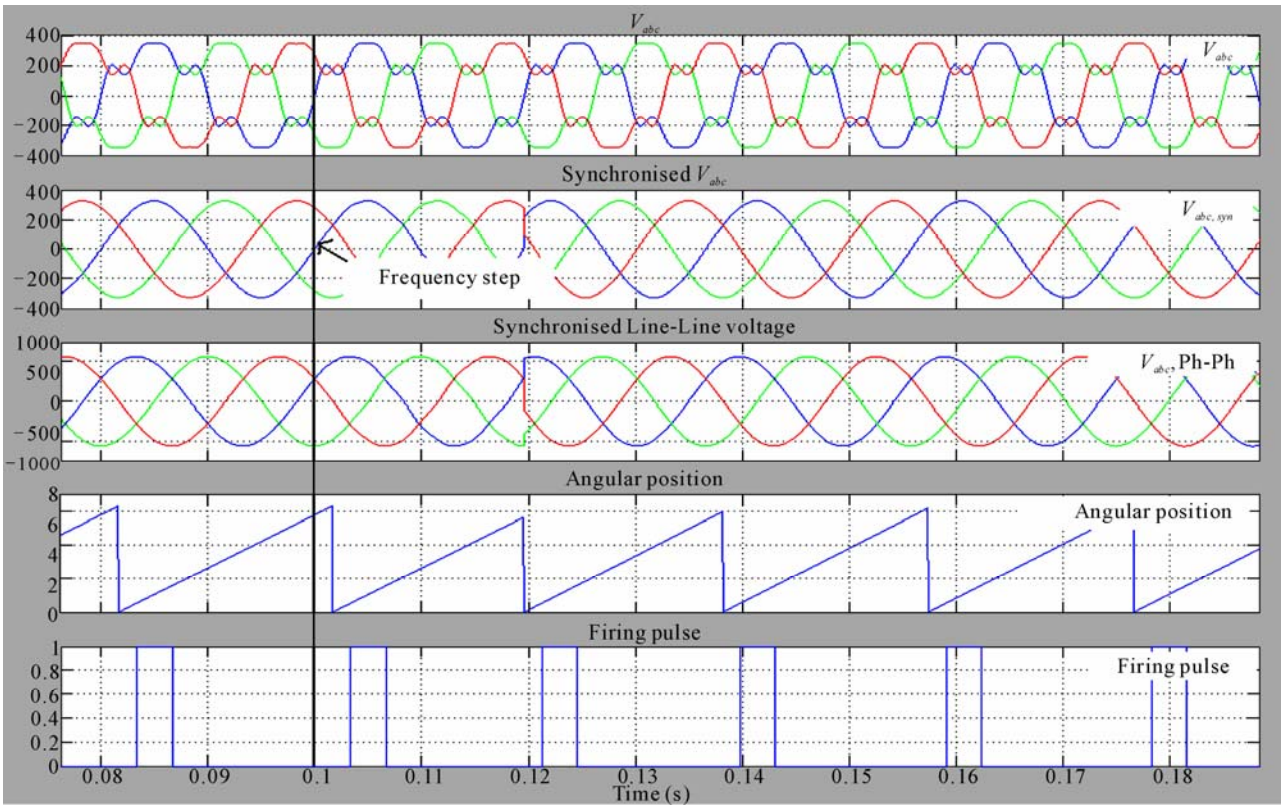

Figure 17. Results of proposed GFU for 1 Hz frequency jump in V_{com}.

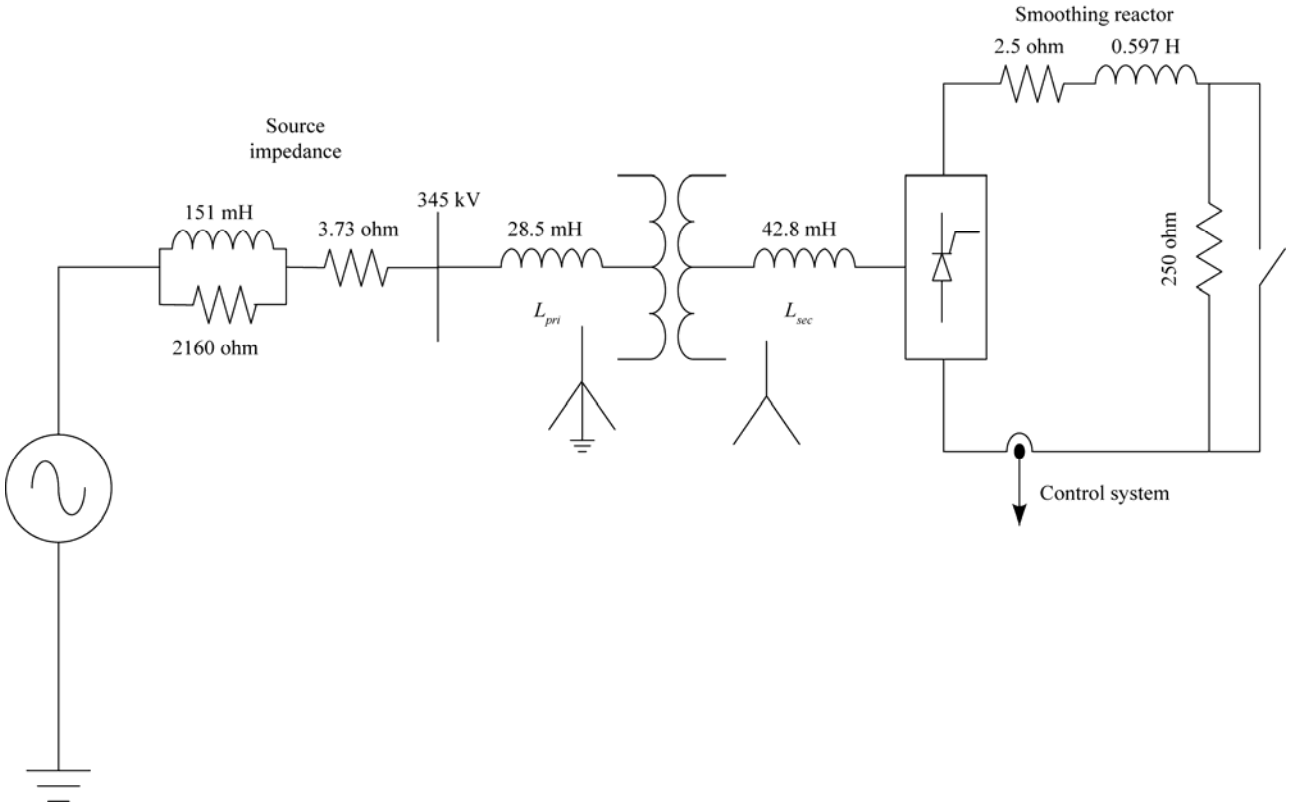

Figure 18. Rectifier system based on CIGRE Benchmark model.

4.1. System Start-up

Figure 19 shows: 1) line currents, 2) V_{dc}, 3) I_{dc}, 4) Thyristor S_1 firing pulse, 5) V_{sync}, 6) V_{com}.

The proposed GFU is designed to send the first firing pulse after 10 ms. From **Figure 19** it is seen that a clean V_{sync} is obtained after 5 ms and firing pulses are applied at the end of 10ms. For I_{dc} of 1 kA, $\alpha = 23.3^{\circ}$. It achieves full load at the end of 1 cycle.

4.2. 10% Change in Current Order

In **Figure 20**, it is seen that for a 10% step in current order from 900A to 990A, α changes from 40.1˚ to 25.3˚ within 20 ms.

4.3. Voltage Unbalance on AC Side

In **Figure 21**, a voltage unbalance applied from 0.4s to 0.5 s. During this time, a second harmonic component is seen in V_{dc} and Idc but a clean V_{sync} is still obtained. Clean V_{sync} under voltage unbalance is not possible with the trans-vector PLL. I_{dc} can be recovered to its rated value within 2-3 cycles.

4.4. DC Line Fault

A DC line fault is applied from 0.4 s to 0.42 s. The fault causes the dc voltage to become zero and current to rise more than 2000A. Even in such a situation a clean V_{sync} is obtained (**Figure 22**). The current controller brings I_{dc} back to 1000A within 3 cycles. No other controller such as Voltage Dependent Current Limits (VDCL) is used here.

4.5. 50% Voltage Sag on AC Side

Voltage sag of 50% is applied from 0.4s to 0.49s with open loop $\alpha = 23.3^{\circ}$ *i.e.* no current controller. This controller requires 10ms to come back to its original state after the voltage has recovered (**Figure 23**). Voltage sag does not produce any second harmonic component in I_{dc}. The closed loop response time depends on the DC current controller used. A simple PI current controller is used here for cases 4.1 to 4.4 whereas more advanced controller can even lessen the transient response time of the proposed controller.

Table 1 shows the comparison between the trans-vector type GFU [18] and proposed GFU.

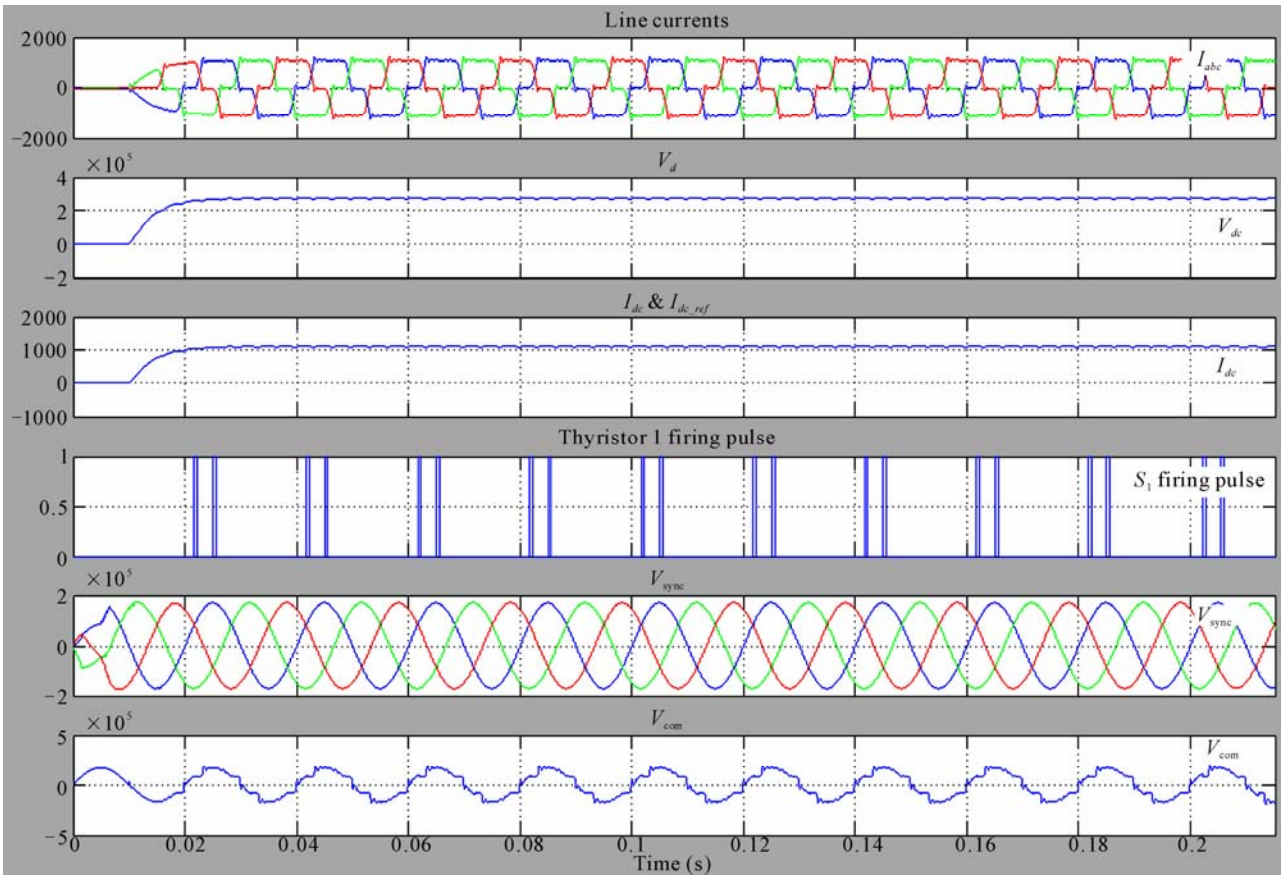

Figure 19. Initialization of system based on proposed GFU.

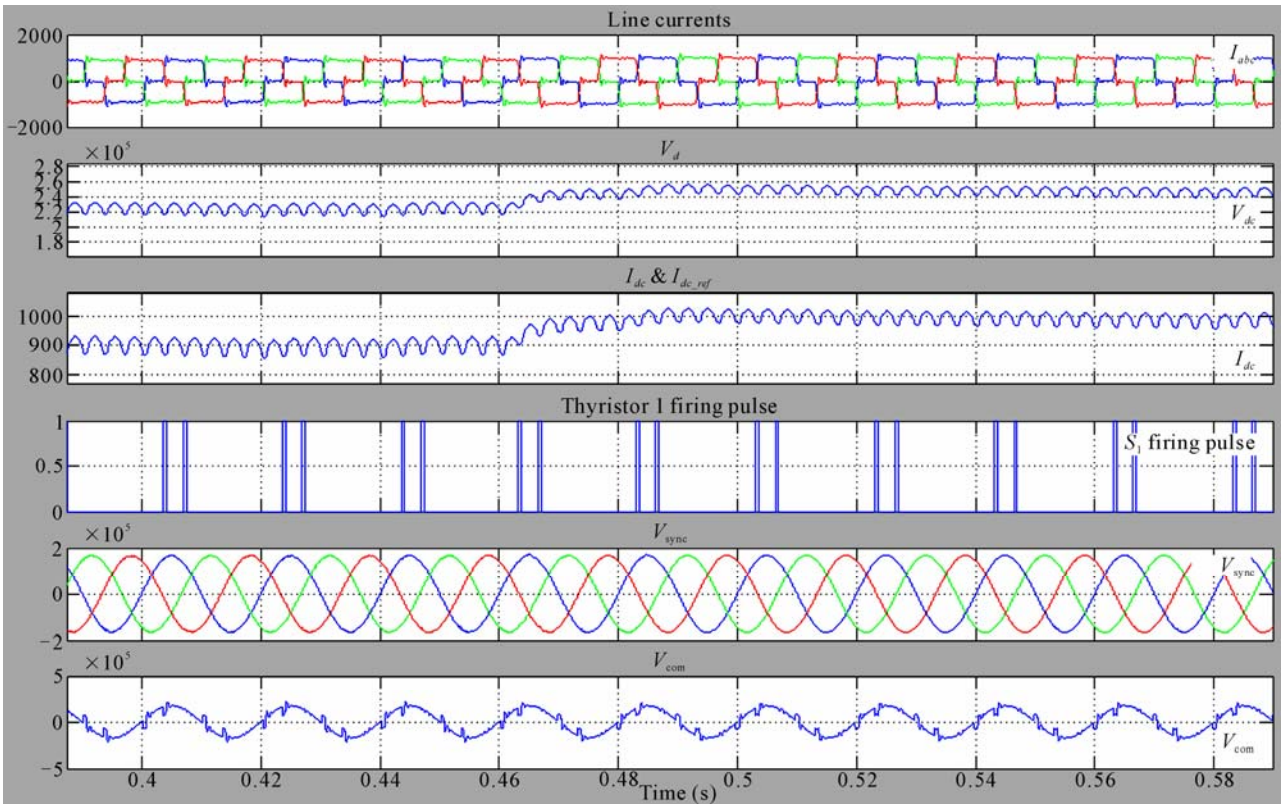

Figure 20. 10% current step change with proposed GFU.

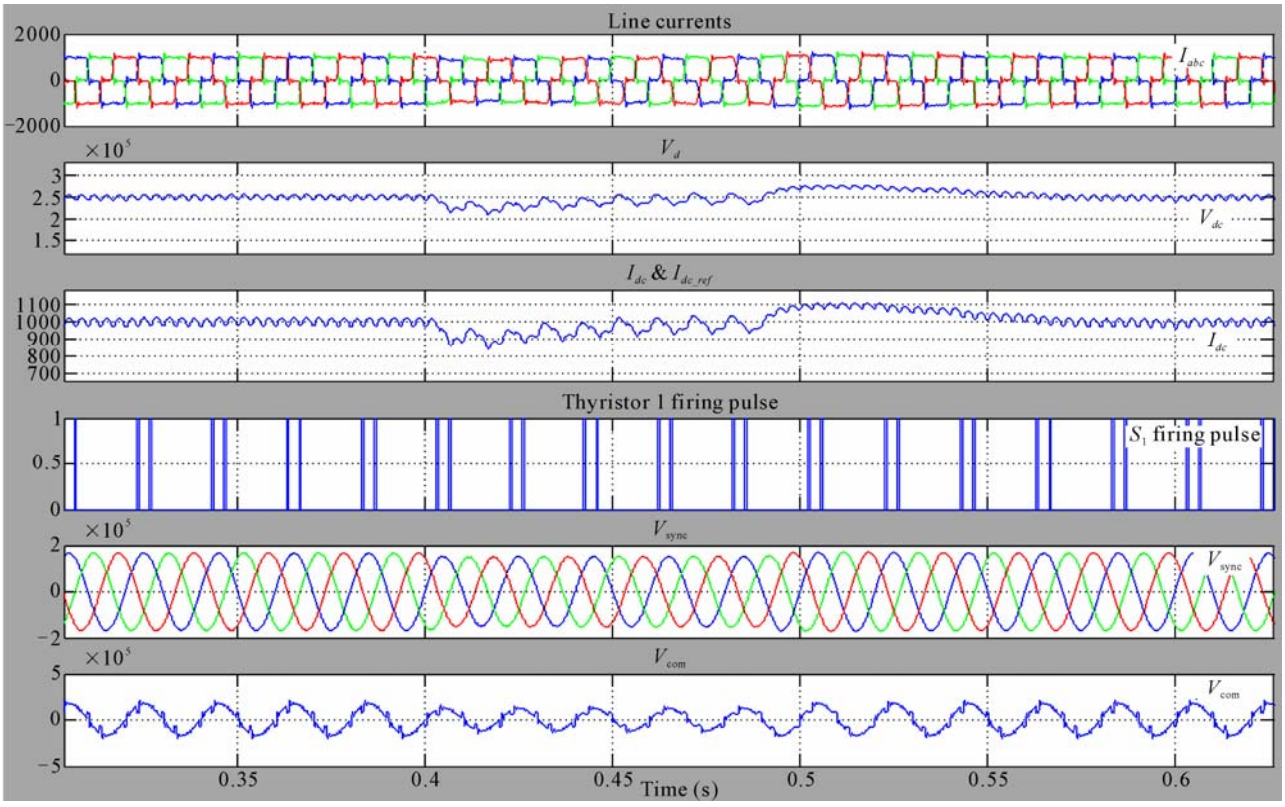

Figure 21. Voltage unbalance with proposed GFU.

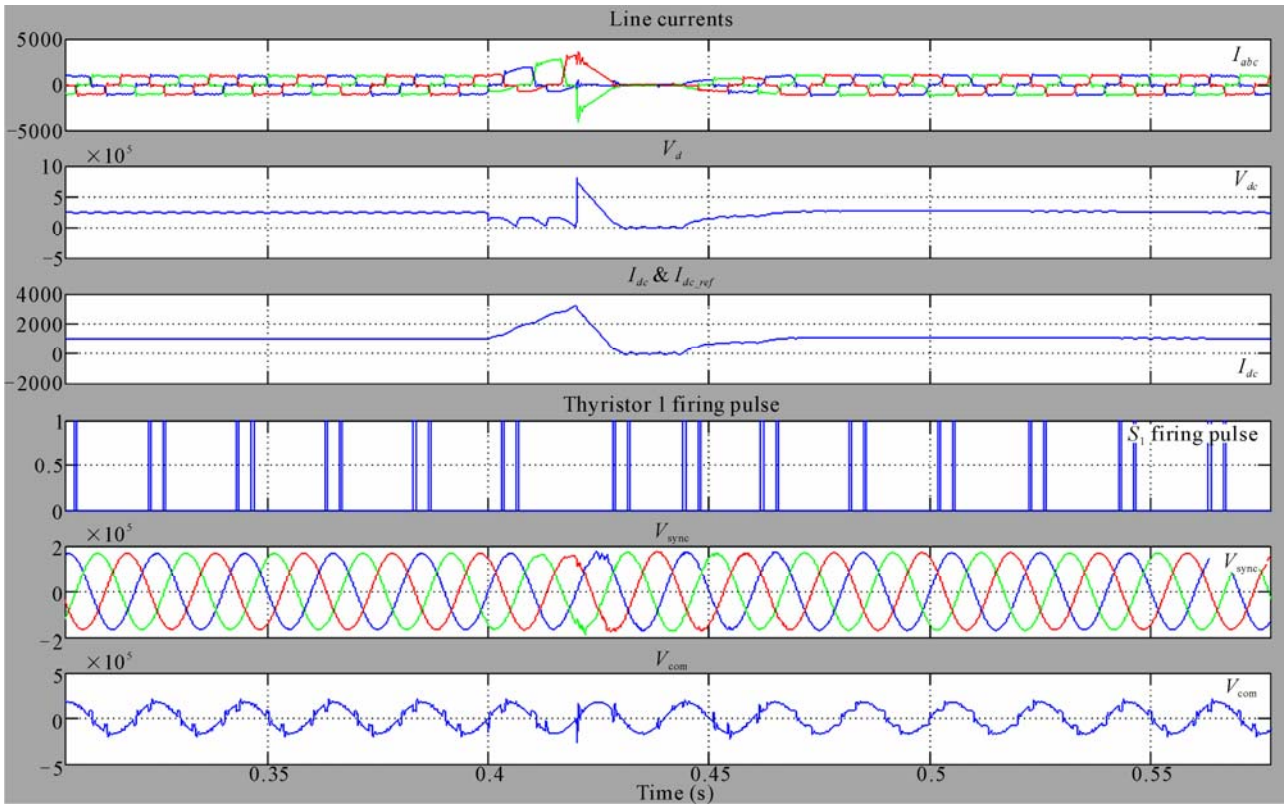

Figure 22. DC line fault with proposed GFU.

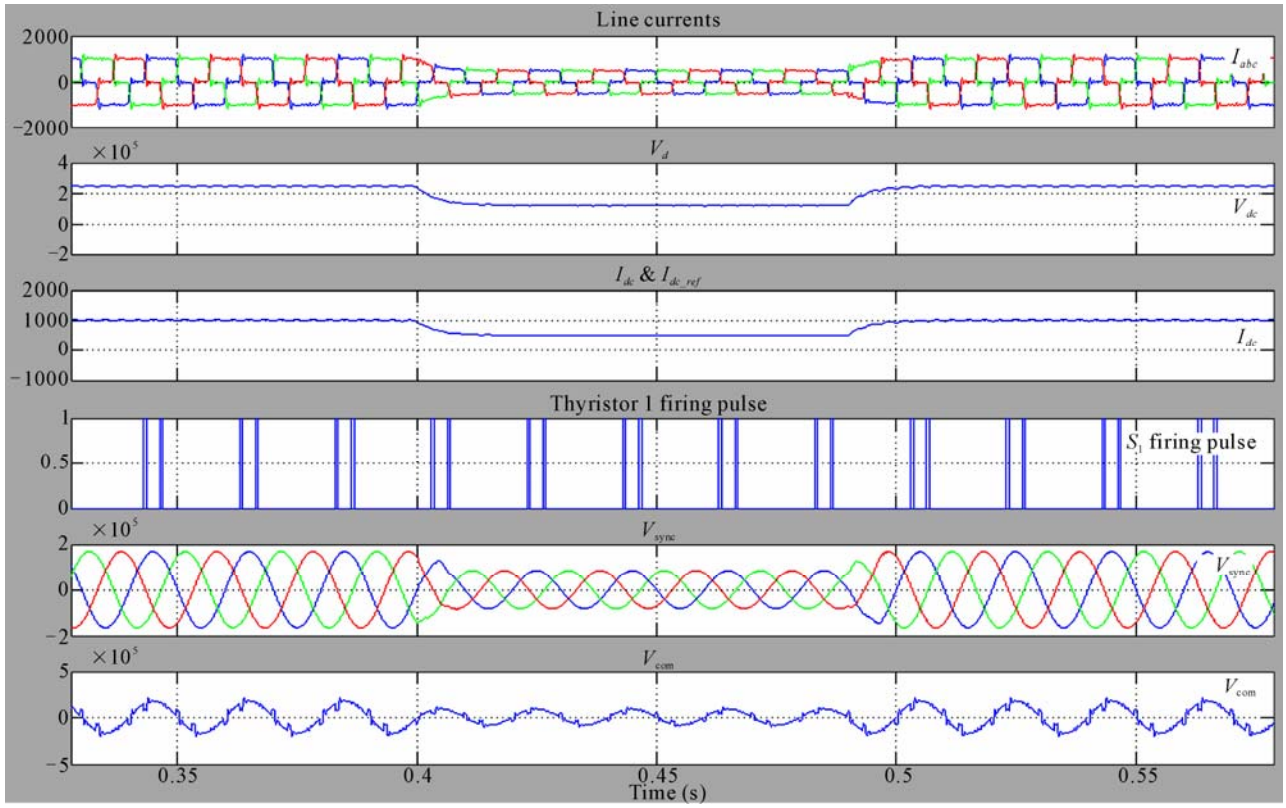

Figure 23. 50% voltage sag with proposed GFU.

Table 1. Shows the comparison with trans-vector type GFU.

Condition	Trans-vector	Proposed
Start-up	60 ms	20 ms
10% step change in I_{dc}	30 ms	20 ms
Voltage unbalance	100 ms	50 ms
DC line fault	80 ms	20 ms
Open loop start up	------	10 ms
Open loop voltage sag	------	10 ms

The GFU is immune to mains voltage unbalance, harmonics, voltage sag, phase jump, frequency variation etc. Also, there is no stability or tuning issue involved. Further, work in extending this to a complete HVDC system is planned.

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