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A Digital Phase Locked Loop Speed Control of Three Phase Induction Motor Drive: Performances Analysis

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Abstract

This paper deals with performance analysis and implementation of a three phase inverter fed induction motor (IM) drive system. The closed loop control scheme of the drive utilizes the Digital Phase Locked Loop (DPLL). The DPLL is safely implemented all around the well known integrated circuit DPLL 4046. An experimental verification is carried out on one kw scalar controlled IM system drives for a wide range of speeds and loads appliance. This presents a simple and high performance solution for industrial applications.

Keywords: Digital Phase Locked Loop (DPLL), Induction Motor, Scalar Strategy, Speed Drives and Load Appliance

1. Introduction

IMs are used in many industry sectors as the leading element to convert electrical energy into mechanical one. The main challenge is based on robustness and low cost. The performance of the motor speed control required in the industrial drives depends on the application specifications. In some applications, an open loop speed variation of the drive motor is enough. In others, feedback control is required for better speed regulation performances. The performances of the speed regulation depend on the performances of the speed controller. In light of available literature, important aspects of the motor drive system, it is considered worthwhile to review it critically in order to find the gaps existing knowledge on the IM drive systems. Researchers have used various types of closed loop controllers for the IM rotor speed. PI controllers are widely and still used in the outer speed loop [1,2]. They have a simple structure and can offer a satisfactory performance for a wide range of operation. Due to the continuous variation in the plant parameters and the non linearities conditions, PI controllers may become unable to provide the required control performance [3,4]. These inherent disadvantages of the PI controllers have encouraged the replacement of this controller with adaptive [5,6] and robust [7-9] control laws. Adaptive control laws impose a very computation burden while H∞ robust control requires the knowledge of the disturbances boundaries [7]. Sliding mode control is also used in the speed loop [10]. Chattering in the steady state is the main drawback of this strategy [11,12]. Recently, speed controllers based on artificial intelligence techniques such as fuzzy logic and neural networks based controllers have been proposed [13,14]. Since these approaches do not rely on any detailed mathematical plant, the algorithm would remain robust despite of parameter deviations and noise measurement [15,16]. However, the computation expenses and the requirement of expert knowledge for the system setup have seriously restricted their applications in practice. In [17], an internal model controller (IMC) is developed for a scalar controlled IM feedback. This IMC controller has the advantage of robustness, ease of design and good responses. In some applications, a precise speed is required. Excellent speed regulation can be achieved with a DPLL. In [18], Moore found that this technique has significant ability to obtain precise speed regulation. When the feedback signal of the IM speed is synchronized with a reference signal, perfect signal speed regulation can be realized about 0.02% to 0.1% of the steady state accuracy which is difficult to obtain by conventional closed loop system. In the research work carried out in [19], the speed control of a three phase squirrel cage IM fed by employing triacs devices in the lines is described. The speed closed loop regulation of the system is then investigated by employing DPLL scheme. In [20], the study of the speed control of the IM drive using DPLL is discussed. The IM is fed with thyristors power inverter. In this, the DPLL is es-

tablished using digital and analog circuits. In [21], the authors have developed an inverter fed IM drive using the PLL speed controller. While more literature has been discussing the design of such control loop, very few articles show the experimental results obtained at a specific target speed under a particular load appliance and none of these articles studies the PLL performance under a wide range of speeds and loads. Therefore, the aim of this paper is to highlight the high performance of the DPLL in experimentation for a wide range of speeds and shaft load appliance.

2. Basic of PLL IM

PLL is a feedback loop where a voltage controlled oscillator can be automatically synchronize to a periodic input signal [22-24]. The basic PLL has three components connected in a feedback loop [25-27] as shown in the block diagram of **Figure 1**: a voltage controlled oscillator (VCO), a phase detector (PD) and a low pass filter (LPF).

The VCO is an oscillator whose frequency f_{osc} is proportional to input voltage. The voltage at the input of the VCO determines the frequency of the periodic signal at its output. The VCO output and a periodic input signal (the reference) are inputs to the phase detector. When the loop is locked on the input signal, the frequency of the VCO output is exactly equal to that of a reference. It is also said that the PLL is in the locked condition. PD produces a signal proportional to the phase difference between the reference signal and the VCO output signal. The output of the PD is altered through a low pass filter. The loop is closed by connecting the filter output to the input of the VCO. The output voltage of the filter is used to control the VCO frequency. A PLL basic property is that it attempts to maintain the frequency lock between the VCO output and reference signal even if the frequency of the input signal varies in time [26]. Suppose that the PLL is in the locked condition, and that the frequency of the incoming signal increases slightly. The phase difference between the VCO signal and the incoming signal will begin to increase in time. As a result, the filter output voltage increases, and the VCO output frequency increases until it matches the reference frequency, thus keeping the PLL in the locked condition. The range of frequencies from minimal to maximal values where the locked PLL remains in the locked condition is called the lock range of the PLL [25-26]. If the PLL is initially locked, and input signal frequency becomes smaller than f_{min} or if input signal frequency exceeds f_{max}, the PLL fails to keep the VCO frequency equal to input signal one and the PLL becomes unlocked. When the PLL is unlocked, the VCO oscillates at the

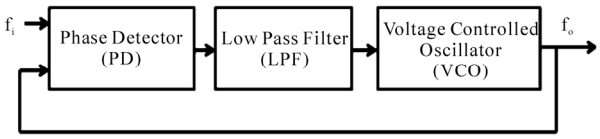

Figure 1. Bloc diagram of the PLL.

frequency fo called the center frequency, or the VCO free-running frequency. The lock can be established again if the incoming signal frequency gets close enough to f_o. The range of frequencies $f_i = f_o - f_c$ to $f_i = f_o + f_c$ such that the initially unlocked PLL becomes locked is called the capture range of the PLL [24]. The capture range 2fc depends on the characteristic of the loop filter [25]. For the used filter, an approximate implicit expression for the capture range can be founded as:

$$fc \cong \frac{VDD}{2}\frac{K_0}{\sqrt{1+\left(\frac{f_c}{f_p}\right)^2}} \tag{1}$$

If the capture range is much larger than the cut off frequency of the filter, $f_c f_p^{-1} > 1$, the expression for the capture range is simplified as:

$$2\,fc \cong \sqrt{2V_{DD}K_0 f_p} \tag{2}$$

K_0 is the VCO gain or the frequency sensitivity.

Thanks to the rapid development of technology, the PLL is implemented using the integrated circuit systems. The most used integrated circuit is the well known 4046 chip [23].

3. System Configuration of the Drive System and Experimental Results

The overall system block diagram of 4046 PLL IM speed control is given in **Figure 2**. This system is roughly classified into two parts: the control and the power parts. The control part is consisting mainly of 4046 PLL and a scalar control unit. A simple positive supply voltage is needed for the chip. The positive supply voltage VDD is connected to pin 16 and the ground is connected to pin 8. The reference square wave signal goes to the input of an internal amplifier at the pin 14 of the chip. The reference signal must be a square wave with a 50% duty cycle. Therefore, to obtain this target signal, a direct voltage is fed to pin 9 (the input of the 4046 VCO) to give at its output (pin 4), a square wave signal representing the target rotor speed. The VCO requires one external capacitor C_1 and one or two external resistors (R_1 or R_1 and R_2). Resistor R_1 and capacitor C_1 determine the frequency range of the VCO and resistor R_2 enables the VCO to have a frequency offset if required. The output motor

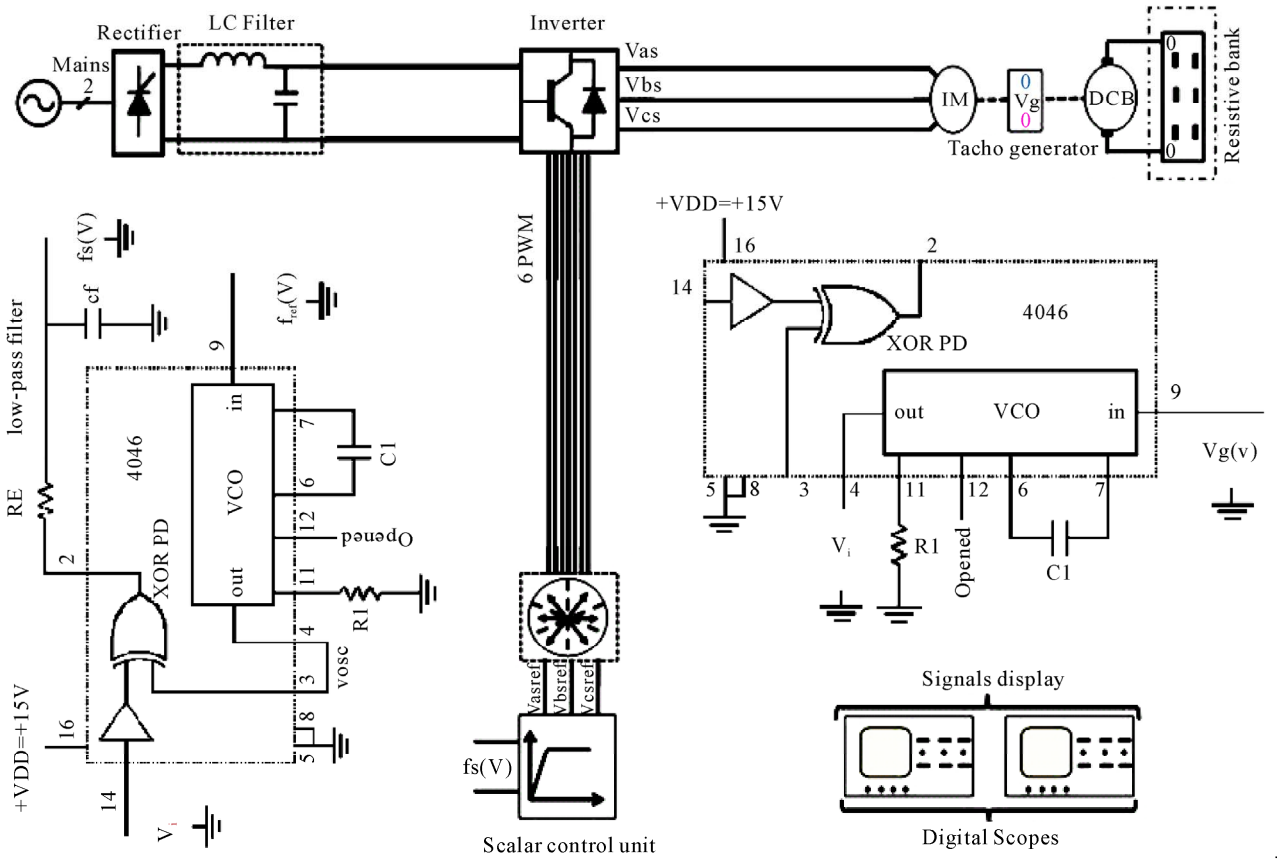

Figure 2. Bloc diagram of the DPLL IM speed control.

speed is sensed by a tacho generator. The motor speed in square waveform is needed. A second 4046 is added and the motor speed in square waveform is received at its VCO output. The obtained signal is feedback at pin 3 and compared to the target frequency received at pin 4 by the phase detector (PD) [27]. The used PD in this application is the comparator I of 4046. It is simply XOR logic gate with logic down output when the two inputs are either high or both low and the logic up otherwise. The PD output is proportional to the phase error between two inputs [25-27]. The obtained PD output is then filtered by an external low pass filter [27]. The obtained filtered voltage is proportional to the synchronous (stator supply) frequency which feeds the scalar control unit. The investigated DPLL IM speed regulation is built and tested using a 1kw — 2.65 A squirrel cage IM. **Figure 3** shows the experimental set up drive system of the hardware configuration. The IM is powered by an insulated gate bipolar transistor (IGBT) voltage source inverter (VSI). It utilizes a thyristor rectifier as a dc bus voltage link. The pulse width modulation (PWM) signals to control the power modules are generated by the scalar control card equipped with a digital processor. A tacho generator delivering 1v for 1000 rpm is mounted on the rotor shaft to measure the rotor speed. The DPLL is built around the 4046 integrated circuit system. A DC generator (1 kw - 6.2 A) is coupled with the IM which feeds the resistor bank used as a load. Investigated system is tested for various ranges of target rotor speeds under various range of loads. For each test, the rotor speeds, waveforms of real and target speeds and the output of the LPF as control signal are together illustrated. Obtained experimental results are given in **Figures 4** to **18**. Excellent steady state frequency has been obtained especially at high and low speeds proving the high performances of the rotor speed regulation using the DPLL. At no load, excellent steady state speed regulation is obtained. At a time of load appliance, the square root of the stator phase current in creases to compensate the effect of the load appliance. Thus, the square root of stator phase voltage decreases due the voltage drop caused by the stator resistance. The fact that decreases the rotor speed. As, the PLL is in the locked condition, and that the frequency of the incoming signal decreases slightly. The phase difference between the VCO signal and the incoming signal will begin to increase in time. As a result, the filter output voltage increases, and the VCO output frequency increases until it matches the reference frequency, thus keeping the PLL

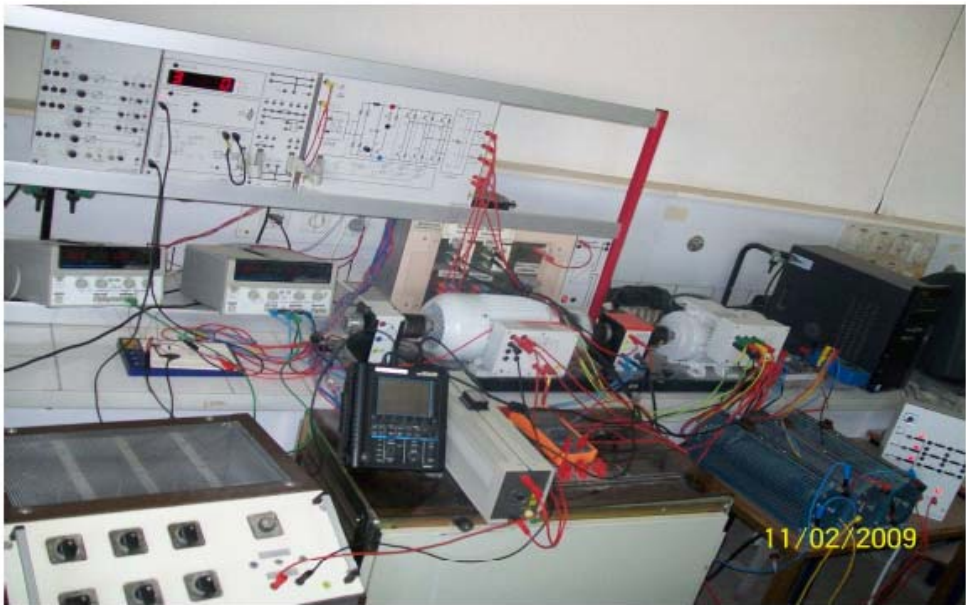

Figure 3. A photo of the experimental set up.

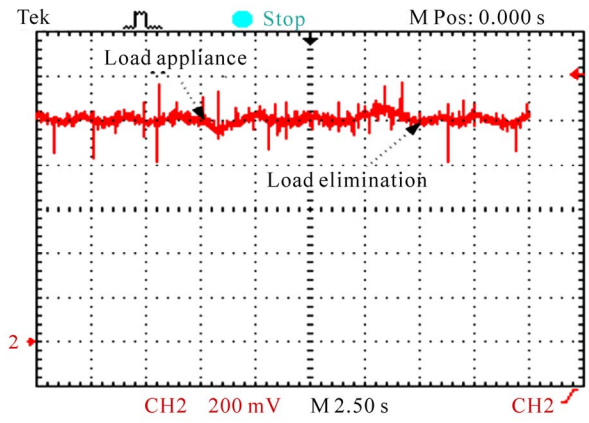

Figure 4. IM speed for a 1000rpm target speed under load appliance of 35% of its rated value.

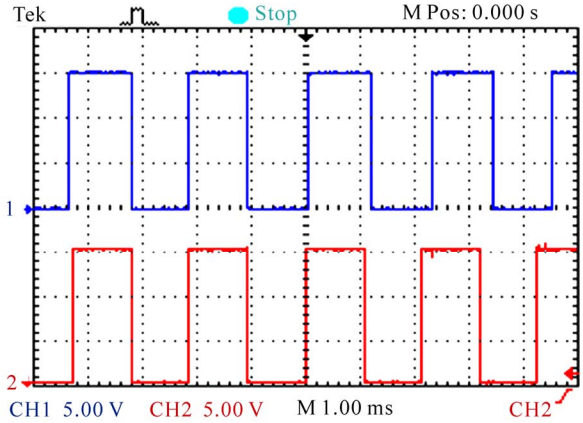

Figure 6. IM speed for a 1000rpm target speed under load appliance of 35% of its rated value.

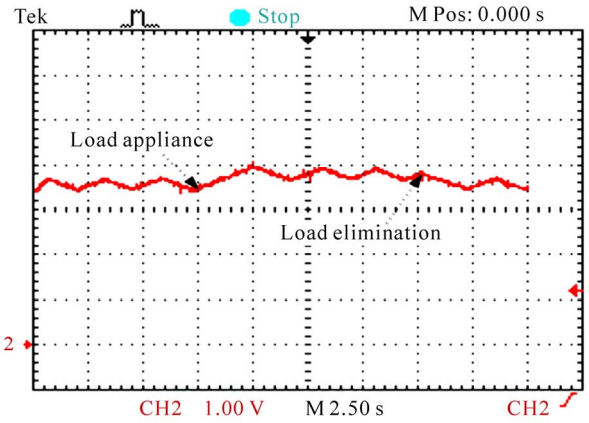

Figure 5. Control law for a 1000rpm target speed under load appliance of 35% of its rated value.

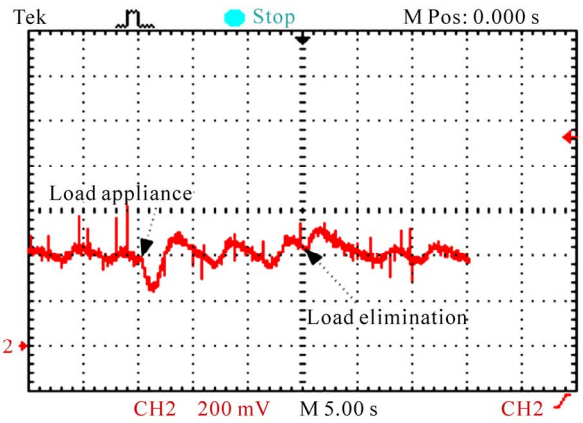

Figure 7. IM speed for a 400rpm target speed under load appliance of 40% of its rated value.

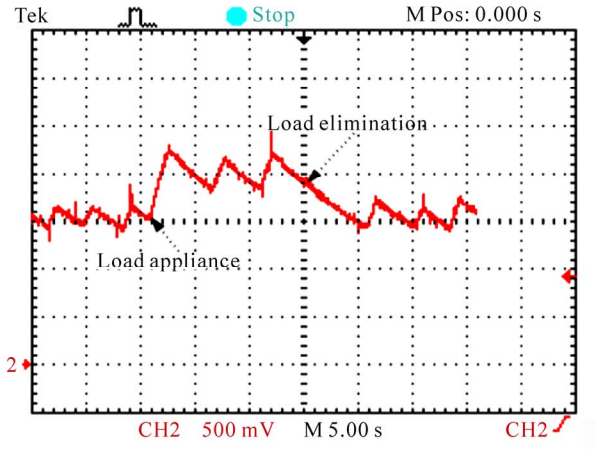

Figure 8. Real and target square waveforms for a 1000rpm target speed under load appliance of 40% of its rated value.

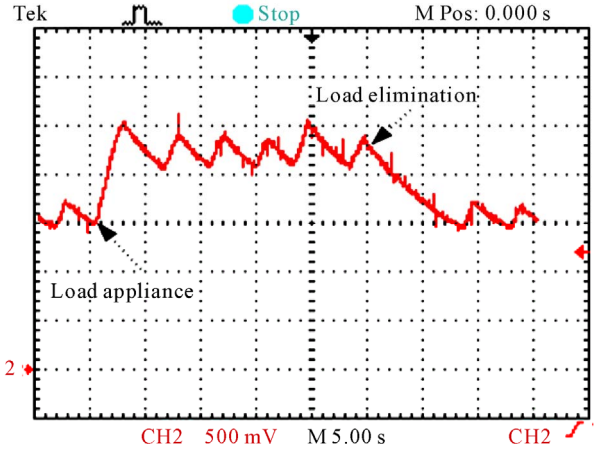

Figure 11. Control law for a 400rpm target speed under load appliance of 50% of its rated value.

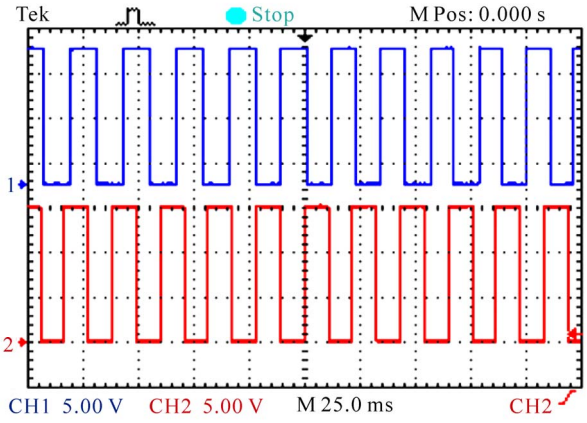

Figure 9. Real and target square waveforms for a 400rpm target speed under load appliance of 40% of its rated value.

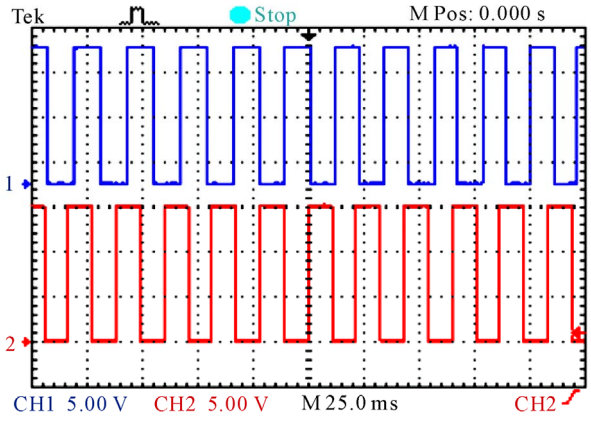

Figure 12. Real and target square waveforms for a 400rpm target speed under load appliance of 50% of its rated value.

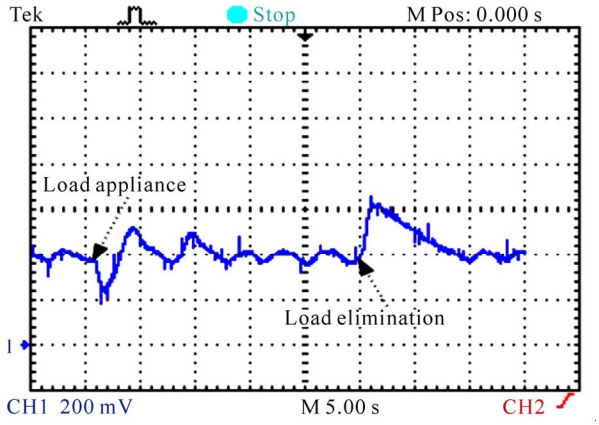

Figure 10. IM speed for a 400rpm target speed under load appliance of 50% of its rated value.

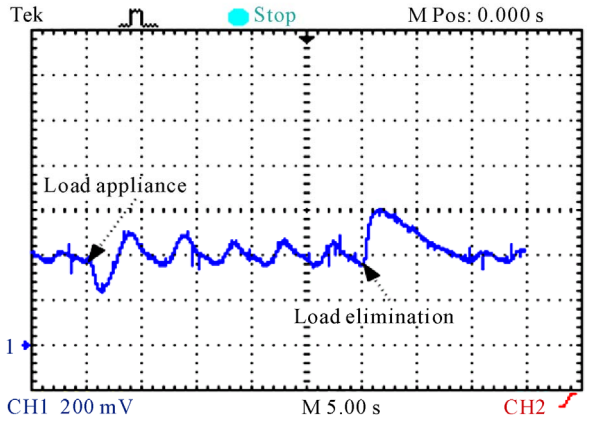

Figure 13. IM speed for a 400rpm target speed under load appliance of 60% of its rated value.

in the locked condition. As, it is illustrated by the obtained experimental results under load appliance. At a time of load elimination, the square root of the stator phase current decreases. Thus, the square root of stator phase voltage increases. The fact that increases the rotor speed. As, the PLL is in the locked condition, and that

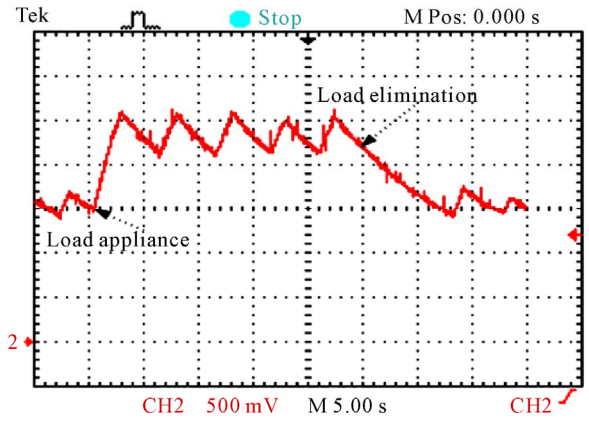

Figure 14. Control law for a 400rpm target speed under load appliance of 60% of its rated value.

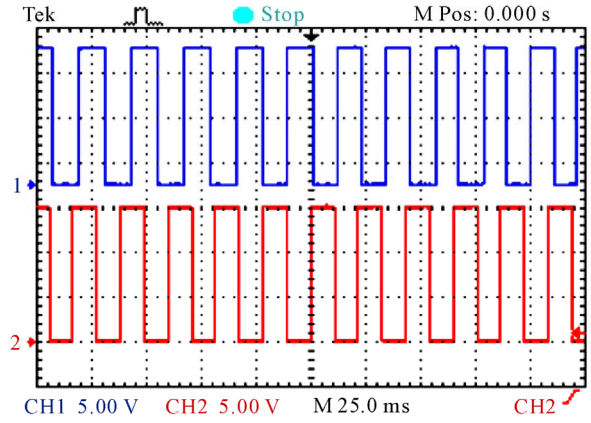

Figure 15. Real and square waveforms for a 400rpm target speed under load appliance of 60% of its rated value.

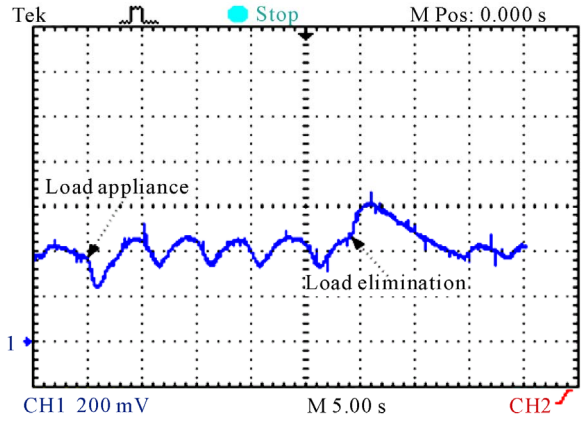

Figure 16. IM speed for a 400rpm target frequency under load appliance of 65% of its rated value.

the frequency of the incoming signal increases slightly. The phase difference between the VCO signal and the incoming signal will begin to decrease in time. As a result, the filter output voltage decreases, and the VCO

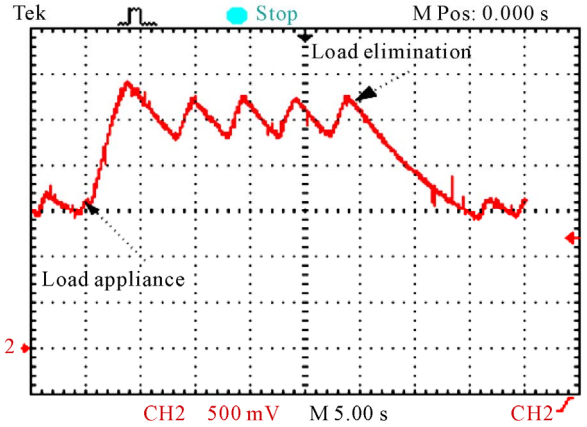

Figure 17. Control law for a 400rpm target speed under load appliance of 65% of its rated value.

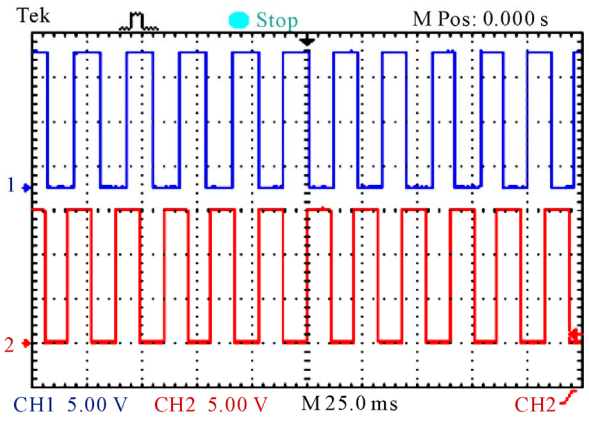

Figure 18. Real and target square waveforms for a 400rpm target speed under load appliance of 65% of its rated value.

output frequency decreases until it matches the reference frequency, thus keeping the PLL in the locked condition. As, it is illustrated by the obtained experimental results under load elimination. The digital scope screen images are illustrating the frequencies and speeds signals which are calibrated as follow: 1v for 1000rpm.

4. Conclusion

In this paper, an experimental set up DPLL IM speed controller is designed and achieved. The overall system with three phase 1kw squirrel cage IM has been designed and tested in the laboratory over the entire range of speeds and loads. Obtained experimental results show that a precise speed regulation is achieved at steady state. Compared with the other control laws, the present scheme is in somewhat simpler, cheaper and provides speed control with high precision. All high performances scalar controlled IM drives require accurate rotational speed information for feedback control. This information

is mainly provided by tackogenerator. The use of this sensor implies more electronics and high cost. To overcome these problems, a speed observer can be included in the control loop. Thanks to high performance of the PLL technique, it can be used to reconstruct the IM speed. The PLL sensorless novel scalar strategy IM speed controller will be the subject for a follow up further studies.

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