

# Multi-Bias Model for Power Diode Using a Very High Description Language

Hassene Mnif, Montassar Najari, Hekmet Samet, Nouri Masmoudi

National School of Engineering of Sfax, LETI Laboratory, Sfax, Tunisia

E-mail: [hassene.mnif@isecs.rnu.tn](mailto:hassene.mnif@isecs.rnu.tn)

Received May 3, 2010; revised June 12, 2010; accepted July 16, 2010

## Abstract

This study focused on the determination and analysis of an accurate analytical model for PIN diode under different bias conditions. This approach employs analytically derived expressions including the variation of the depletion regions in the device to make the used model available over a wide range of testing conditions without remake the parameters extraction procedure. The validity of the proposed extraction procedure has been verified by the very good agreement between simulated and measured current and voltage waveforms reverse recovery at different range of the operation conditions. The model is developed and simulated with the VHDL-AMS language under Ansoft Simplorer® Environment.

**Keywords:** Power PIN Diode, VHDL-AMS, Modeling, High Injection, Parameter Extraction

## 1. Introduction

Design of integrated power systems requires prototype-less approaches. Accurate simulations are necessary for analysis and verification purposes. Simulation relies on component models and associated parameters.

Most of the power PIN diode models provided by the literature are not valid for a mutli-bias simulation because of their limitation to accurately describe the device's physical rules.

One of these physical limitations can be due to supposing a fixed depletion region width which is the case of several studies [1]. In [2], the power PIN diode model includes three empirical and non physical equations to escape the extraction procedure when using the model for multi-bias conditions.

In this study, the developed power PIN diode model supposes that the width of the intrinsic bulk region is a function of reverse applied voltage as it's reported by Neudeck and Streetman [3].

Our study is structured as follows. In Section 2, a detailed presentation of a new moving boundary diffusion model for the power PIN diodes is made. Section 3 treats the test bench circuit and demonstrates a first comparison with experimental data. Section 4 investigates on the influence of the parasitic inductance in simulation result and the improvement of simulated test circuit by the correction of this parasitic inductance value. Finally, Section 6 gives some conclusions and future study.

All the operations (implementation, extraction, optimization ...) are made under the free mixed signal simulator "Simplorer-sv 7.0" by Ansoft®.

## 2. PIN Diode Model Description

As it is reported in [2], the model is formulated for a  $P^+IN^+$  type diode based on the Lauritzen power diode model [1]. Lauritzen and Al.'s model is based on a systematic technique for analytical modeling; the lumped-charge modeling technique (LC) developed by Linvill [4].

Figure 1 shows the charge distribution in a conducting pin diode under forward conduction.

The charge distribution in the i-region is assigned to four charge storage nodes following the lumped model approach developed by Linvill [4] with:

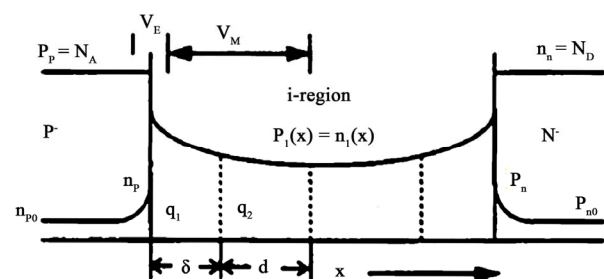


Figure 1. Charge distribution profile in diode forward conduction [1].

- In the left node:
  - $q_1$  is the total charge
  - $p_1$  is the average hole concentration
  - $\delta$  is the respective width
- In the adjacent node:
  - $q_2$  is the total charge
  - $p_2$  is the average hole concentration
  - $d$  is the respective width

**Table 1** summarizes the complete set of “Lauritzen” and Al.’s model equations [1], collected together in a simple and consistent form.

More information about the original model can be found on [1].

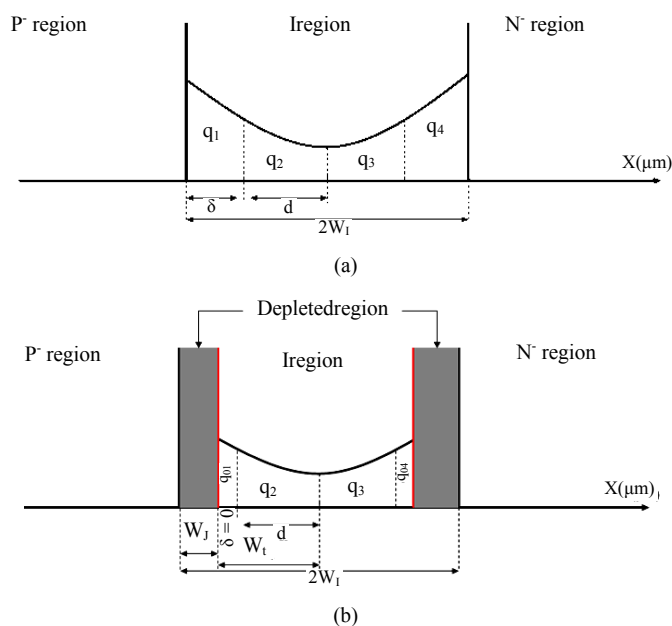
By seeing this previous set of equations, one can clearly remark that there is no variation of the special dimensions of depletion regions in the device.

So, by considering the fact that the width of the intrinsic bulk region reduces significantly during the reverse biased condition, more accurate simulation results for reverse recovery current and voltage can be found.

An improvement was made in [2], which consists of introducing some empirical equations. In this study the developed PIN diode model considers the variation of depletion regions width in the  $p^+i$  and  $i-n^+$  junctions as depicted in **Figure 2**.

**Table 1. Lauritzen model’s equations [1].**

Equation form	Description	Observations	Number
$i_M(t) = \frac{q_E - q_M}{T_M}$	$i_M(t)$ : Diode current with time dependency.	-----	(1)
$q_E = I_s \tau \left[ \exp\left(\frac{V_E}{V_T}\right) - 1 \right]$	$q_E$ : Injected charge level at both the $p^+i$ junction and $n^+i$ junction	$q_E = 2q_0$ with $q_0$ represents the variable remaining after $\delta \rightarrow 0$	(2)
$i_E = I_{SE} \left[ \exp\left(\frac{2V_E}{V_T}\right) - 1 \right]$	$i_E$ : End region recombination current	Occurs at very high current level	(3)
$\frac{dq_M}{dt} + \frac{q_M}{\tau} - \frac{(q_E - q_M)}{2T_M} = 0$	$q_M$ : Total charge in the $i$ -region	$q_M = 2q_E$ ; analysis made to only half of the structure	(4)
$v_M = \frac{V_T T_M R_{M0} i}{q_M R_{M0} + V_T T_M}$	$v_M$ : Voltage across half of the $i$ -region	-----	(5)
$v = 2v_E + 2v_M + R_S i$	$V$ : Total diode voltage	Kirchoff voltage law	(6)
$i = i_E + i_M + \frac{dq_C}{dt}$	$I$ : Total diode current	Kirchoff current law with $q_C = \int C_j d(2v_E)$ is the total charge in the capacitor	(7)



**Figure 2. Improved charge distribution profile in diode forward conduction: (a) static depletion region width; (b) dynamic depletion region width.**

### 3. A Moving Boundary Diffusion Model

In fact, by applying a reverse potential and due to the asymmetrically doped junction, the junction region extends primarily into the less doped intrinsic side. The half width of the dynamic intrinsic bulk region  $W_t$  can be calculated as:

$$W_t = W_i - W_j \tag{8}$$

in which  $W_i$  is the half physical intrinsic region.

Unlike the low injection phenomenon, the junction-depletion width  $W_j$  variation effects under the high injection phenomenon can be written as [5]:

$$W_j = \left( \frac{2\epsilon_s (V_{bi} - V_A)}{q \left( N_i + \frac{|i_{diode}|}{qAV_{sat}} \right)} \right)^{1/2} \tag{9}$$

where:

- $\epsilon_s$  = The silicon permittivity;
- $N_i$  = The doping level of the bulk region;
- $q$  = The electron charge;
- $V_{bi}, V_A$  = Respectively the built-in potential and the applied voltage to the junction;
- $i_{diode}$  = The total current under the device;
- $A$  = The device active area;
- $v_{sat}$  = The carrier saturation velocity.

By adding this new concept to Najjari's and Al. Model [2], many parameters, especially the carrier transit time, will be affected and it's crucial to investigate on this.

**Transit time  $T_M$ :** As it's reported in **Table 1**, to calculate the diode current due to carriers injected to the i-region by the two junctions, *i.e.*  $p^+/i$  and  $i/n^+$  junctions, the carrier transit time must be defined. So, by varying the depletion region width in the power PIN diode model with respect to the two (8) and (9), the carrier transit time  $T_M$  will be varied and the following equation is crucial for establishing this relation:

$$T_M = \frac{(W_t)^2}{4D_a} \tag{10}$$

with  $D_a$  is the ambipolar diffusion constant defined by:

$$D_a = 2 \frac{\mu_n \mu_p}{\mu_n + \mu_p} U_T \tag{11}$$

So, the set of equations in **Table 1** will be affected by this new concept and this variation of the depletion region with respect to the applied bias on the device will be considered in our new formulation of the power diode model.

In addition to the nine classical Lauritzen and Al.'s model parameters ( $\tau, T_M, I_{SE}, I_S, C_{j0}, R_S, m, \Phi_B$  and  $R_{M0}$ ), three new parameters describing the moving boundary effect are added, *i.e.* ( $W_i, N_i$  and  $\tau_{tr}$ ). The new improved

model has the following VHDL-AMS structure, **Figure 3**.

### 4. New Model's Parameters Discussion

In this section, an investigation about the new model parameters ( $W_i, N_i$  and  $\tau_{tr}$ ) influence will be done.

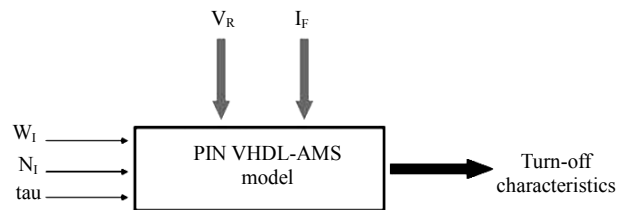
After writing the VHDL-AMS code for this power PIN diode model, the device is simulated under the circuit simulator Simplorer from Ansoft.

The same switching cell used in [2] is considered like it's shown in **Figure 4**.

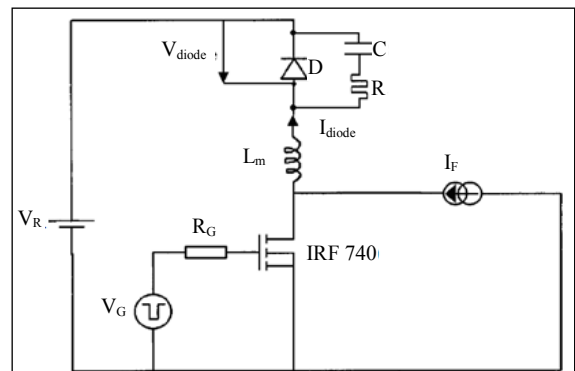
The switching cell main operating conditions are the forward current  $I_F$  and the reverse voltage  $V_R$ . These conditions are imposed by a current and a voltage source respectively. The "IRF740" transistor is a fast NMOS type. The parasitic inductance  $L_m$  has to be estimated carefully since it controls the current rate to some extent. In Section 4, we will discuss how to fix the value of this parasitic capacitance in the right way.

In order to avoid damaging the device, generally, due to the voltage overshoot, a RC-snubber was placed in parallel with the diode. Because of the small values of the snubber resistance and capacitance, the variation in component values with respect to temperature change could be neglected in so far as these variations might alter the diode switching waveforms [6].

Since the diode turn-off behavior is of more concern to engineers than the turn-on because of the important energy losses, only the experimental results for diode turn-off are performed.



**Figure 3.** New VHDL-AMS power PIN diode structure.



**Figure 4.** Principal circuit for the measurements.

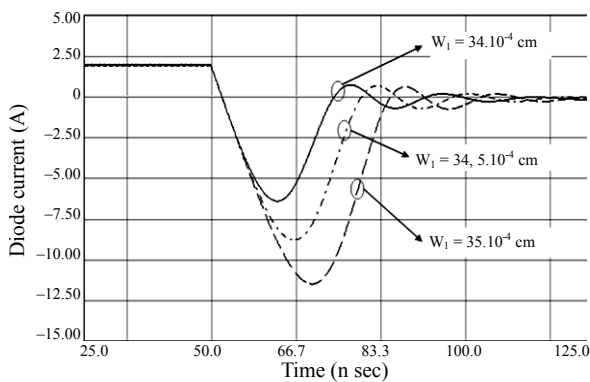
### 4.1. Influence of the Half Physical Intrinsic Region Width $W_I$

Under this turn-off state, we perform a simulation of the device with different values of the physical intrinsic region width  $W_I$  and we capture the curves of the forward current,  $I_F$  and the reverse voltage,  $V_R$ .

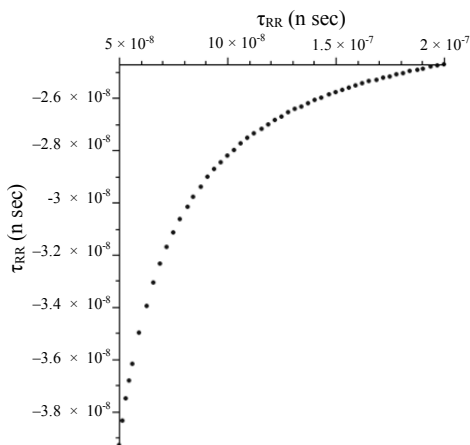
**Figure 5** shows that with increasing  $W_I$ , we give permission to the device to accumulate more charge under the on-state. When switched to the off-state, the device gets more time to evacuate these accumulated charges, so we can see a higher maximal reverse voltage and current.

### 4.2. Influence of the Doping Level $N_I$

**Figure 6** shows that with increasing the doping profile  $N_I$  in the device, the device gives more important values of reverse voltage and current. This can be explained by the fact that the depletion region width  $W_J$  becomes higher and so, injected charges rise more and more.



**Figure 5.** Influence of the intrinsic region width  $W_I$  on the diode current turn off characteristic.



**Figure 7.** Variation of the reverse recovery time  $\tau_{RR}$  in respect to the carrier life time  $\tau$ .

### 4.3. Influence of the Carrier Life Time $\tau$

With respect to the following equation of the reverse recovery time  $\tau_{RR}$  [2]:

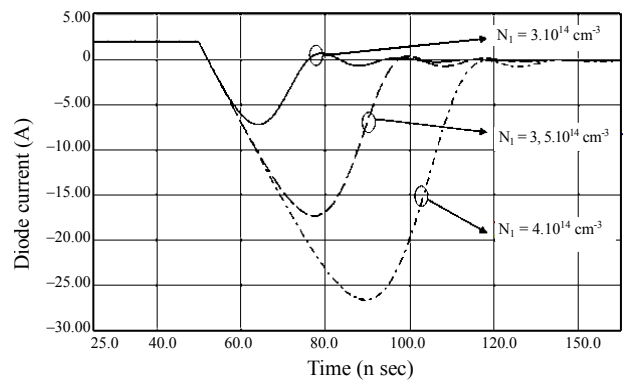
$$\tau_{RR} = \frac{T_M \tau}{T_M - \tau} \tag{12}$$

The plot of **Figure 7** is established with supposing a constant transit time set to 22ns. This plotted function is growing-up with increasing the carrier life time  $\tau$ , *i.e.*, the reverse recovery time  $\tau_{RR}$  is growing-up.

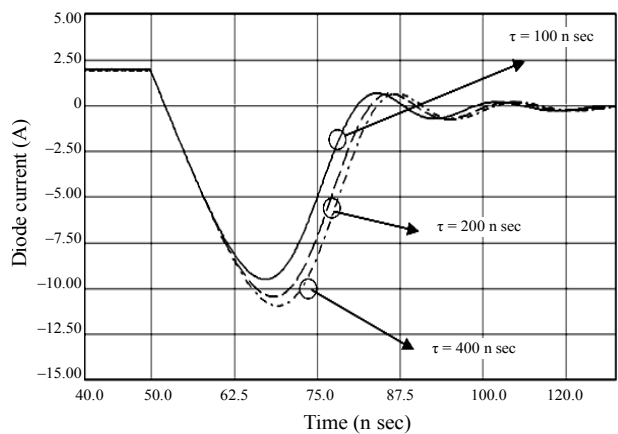
In fact, carriers injected to the bulk region recombine less and they have more chances to reach the side contacts of the device. So in the turn-off state, the device gives higher values of reverse voltage and current which is mentioned in **Figure 8**.

### 4.4. Comparison with Experimental Data

The model parameters for the power diode are estimated



**Figure 6.** Influence of the intrinsic region doping  $N_I$  on the diode current turn off characteristic.



**Figure 8.** Influence of the carrier life time  $\tau$  on the diode current turn off characteristic.

using the same parameter extraction procedure described in [2] at reverse recovery condition. The **Table 2** gives a summary of these model parameters values for the BYT12P600 power diode [7] which are valid for all operation conditions.

**Figure 9** illustrates a comparison of the measured and the simulated voltage and current waveforms for reverse recovery on three different operating conditions: a)  $V_R = 60V$  and  $I_F = 10A$ , b)  $V_R = 70V$  and  $I_F = 2.05A$ , c)  $V_R = 120V$  and  $I_F = 10A$ . The two simulated curves are respectively the simulation result of model [2] and the improved model developed in this study.

These previous **Figures 9(a), (b)** and **(c)** show a good agreement between simulation and experimental results except at the end of turn-off where oscillations appear. These oscillations at the end of the reverse recovery voltage waveforms are due to residual phenomena and are very difficult to simulate. However, the effect of these oscillations is not very interesting in design applications [8].

In this figure, the agreement is good enough about the current ( $I_{RM}$  and  $\tau_{RR}$ ) but not so good about the voltage.

On the other hand, the estimation of the stray inductance in the switching loop of the circuit is critical for modeling the switching process.

One cause of error is due to the current and voltage probes. In fact, as stated in [8], probes interact with the device under test, create delays due to propagation in the cable and worst of all degrade the signal due to distortion in the probes and the cables. The overall accuracy of the extraction procedure requires the probe effects to be taken into account in simulation.

Simulated forward current curve for the model cited in [2] for  $I_F = 2A$  and  $V_R = 120A$  presents an error on the slope compared with the measurement forward current curves. In fact, textbooks [9,10] detail that the diode current slope is approximated by  $di/dt = -V_R/L_m$  at the beginning of the reverse recovery, inside a switching cell circuit where a unique wiring parasitic inductance is considered.

For this reason, an improvement on the parasitic test-bench inductance was made in this work. The next section will treat this part.

#### 4.5. Parasitic Test Bench Inductance Investigation

For estimating the behavior of the device in circuit simulation, a complete model of the wiring influence is required which demands the development of a parasitic inductive matrix [8]. For more simplicity and short simulation time, in this study, a simple model for this wiring parasitic is formulated. This simulated test bench inductance improvement is based on the extracted values of  $L_m$  (see test bench circuit, **Figure 4**) from the measured turn-off characteristics according to the following relation:

$$\frac{di}{dt} = -\frac{V_R}{L_m} \quad (13)$$

**Figure 10** presents the variation of this test bench parasitic inductance extracted from the measured turn-off characteristics for 3 different test conditions. To capture this inductance influence on the simulated switching cell, a 2nd order polynomial fitting equation is introduced to predict its right value:

$$L_m = a_2 \left( \frac{V_R}{I_F} \right) + a_1 \left( \frac{V_R}{I_F} \right) + a_0 \quad (14)$$

With  $a_2$ ,  $a_1$  et  $a_0$  are fitting parameters set to:

$$a_2 = 0.0268 \cdot 10^9 \text{ [HA/V]}$$

$$a_1 = 1.3582 \cdot 10^9 \text{ [HA/V]}$$

$$a_0 = 103.19 \cdot 10^9 \text{ [HA/V]}$$

This equation is added to simulated test bench circuit via a VHDL-AMS entity in substitution of the fixed inductance.

**Figure 9(c)** shows the correction of the slope on the simulated current curves compared to measurement.

## 5. Conclusions

A physical improvement is made for a power diode lumped-charge model which consists of varying the width of the intrinsic bulk region with respect to the reverse applied voltage and current variations. A second improvement is made to the simulated test-bench circuit to estimate the right value of the parasitic inductance value. The new model is described in VHDL-AMS language and has been implemented in the SIMPLORER simulator. A good agreement is observed between the new model simulated data and measured data. The results of this improved model are verified with a wide range of operating conditions.

This model can be extended by including the selfheating effect which can greatly affect the turn off characteristics and the device performance.

**Table 2. New model's parameters list.**

Parameter symbol	description	Parameter value	Unity
$W_I$	Bulk region width	37.6	$\mu m$
$N_I$	Doping level of the I-region	$3.12 \times 10^{14}$	$cm^{-3}$
$\tau$	carriers lifetime	103.5	n sec
$T_M$	carriers transit time	Equation 10	n sec
$I_S$	Saturation current	$2.78 \times 10^{24}$	A
$R_{M0}$	Initial resistance	500	$\Omega$
$I_{SE}$	Recombination current	$45.7386 \times 10^9$	A
$C_{j0}$	Junction capacitance	2.2281	nF
$R_S$	Serial resistance	15.7632	m $\Omega$
$m$	Gradient coefficient	$430.9960 \times 10^3$	--
$\Phi_B$	Built-in potential	5.9294	mV

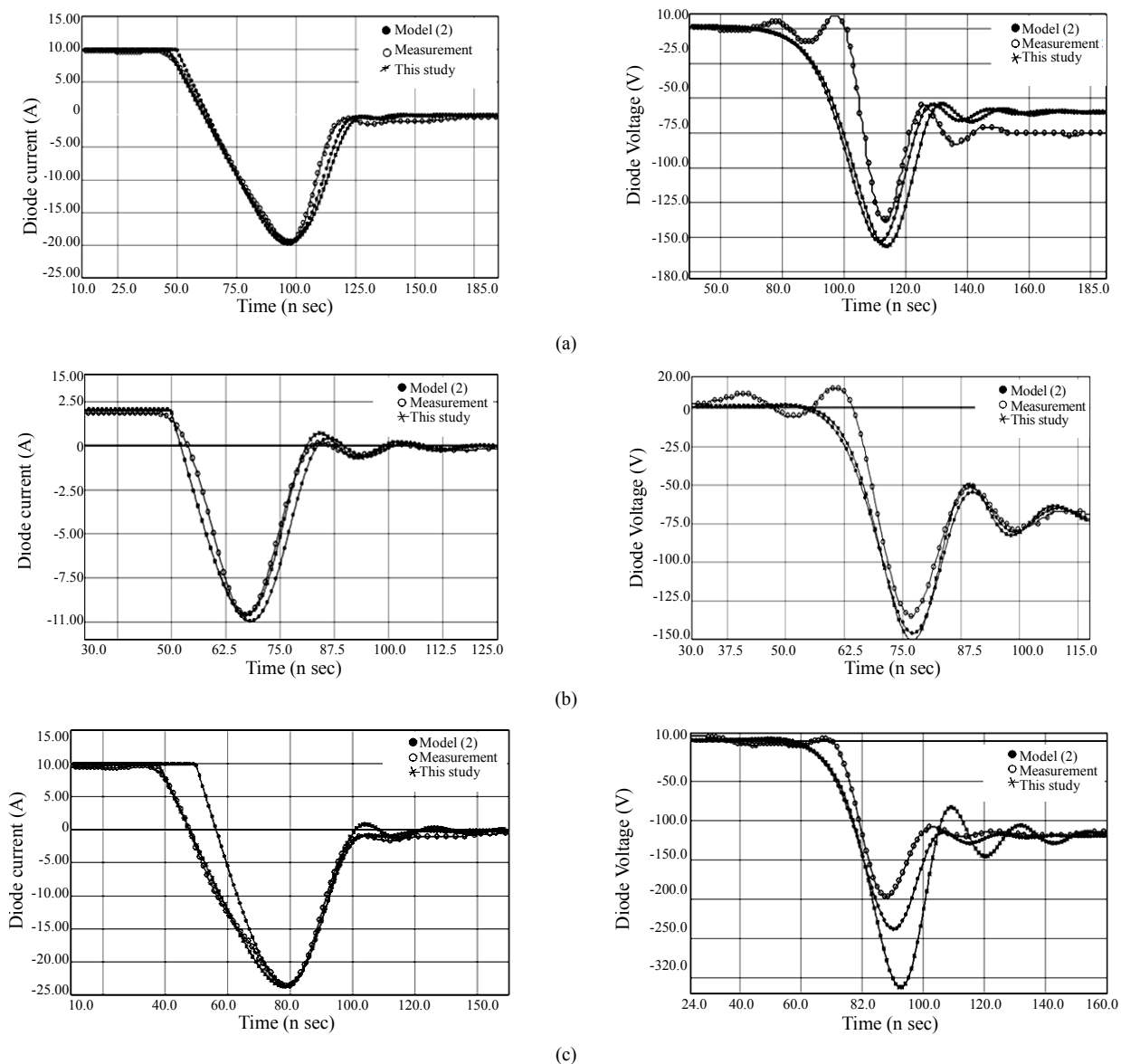


Figure 9. Comparison of measured and simulated current and voltage waveforms reverse recovery for model [2] and this study's model (a) VR = 60 V and IF = 10 A, (b) VR = 70 and IF = 2.05A, (c) VR = 120 V and IF = 10 A.

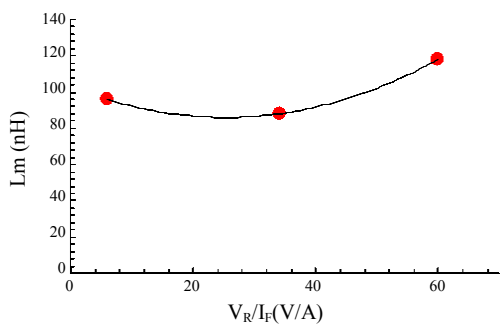


Figure 10. Extracted parasitic inductance test-bench (circles) for three measurement test conditions with 2nd order polynomial fitting function (black line).

This research is being continued at our laboratory to have a variety of basic library of elementary semiconductors in VHDL-AMS.

### 6. Acknowledgements

The authors thank H. Morel from “INSA de Lyon-CEGELY laboratory” for providing us with the reverse recovery measurement data and helpful discussions.

### 7. References

[1] C. L. Ma and P. O. Lauritzen, “Simple Power Diode Mo-

- del with Forward and Reverse Recovery,” *IEEE Transactions on Power Electronics*, Vol. 8, No. 4, 1993, pp. 342-346.
- [2] M. Najjari, H. Mnif, H. Samet and N. Masmoudi, “New Modeling of the Power Diode Using the VHDL-AMS Language,” *The European Physical Journal Applied Physics*, Vol. 4, No. 1, 2008, pp. 1-11.
- [3] H. Zhang and J. A. Pappas, “A Moving Boundary Diffusion Model for PIN Diodes,” *IEEE Transactions on Magnet*, Vol. 37, No. 1, 2001, pp. 406-410.
- [4] P. Antognetti and G. Massobrio, “Semiconductor Device Modeling with SPICE,” McGraw-Hill Inc, New York, 1988.
- [5] C. L. Ma and P. O. Lauritzen, “Modeling of Diodes with the Lumped-charge Modeling Technique,” *IEEE Transactions on Power Electronics*, Vol. 12, No. 3, 1997, pp. 398-405.
- [6] K. X. A. Caiafa, E. Santi, J. L. Hudgins and P. R. Palmer, “Parameter Extraction for a Power Diode Circuit Simulator Model Including Temperature Dependent Effects,” *17th Annual IEEE Applied Power Electronics Conference and Exposition*, Dallas, March 2002, pp. 452-458.
- [7] BYT12 600 Datasheet, “Datasheet Archive,” 1998. <http://www.datasheetArchive.com>
- [8] H. Garrab, B. Allard, H. Morel, K. Ammous, S. Ghedira, et al., “On the Extraction of PiN Diode Design Parameters for Validation of Integrated Power Converter,” *IEEE Transactions on Power Electronics*, Monastir, Vol. 20, No. 3, May 2005, pp. 660-670.
- [9] N. Mohan, T. M. Undeland and W. R. Robbins, “Power Electronics: Converters, Applications and Design,” 2nd Edition, John Wiley & Sons, New York, 1995.
- [10] R.W. Erickson and D. Maksimovic, “Fundamentals of Power Electronics,” 2nd Edition, Kluwer Academic Publishers, Berlin, 2001.