Engineering, **2011, 3, 583-587**
doi:10.4236/eng.2011.36069 Published Online June 2011 (http://www.SciRP.org/journal/eng)

Scientific Research

Computation of Error in Estimation of Nonlinearity in ADC Using Histogram Technique

Radhe Shyam Gamad*, Deepak Kumar Mishra
Department of Electronics & Instrumentation Engineering, S. G. S. Institute of Technology and Science, Indore, India
E-mail: *rsgamad@gmail.com, mishrad_k@hotmail.com*
Received December 22, 2010; *revised May* 25, 2011; *accepted June* 5, 2011

Abstract

Computation of error in estimation of nonlinearity in ADC using histogram test are reported in this paper. Error determination in estimation of Differential Nonlinearity (DNL) and Integral Nonlinearity (INL) of an ADC is done by taking deviation of estimated value from actual value. Error in estimated INL and DNL is determined to check the usefulness of basic histogram test algorithm. Arbitrary error is introduced in ideal simulated ADC transfer characteristics and full scale simulated sine wave is applied to ADC for computation of error in estimation of transition levels and nonlinearity. Simulation results for 5 and 8 bit ADC are presented which show effectiveness of the proposed method.

Keywords: Nonlinearity, Transfer Characteristics, Code Bin Width, Error Estimation, Transition Levels

1. Introduction

Real life signals are analog in nature and in order to interface them with digital processing systems it is necessary to convert them in digital using ADC. As ADC plays an important role in deciding accuracy of overall system, testing of an ADC is essential to find out its functional parameters. ADC test duration and its cost increase significantly with resolution of ADC. ADC is usually characterized by its figures of merits like Effective Number of Bits (ENOB), Signal to Noise and Distortion ratio (SINAD), DNL and INL [1,2]. Histogram technique is very popular for testing an ADC to determine several parameters of interest namely, INL, DNL, ENOB, gain error and offset error. Recently work on determination of error in estimation of code transition levels and computation of variance in gain and offsets has been published [3,4].

Also performance of techniques to determine ADC parameters have been evaluated [5,6]. DNL, INL and ENOB are determined based on code transition levels of ADC transfer characteristics [7,8]. If estimation of code transition levels has errors then subsequently it will lead error in estimation of parameters based on code transition levels. In this paper our contribution is in determination of error in estimation of DNL and INL.

Section 2 presents brief review of earlier work using histogram technique. Mathematical formulae developed for computing error in estimation of nonlinearity are presented in Section 3. Simulation results for 5 and 8 bit ADC are reported in Section 4. Conclusions are presented in Section 5.

2. Earlier Work Done on Histogram Technique

A sinusoidal stimulus signal with frequency (*f*), amplitude (*A*), and offset (*O*) is applied to the ADC under test and predefined number of samples, *M*, with sampling frequency (*fs*) are acquired. The expression used to estimate the transition levels, *T*[*k*], of an ADC with *N* bits is given as [3,9].

$$\hat{T}[k+1] = O - A\cdot\cos\left(\frac{C_k}{M}\right) \quad K = \quad \cdots \quad {}^{N-1} \qquad (1)$$

where $C_k = \sum_{i=0}^{k-1} h[i]$.

$h[i]$ = The total number of samples received in code bin *i*.

The number of counts in the cumulative histogram is a random variable and these depend on real transition voltages '*T*' and number of samples '*M*'. Normalized transition voltages '*U*(*k*)' can be expressed using Equation (1)

as:

$$U[k] = \frac{T[k] - O}{A} \quad (2)$$

For any particular values of gain and the offset, the DNL and INL can be determined without additive noise and overdrive as follows [10,11].

$$DNL = \frac{GW[K] - Q}{Q} \quad (3)$$

$$INL = \frac{[K-1]\cdot Q + T[1] - T[K]}{Q} \quad (4)$$

where, G = gain, $W[k] = K^{th}$ code bin width and Q = ideal code bin width.

3. Estimation of Nonlinearity

DNL is deviation of actual code bin width from ideal code bin width and INL is maximum deviation of actual transfer characteristics from ideal or best fit transfer characteristics. Estimate values of parameter are computed when additive noise and overdrive effects are considered. Considering additive noise, estimate of DNL and INL can be expressed as follow. In all formulae this symbol ^ on top of parameter indicates estimate value.

$$\hat{DNL} = \frac{\hat{G}\hat{W}[K] - Q}{\hat{Q}} \quad (5)$$

where, estimated code bin width = $\hat{Q} = \frac{\hat{V}}{2^N - 2}$,

$\hat{V} = T[2^N - 1] - T[1]$ or $\hat{V} = \hat{L} - F$

Similarly estimate of INL can be expressed as:

$$\hat{INL} = \frac{\{\hat{G}\cdot\hat{T}[K] + O\} - T_K^{ideal}}{\hat{Q}} \quad (6)$$

where from [2,3,12]:

$$\hat{G} = \frac{L_{ideal} - F_{ideal}}{\hat{L} - F}$$

where, L = Last transition level, F = First transition level.

Therefore,

$$\hat{Q} = \frac{\hat{L} - F}{2^N - 2} \quad (7)$$

$$\hat{W}[K] = T[K+1] - T[K] \quad (8)$$

Error Estimation in DNL and INL

From Equations (3) and (5), estimation error of DNL can be written as:

$$e_{D\hat{N}L} = DNL_{est} - DNL \quad (9)$$

Similarly from Equations (4) and (6), estimation error of INL can be given as:

$$e_{I\hat{N}L} = INL_{est} - INL \quad (10)$$

4. Results and Discussion

Ideal ADC transfer characteristics for 5 and 8 bit resolution are simulated and arbitrary nonlinearity error is introduced in their transfer characteristics. Simulated full scale sine wave with 0.98 MHZ frequency with slight over derives is applied to the ADC and large number of samples at 5 MHZ sampling frequency are collected. In first case using standard histogram technique code transition levels are computed after introducing DNL error in ADC transfer characteristics. Further error in code transition level estimation is determined. Error determination in estimation of DNL is done and is shown in **Figure 1** and **Figure 2** for 5 and 8 bit ADC respectively with respect to ADC code. Error variation in DNL estimation is observed with maximum value of approximately of 0.4 LSB and minimum value of <−0.2 LSB as shown in **Figure 1** for 5 bit ADC. Similarly for 8 bit ADC maximum value of error is observed and is equal to 0.5 LSB and minimum value equal to −0.2 LSB as shown in **Figure 2**. Also arbitrary INL error is introduced in 5 and 8 bit ADC transfer characteristics and computation of error in INL estimation is done and is shown in **Figure 3** and **Figure 4** for 5 and 8 bit ADC respectively. Though in this paper results for 5 and 8 bit ADC are presented but same test technique can be used for testing ADC with higher resolution.

5. Conclusion

This paper reports effects of additive noise and overdrive in computation of estimation error in DNL and INL of 5 and 8 bit ADC. Estimate value is taken when effects of additive noise and overdrive are considered. While actual value is considered without additive noise and overdrive. Estimation error is determined by taking difference of estimate value and actual value. Simulation of ideal ADC transfer characteristic is done and arbitrarily nonlinearity error is introduced in it. Simulation results for estimation error in DNL and INL are reported for 5 and 8 bit ADC.

6. Acknowledgements

This work has been carried out in SMDP VLSI laboratory of the Electronics and Instrumentation Engineering Department of Shri G. S. Institute of Technology and Science, Indore, India. This SMDP VLSI project is funded

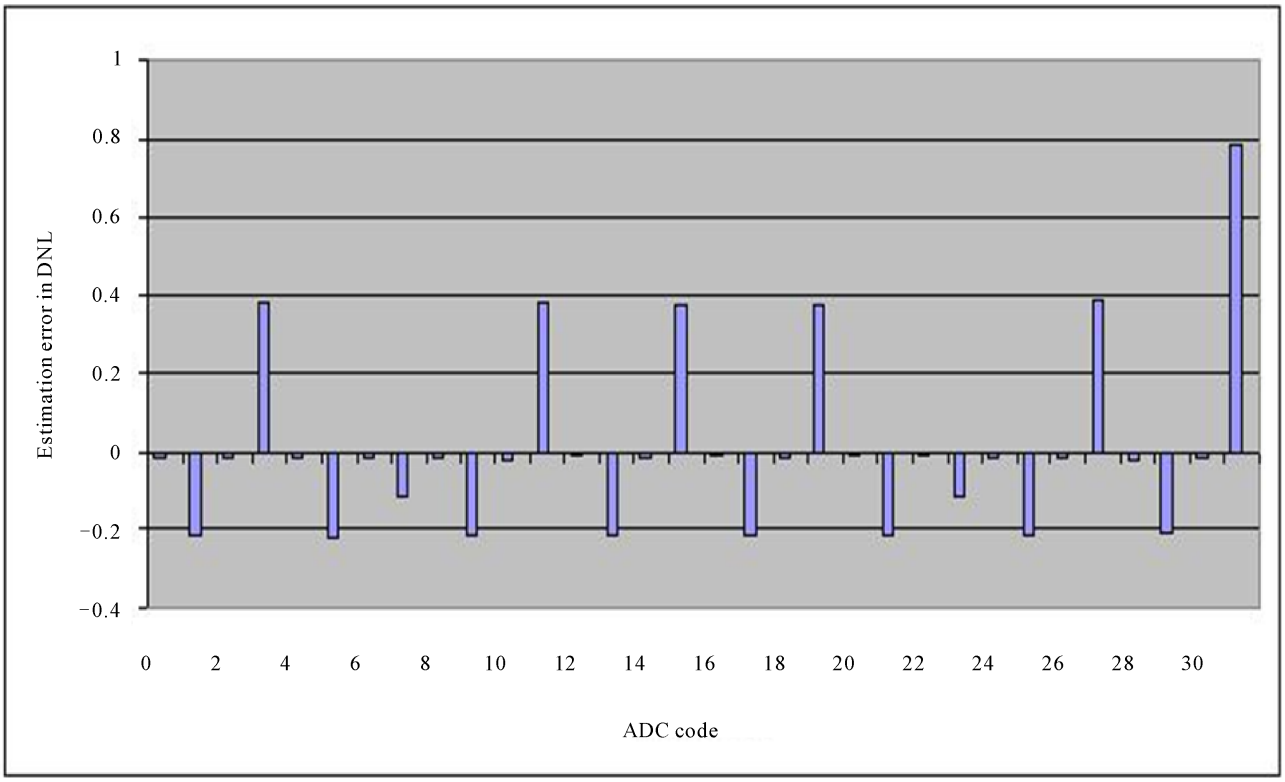

Figure 1. Estimation error in DNL for 5 bit ADC.

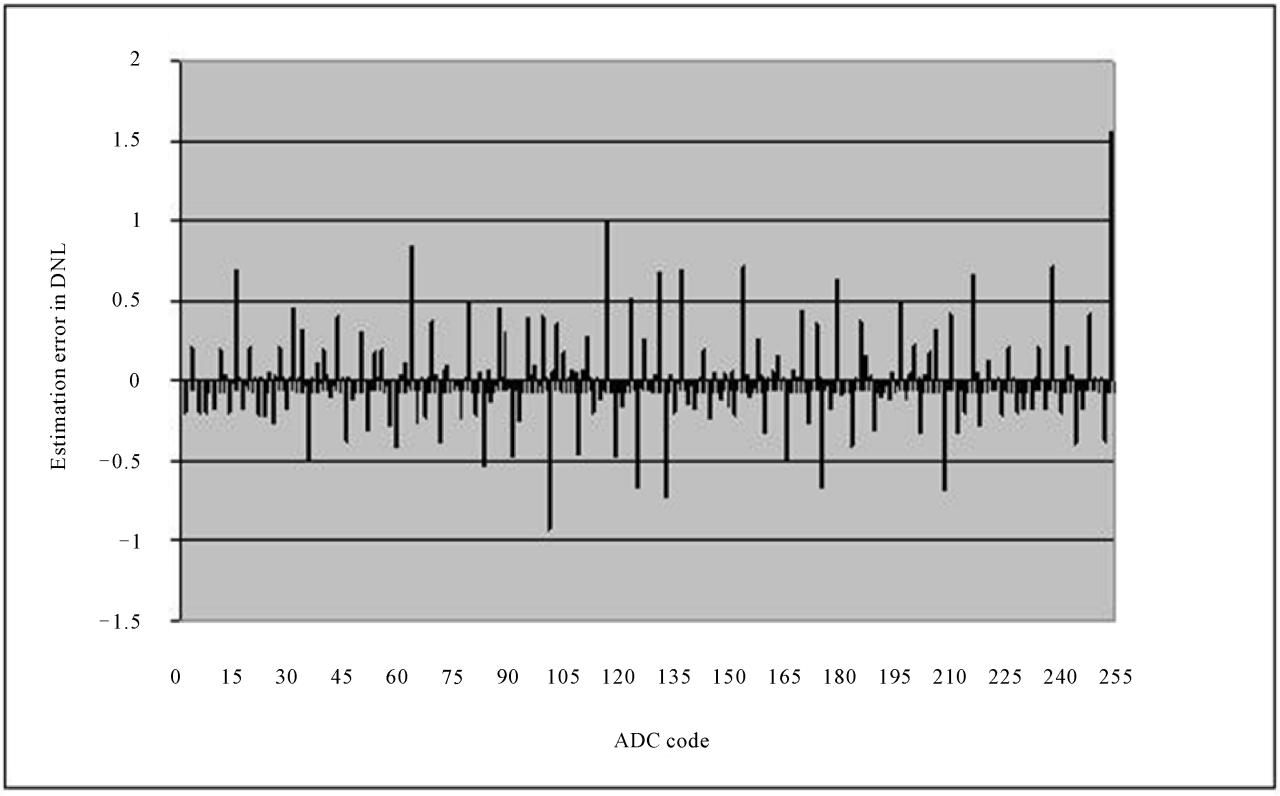

Figure 2. Estimation error in DNL for 8 bit ADC.

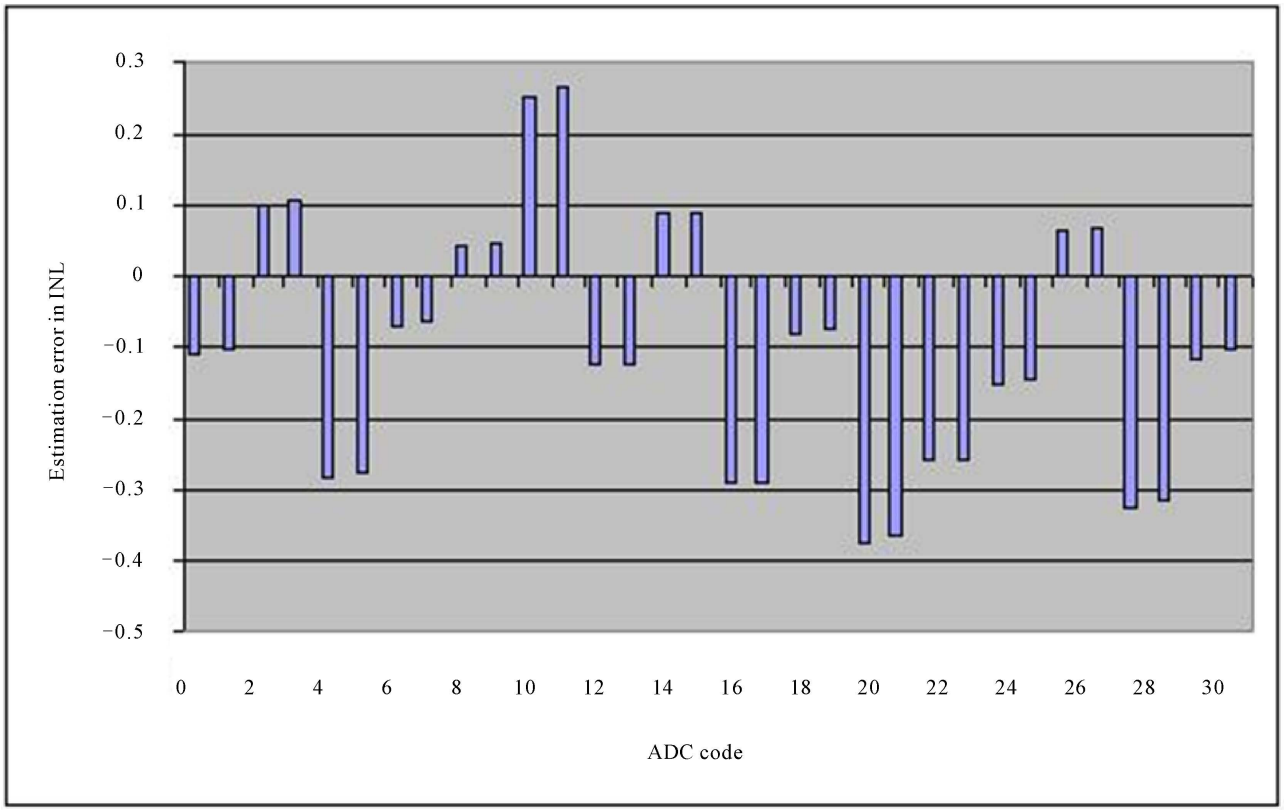

Figure 3. Estimation error in INL for 5 bit ADC.

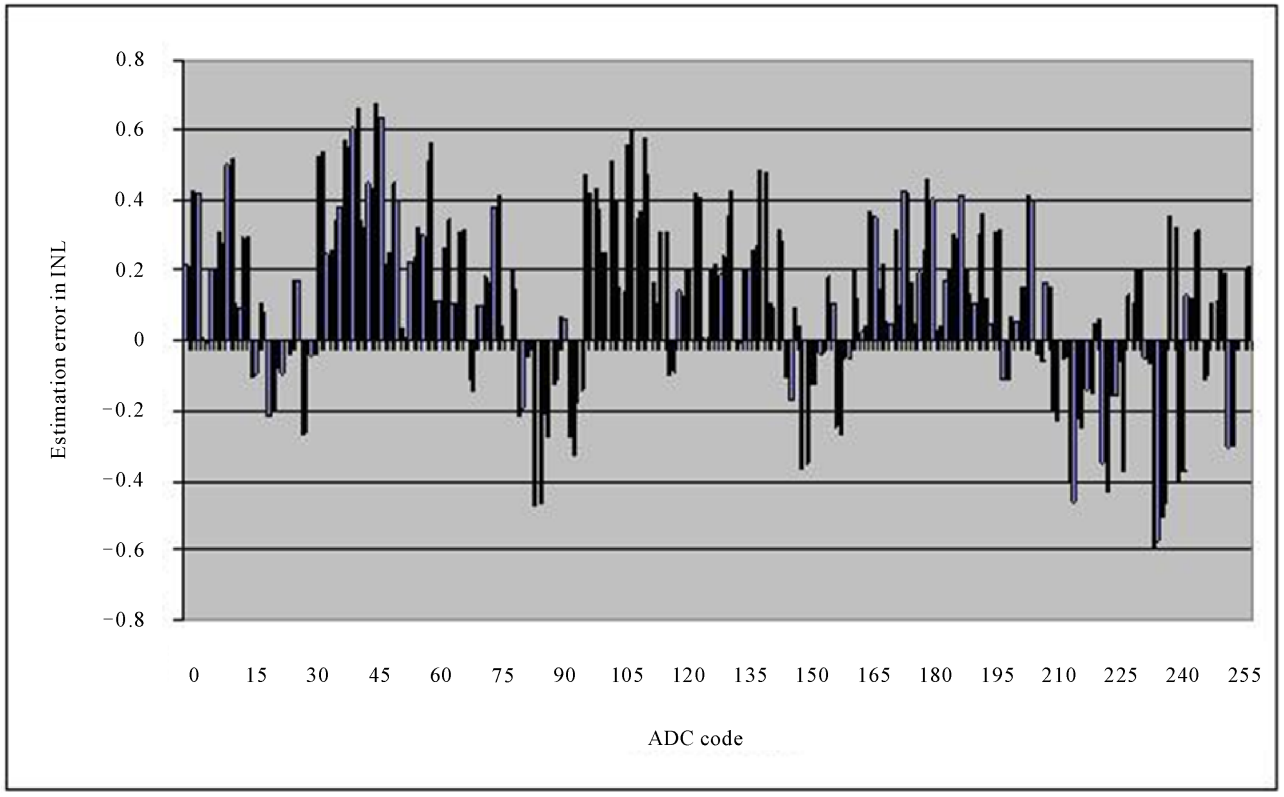

Figure 4. Estimation error in INL for 8 bit ADC.

by Ministry of Information and Communication Technology, Government of India. Authors are thankful to the Ministry for the facilities provided under this project.

7. References

[1] P. D. Capofreddi and B. A. Wooley, "The Use of Linear Models in A/D Converter Testing," *IEEE Transactions on Circuits and Systems –I*, Vol. 44, No. 12, 1997, pp. 1105-1113.

[2] IEEE std. "IEEE Standard for Digitizing Waveform Recorders," 1057-1994.

[3] F. C. Alegria and A. C. Serra, "Standared Histogram Test Precision of ADC Gain and Offset Error Estimation," *IEEE Transactions on Instrumentation and Measurement*, Vol. 56, No. 5, 2007, pp. 1527-1531. doi:10.1109/TIM.2007.907978

[4] F. C. Alegria and A. C. Serra, "Error in the Estimation of Transition Voltages with the Standard Histogram Test ADCs," *ELSEVIER International Journal on Measurement*, Vol. 35, 2004, pp. 389-397.

[5] H-W. Ting, Bin-Da Liu and S-Jyh. Chang, "A Histogram - Based Testing Method for Estimating A/D Converter Performance," *IEEE Transactions on Instrumentation and Measurement*, Vol. 57, No 2, February 2008, pp. 420-427. doi:10.1109/TIM.2007.910106

[6] R. S. Gamad and D. K. Mishra, "Gain Error, Offset Error and ENOB Estimation of an A/D Converter Using Histogram Technique," *Measurement*, Vol. 42, No. 4, May 2009, pp. 570-576.

[7] D. K. Mishra, "Dynamic Testing of High Speed A/D Converters Using Triangular Wave as Input Test Signal," *IE* (*I*) *Journal-ET*, Vol. 85, 2005, pp. 68-71.

[8] R. S. Gamad and D. K. Mishra, "Determination of Error in Nonlinearity Estimation in A/D Converter with Triangular Wave Input," *International Journal of Electronics, Taylor and Francis*, Vol. 96, No. 12, 2009, pp. 1237-1247. doi:10.1080/00207210903168314

[9] D. K. Mishra, N. S. Chaudhary and M. C. Shrivastava, "New Dynamic Test Methods for Determination of Nonlinearity and Effective Resolution of A/D Converters," *IETE Journal of Research* (*INDIA*), Vol. 43, No. 6, 1997, pp. 403-409.

[10] IEEE std. "IEEE Standard for Terminology and Test Methods for Analog to Digital Converters," 2000.

[11] J. Blair, "Histogram Measurement of ADC Nonlinearity Using Sine Waves," *IEEE Transactions on Instrumentation and Measurement*, Vol. 43, No. 3, 1994, pp. 378-383.

[12] A. Papoulis, "Probability, Random Variable and Stochastic Process," Third Edition, McGraw-Hill, New York, 1991.

