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Design of Digital to Analog Converters with Arbitrary Radix

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Abstract

There are DAC structures available in the literature for radix r = 2, 3, and 4; but how they are arrived at is missing. No general structure is available for any radix r. The aim of the paper is, therefore, to fulfil these gaps. To start with, the design relations are derived for the simplest possible attenuator circuit when connected to a voltage source V and a series resistance R, such that the complete circuit offers the Thevenin resistance R. Spread relations for this attenuator are derived. An example when 3 such attenuators with different attenuation constants are connected in cascade is given. Interestingly, the two attenuators with attenuation factors 1/2 and 1/3 have the same spread of 2. A generalized attenuator is then obtained when N number of identical attenuators are connected in cascade. This is modified to derive a digital to analog converter for any radix r.

Keywords

Digital to Analog Converter, Design of DAC, DAC of any Radix, DAC Structure

1. Introduction

Multiple logics have several advantages over binary ones. Therefore, many multiple logic circuits have been developed [1]-[7]. Due to all these applications, there has been an interest in digital to analog converters (DACs) since long [8]-[16]. Binary to analog conversion (B/A) (radix 2) is very popular. Miyata *et al.* [8] and Current [9] deal with ternary (T/A) and quaternary (Q/A) (radices 3 and 4, respectively), to analog conversion. But none of these gives how the structures are arrived at. In [9] quaternary to analog conversion is obtained directly from that of radix 2 and compared with that R, 4/3R, 3R ladder DAC. It is shown that the Q/A requires 26% less total resistance if fabricated and approx-

imately 15% more if assembled with discrete resistors of one value by series and parallel combinations of resistors. No generalized design is available for DACs with arbitrary radix r.

This paper gives the design of ladder DACs for any radix r. B/A, T/A, Q/A converters are the special cases. Conditions will be derived when N number of attenuators (one such attenuator is shown in Figure 1(a) in dashed line box) are cascaded so that the Thevenin voltage will be aV, $a = 1/r$ is the attenuation factor (AF), while the Thevenin resistance is R. Such a structure is further modified for realizing ladder DACs for any radix $r = 1/a$.

2. Design of Ladder DACs

2.1. Basic Attenuator

Consider the circuit shown in Figure 1(a) where the simplest possible attenuator (potential divider) shown in dashed line box. Its Thevenin voltage

$$V_1 = \frac{R_2}{R_2 + R_1 + R} V = aV \tag{1}$$

where

$$a = \frac{R_2}{R_2 + R_1 + R} \tag{2}$$

is the AF. Thevenin resistance R_{T1} as seen from 1-1' in Figure 1(a) can be made equal to R, first increasing R by a series resistance R_1 and then restoring it by connecting a parallel resistance R_2. Thus the condition is

$$R_{T1} = \frac{R_2 (R_1 + R)}{R_2 + R_1 + R} = R\,. \tag{3}$$

Solving for R_1, we get

$$R_1 = \left(\frac{1-a}{a}\right) R = (r-1)R\,. \tag{4}$$

From (2) and (4), we get

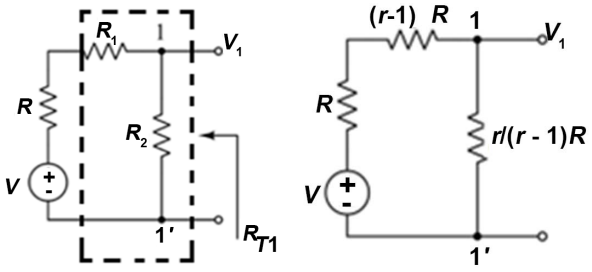
$$R_2 = \left(\frac{1}{1-a}\right) R = \left(\frac{r}{r-1}\right) R\,. \tag{5}$$

After substituting the values of R_1 and R_2 in circuit of Figure 1(a), we get the circuit shown in Figure 1(b). To avoid the fractional value of R_2, we scale up all the resistance values by a factor $(r-1)$. Scaled circuit is shown in Figure 2(a).

Note that, if a voltage V is applied in series with rR instead of $(r-1)R$, as shown in Figure 2(a), Thevenin voltage will be $\left[(r-1)/r\right]V$ with the same Thevenin resistance R_{T1}.

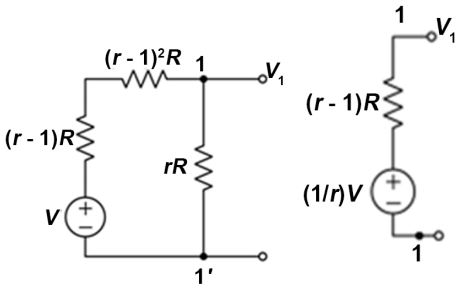
2.2. Spread

Out of the three resistance values $(r-1)$, r and $(r-1)^2$ in Figure 2 the minimum value is $r-1$, and the maximum value is $(r-1)^2$ as long as $(r-1)^2 \geq r$, *i.e.*, when $r \geq 2.6$ and ≤ 0.36. For integer values of r, $r \geq 3$ as r cannot be negative.



(a) (b)

Figure 1. (a) A simplest possible attenuator; (b) Attenuator with values.



(a) (b)

Figure 2. Scaled circuit of **Figure 1(b)** and its Thevenin equivalent.

Spread

$$S = \frac{R_{\max}}{R_{\min}} = \begin{cases} \dfrac{(r-1)^2}{r-1} = r-1, & r \geq 3 \\ \dfrac{r}{r-1}, & r = 2 \end{cases}. \tag{6}$$

Note that the spread is 2 for both $r = 2$ and 3.

2.3. Cascaded Attenuator

If one more section is cascaded as shown in **Figure 3(a)**, it can easily be seen that Thevenin voltage is

$$V_2 = \frac{R_2}{R_2 + R_1 + R} aV = a^2 V \tag{7}$$

and Thevenin resistance is still R. The Thevenin equivalent is shown in **Figure 3(b)**.

Thus if N number of sections are connected in cascade as shown in **Figure 4(a)**, then Thevenin voltage will be

$$V_n = a^N V \tag{8}$$

and the Thevenin resistance will be R. The equivalent circuit is shown in **Figure 4(b)**.

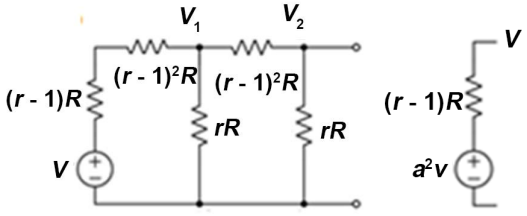


Figure 3. (a) Cascaded 2 sections, (b) Thevenin equivalent circuit.

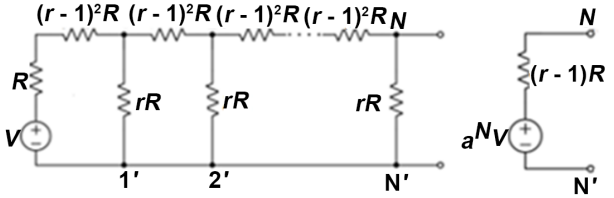


Figure 4. (a) Cascaded *n*-sections, (b) Thevenin equivalent circuit.

As an application of the above theory, Figure 5 shows a circuit which has 3 attenuators in cascade with $r = 2, 3, 4$.

It may be noted that the Thevenin voltage and the node voltage are the same as long as attenuator is not loaded. Hence in a chain of cascaded attenuator only the last one will have this property; all others do change their node voltages. This aspect is further discussed in section on practical results. Note that the spread, from Equation (6), is 2.25; while this would have been 23 if a single attenuator with $a = 1/24$ were used.

2.4. DAC Circuit

Let us consider the circuit of Figure 4 with voltage sources connected as shown in Figure 6(a). After replacing the portion of the circuit left to 11' by Thevenin equivalent the circuit becomes as shown in Figure 6(b) where

$$V_{T1} = \frac{r-1}{r} V_o . \tag{9}$$

Repeating the similar step across the terminals 22' and using superposition theorem, the circuit reduces to that shown in Figure 6(c) where

$$V_{T2} = \frac{r-1}{r^2} V_o + \frac{r-1}{r} V_1 = \frac{r-1}{r^2} \left[V_o + r V_1 \right]. \tag{10}$$

Repeating the same across terminals 33', the circuit reduces to that shown in Figure 6(d).

$$\begin{aligned} V_{T3} &= \frac{r-1}{r^3} V_o + \frac{r-1}{r^2} V_1 + \frac{r-1}{r} V_2 \\ &= \frac{(r-1)}{r^3} \left[V_o + r V_1 + r^2 V_2 \right]. \end{aligned} \tag{11}$$

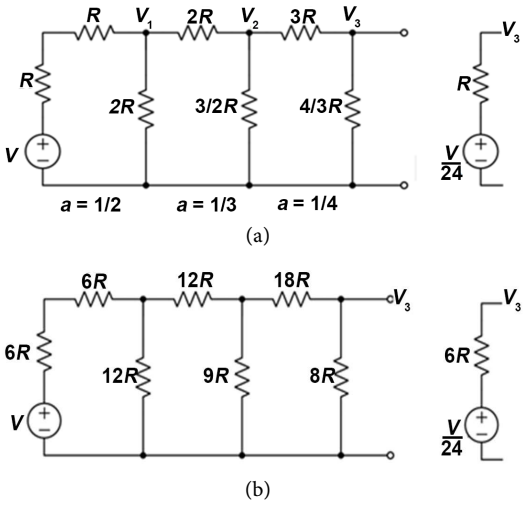


Figure 5. (a) 3 cascaded sections with different AFs; (b) Circuit after scaling with a factor of 6.

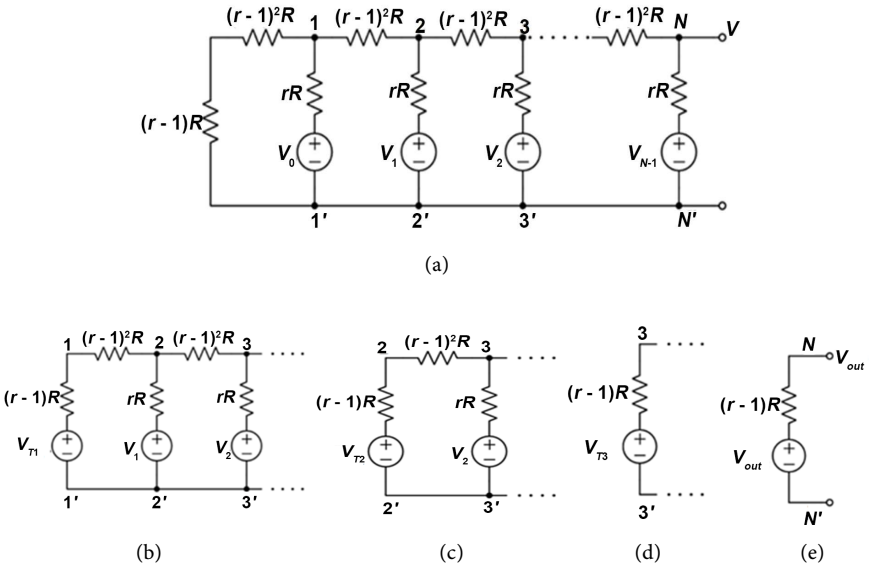


Figure 6. (a) Ladder with voltage sources, (b)-(e) circuits after applying successively Thevenin theorem.

Proceeding in this manner, we can write for the entire circuit of Figure 4(a),

$$V_{out} = \frac{r-1}{r^N} \sum_{k=0}^{N-1} r^k V_k. \tag{12}$$

Now we modify the circuit as shown in Figure 7 where switches $S_k (k = 1, N-1)$ are inserted which are operated by digital input. Depending upon the bit value, the particular switch connects to different weighted voltages according to the radix r. Thus the output voltage is proportional to the analog value of the digital input.

The resistance values in Figure 7 are the same for $r = 2$ as given in [17] [18], for $r = 3$ given in [8] after scaling by a factor 2/3, and for $r = 4$ given in [9].

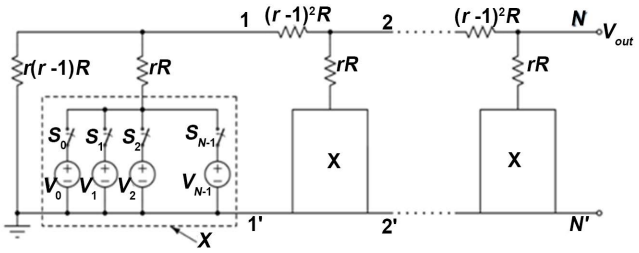


Figure 7. Digital to analog voltage converter.

A resistance of value $(r-1)$ is connected across terminals NN' so as to make the ladder symmetrical. This is shown in Figure 8(a). This will, however, reduce the voltage to

$$V'_{out} = \frac{r}{r+1} V_{out}. \tag{13}$$

This DAC, if connected to some circuit, will be further loaded. To avoid this loading, one can connect a non-inverting amplifier at the output as shown in Figure 8(b). This will have an extra advantage of adjusting the gain to any desired value by choosing R_f. However, one resistance can be reduced, if an inverting amplifier is used, as shown in Figure 8(c), wherein the resistance of $r(r-1)$ is connected to virtual ground instead of actual ground. Again the desired gain can be adjusted by choosing proper value for R_f. If a positive output is required, then the polarity of all the weighted reference voltages can be changed to negative.

3. Practical Results

The circuits shown in Figure 5(b) and that in Figure 7 for radix 3 and number of bits $N = 3$, were assembled. The resistances used were 10% tolerance, OA used is 741, resistances were connected in series and/or parallel to have the desired values. Voltage used for Figure 5(b) is 12 V and for Figure 6 were +15 V, −15 V, 4.5 V and 9 V.

The calculated values of voltages V_1, V_2 and V_3 are (4.54 ≠ 6 V, 1.625 ≠ 2 V, 0.5 V, respectively, using node analysis, and the corresponding practically measured values are 4.6 V, 1.82 V and 0.5 V which are in close agreement.

Following 3 sets of measurements were made for the DAC: 1) without any resistance $r(r-1)R = 6$ kΩ at the output, 2) with resistance 6 kΩ connected across NN' and 3) with inverting amplifier of gain −3/2. Resistance values chosen as R_1 = 4 kΩ, R_2 = 3 kΩ, and R = 2 kΩ, R_f = 8 kΩ. The analog voltage output V'''_{out} versus the digital input for set (3) are plotted in Figure 9. In all the cases, the practical results were in close agreement with the theoretically expected results. For example, when the digital input given is 200, the output $V_{out} = 6.01$ V (6 V), $V'_{out} = 4.53$ V (4.5 V) and $V'''_{out} = 6.04$ (6 V). The bracket values are the theoretically expected ones. These results show that the DAC exhibits the practical response very closely the expected theoretical one.

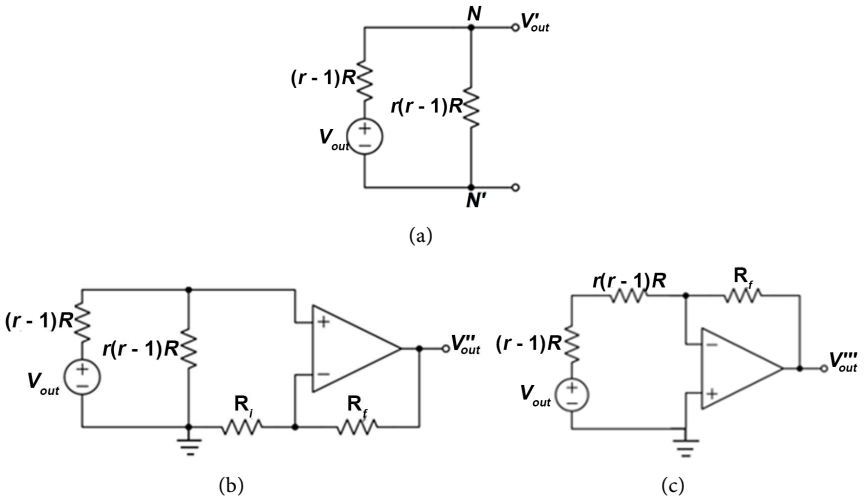


Figure 8. (a) Circuit with additional resistance connected; (b) Circuit with non-inverting amplifier; (c) Circuit with inverting amplifier.

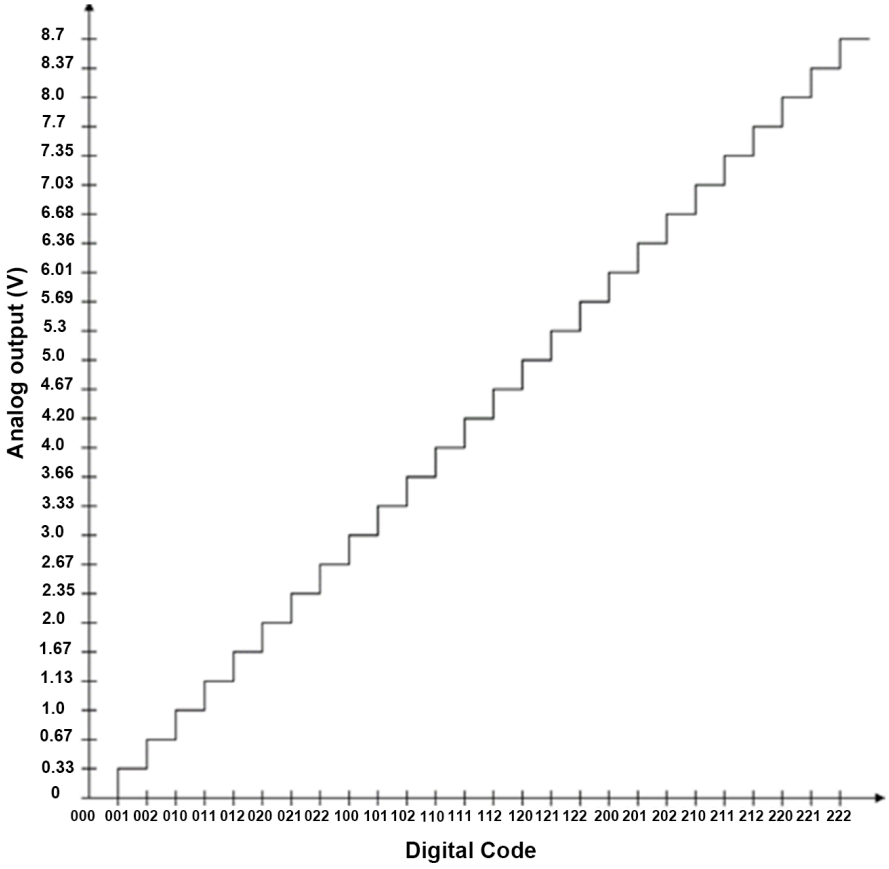


Figure 9. Plot of analog voltage output versus digital input.

4. Conclusion

Design relations have been derived for the simplest possible attenuator circuit when connected to a voltage source of voltage V and a series resistance R, such that the complete circuit offers the Thevenin Resistance R. Spread relations for

the circuit have been derived. An example when 3 such attenuators with different attenuation constants are connected in cascade has been given. Interestingly, the two attenuators with attenuation factors 1/2 and 1/3 have the same spread of 2. A generalized attenuator has been obtained when N number of identical attenuators are connected in cascade. This has been used to derive a general digital to analog converter for any radix r. Specific circuits were assembled in the laboratory and practical results were taken. These results match closely with the expected theoretical ones.

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