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28-nm UTBB FD-SOI vs. 22-nm Tri-Gate FinFET Review: A Designer Guide—Part I

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Abstract

Nowadays, transistor technology is going toward the fully depleted architecture; the bulk transistors are becoming more complex in manufacturing as the transistor size is becoming smaller to achieve the high performance especially at the node 28 nm. This is the first of two papers that discuss the basic drawbacks of the bulk transistors and explain the two alternative transistors: 28 nm UTBB FD-SOI CMOS and the 22 nm Tri-Gate FinFET. The accompanying paper, Part II, focuses on the comparison between those alternatives and their physical properties, electrical properties, and reliability tests to properly set the preferences when choosing for different mobile media and consumers' applications.

Keywords

UTBB FD-SOI: Ultra-Thin Body and Box Fully Depleted Silicon on Insulator, Tri-Gate FinFET, DIBL: Drain Induced Barrier Lowering

1. Introduction

As the size of the transistor is downscaled, the decrease of the power consumption, the decrease of the leakage current, and the achievement of high performance should be taken into account. In bulk transistors, the two electrical terminals, source and drain, are built on doped silicon and the flow of electrons between them is controlled by the gate. As the transistor shrinks, the channel is reduced, the control of gate exercised over the channel region is reduced too, thus lowering the transistor performance [1] and allowing some unwanted leakage current flows even if the transistor is off; this leakage is increased as the channel gets smaller as shown in **Figure 1** [1].

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In an ideal transistor, the channel potential is only controlled by gate voltage (V_g) through gate capacitance. On the other hand, the channel potential, in a real transistor, is also subjected to the influence of drain voltage through drain capacitance, which is between the drain and the channel. When the gate length is large, the drain capacitance is much smaller than the gate capacitance and the drain voltage does not interfere with $V_g's$ role as the sole controlling voltage. When the channel becomes short, the distance between source and drain gets smaller, and the drain capacitance becomes larger [2]. Then, the transistor will have two terminals that play a role in controlling the channel: drain and gate terminals. And because the drain is connected to a potential voltage V_{DD}, a flow of electrons is occurred and the channel starts to conduct, increasing the leakage current. For a long time, researchers had believed that this problem can be solved by reducing the gate thickness to make a compromise with the largeness of the drain capacitance. But in the 90's, and after several experiments, it was realized that this is not accurate; the leakage current still occurs in the channel interface as shown in **Figure 2** [3], the gate thickness can make no difference, whether it is thick or thin. Thus, the solution was to find a technique in which the silicon must not be far from the gate [3].

Two facts drastically reduce device performance: leakage is one of those, and variability is the other [4]. If doping concentration is increased, then leakage is reduced but variability increases [5]. When the transistor is scaled down, the random dopants, which are the difference in implanted impurities concentration, are unacceptable from design point of view. There are other sources of variability such as the metal gate granularity, and line edge roughness as shown in **Figure 3** [5]. The metal gate granularity is occurred when the metallization annealing results in crystallization of the metal; the metal grains will have different

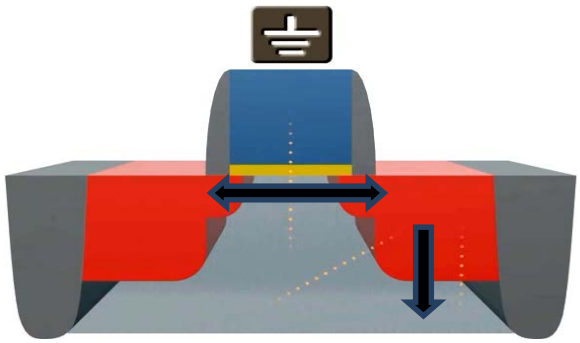

Figure 1. Bulk CMOS leakage currents at OFF state [1].

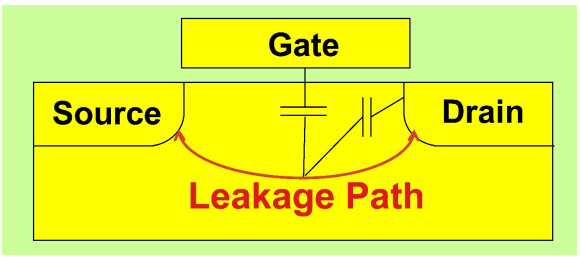

Figure 2. Leakage path [3].

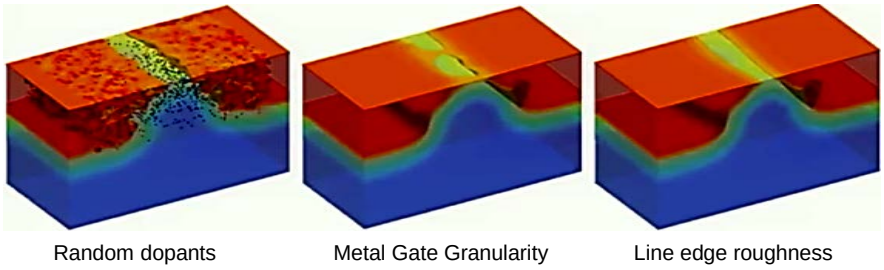

Figure 3. Statistical variability in 20 nm CMOS [5].

crystallographic orientation that leads to different work functions at the interface between the metal and the high-K material, that will cause a variation of the local threshold voltage in the gate area. The line edge roughness is a result from the variations in lithography and etching in fabrication process which causes a variation in the channel width and gate length.

The topics of this paper are outlined as follow:

- Alternative Transistors: the current design solutions used to reduce transistor's geometry and enhance the performance: UTBB FD-SOI and Tri-Gate FinFET.
- Reliability Test for UTBB FD-SOI AND TRI-GATE: applying Hot Carrier Injection (HCI) and the breakdown of the gate oxide TDDB (Time Dependent Dielectric Breakdown).
- Comparison Between 28-nm UTBB FD-SOI and 22-nm TRI-GATE FINFET: compares the physical and electrical characteristics of both transistors and determines the appropriate one to select for analog or digital applications.
- Conclusion.
- Future Work.

2. Alternative Transistors

Minimizing the leakage current and improving the performance in bulk silicon transistor have been more complex when the node of the transistor arrived to 28 nm. In technology of about 28 nm and below, a new solution was introduced to reduce the complexity and to get the advantage of reducing transistor's geometry: UTBB FD-SOI and Tri-Gate FinFET. Both transistors share CMOS technology with a fully depleted transistor architecture but make the transistor a better switch.

2.1. 28-nm UTBB FD-SOI

A 28-nm Fully Depleted Silicon on Insulator (FD-SOI) which was built without changing the fundamental geometry of the transistor lies on adding a thin insulator layer of buried oxide positioned under the channel as shown in **Figure 4**. By that there is no need to add dopants to the channel due to the thin silicon film in the channel, thus making it fully depleted. The net effect is that the gate can now control very tightly the full volume of the transistor body which makes it behave much better than a Bulk CMOS transistor, especially as supply voltage

(hence gate voltage) gets lower and transistor's dimensions shrink. The technology of very thin buried oxide is called Ultra-Thin Body and Buried Oxide (UTBB).

On the same technology node, the UTBB FD-SOI has smaller channel effective length 24 nm (PB0: poly-bias 0) compared to that of the bulk's one 28 nm. Smaller channel length means shorter path flow for electrons. That reduces the time needed for the electrons' flow from the source to the drain, leading to a fast transistor [6]. UTBB FD-SOI poly-bias enables several channel lengths (PB4 = +4 nm, PB10 = +10 nm, and PB16 = +16 nm) to obtain different V_{th} and to optimize the leakage. This technique is used also in bulk design.

The buried oxide insulator layer confines the electron when flowing from the source to the drain as shown in **Figure 5**, so it reduces the leakage current from the channel to the substrate.

The very thin silicon layer enables the silicon under the transistor gate to be fully depleted of charges; therefore, it eliminates the random dopants fluctuation; as shown in **Figure 6(b)**. In UTBB FD-SOI, field lines from gate cannot terminate in the undoped body (no charges there) because mirror charges are localized beneath BOX and the Lengths of field lines have tight distribution [7]. By that, it decreases the variability [8], and it will have better matching for short channel devices. Also, the absence of channel doping and pocket implants in the fully depleted transistor produces lower noise specifications and higher gains when compared to bulk technologies. The total dielectric isolation of the channel

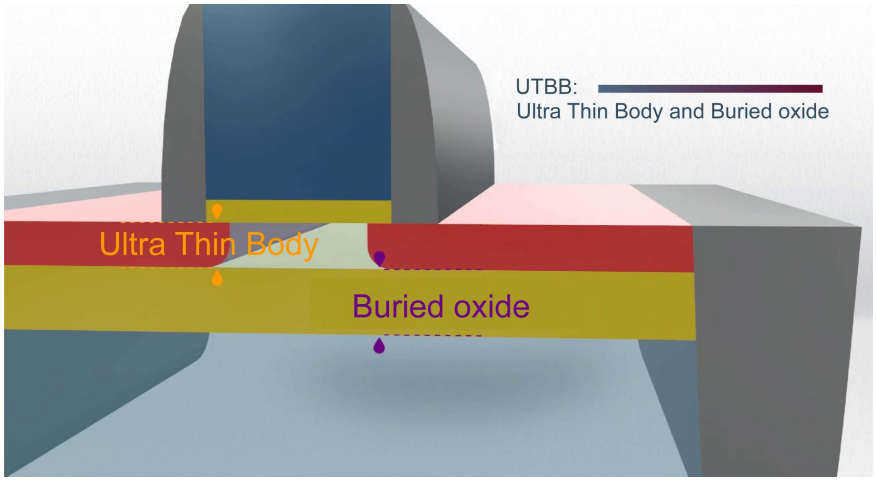

Figure 4. UTBB FD-SOI geometry [1].

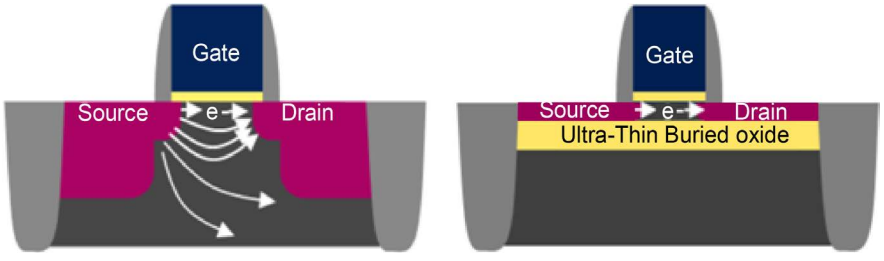

Figure 5. Electron flow [1].

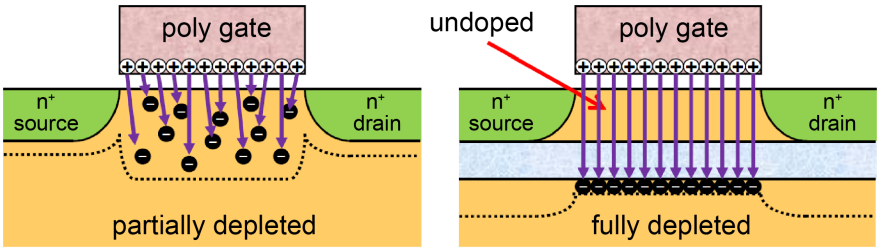

Figure 6. Field lines in partially depleted and fully depleted [7].

allows for lower drain/source capacitances and leakage currents in addition to the benefit of total latch-up immunity. Also, the reduction of the gate length decreases the gate capacitance and it has a raised source/drain epitaxy to reduce the access resistance. The saturation drain current, I_D, as in Equation (1):

$$I_D = \frac{1}{2n}\mu C_{ox}\frac{W}{L}\left(V_{GS} - V_{TH}\right)^2 \tag{1}$$

where μ: effective mobility, W: device width, L: channel length V_{GS}: gate to source voltage, V_{TH}: threshold voltage.

For the bulk transistor, n is as in Equation (2):

$$n = 1 + \frac{\varepsilon_{si}}{C_{ox} X_{d\max}} \cong 1.4 \text{ to } 1.6 \tag{2}$$

For UTBB FD-SOI, n is as in Equation (3):

$$n = 1 + \frac{\frac{\varepsilon_{si}}{t_{si}} C_{oxb}}{C_{ox}\left(\frac{\varepsilon_{si}}{t_{si}} + C_{oxb}\right)} \cong 1.05 \text{ to } 1.1 \tag{3}$$

where $X_{d\max}$: maximum depletion width, C_{ox}: gate oxide capacitance, C_{oxb}: buried oxide capacitance, t_{si}: silicon thickness.

Based on the above equations of n, it is clear that the current in UTBB FD-SOI will be higher than that of the bulk transistor by a factor of $\times(1.3 - 1.4)$.

The Sub-threshold slope (SS) indicates how effectively the flow of drain current of a device can be stopped when V_{gs} is decreased below V_{th}. When $I_d - V_g$ curve of a device is steeper, sub-threshold slope will improve. It is characterized by steep sub-threshold slope that exhibits a faster transition between off (low current) and on states (high current). The sub-threshold slope factor depends on the capacitance of the CMOS technology as in Equation (4), which is degraded due to the insulated layer. The thickness of the insulated layer also plays a role on the capacitance value: as the thickness of insulated layer is increased, consequently capacitance decreases. Therefore, the sub-threshold slope will be decreased [9].

$$S_t = \frac{KT}{q}.\left(1 + \frac{C_d}{C_i}\right) \tag{4}$$

where $\frac{KT}{q}$ is the thermal voltage, C_d is the depletion capacitance, and C_i is the

gate oxide capacitance.

In the weak inversion regime, there is a potential barrier between the source region and the channel region. The height of this barrier is a result of the balance between drift and diffusion current between those two regions. The barrier height for channel carriers should be ideally controlled by the gate voltage to maximize trans-conductance. The DIBL (Drain Induced Barrier Lowering) [10] effect occurs when the barrier height for channel carriers at the edge of the source is reduced due to the influence of drain electric field, upon application of a high drain voltage. This increases the number of carriers injected into the channel from the source leading to an increased drain off-current as shown in Figure 7. Thus, the drain current is controlled not only by the gate voltage, but also by the drain voltage [11].

The bulk DIBL is as in Equation (5):

$$\mathrm{DIBL} = 0.8\frac{\varepsilon_{si}}{\varepsilon_{ox}}\left(1+\frac{X_j^2}{L_{el}^2}\right)\cdot\frac{T_{ox}}{L_{el}}\cdot\frac{T_{dep}}{L_{el}}\cdot V_{DS} \tag{5}$$

where ε_{si}: silicon permittivity, ε_{ox}: gate oxide permittivity, X_j: junction depth, L_{el}: electrical channel length, T_{ox}: gate oxide thickness, T_{dep}: depletion width in bulk transistor, V_{DS}: Drain Source voltage.

The DIBL of UTBB FD-SOI is in Equation (6):

$$\mathrm{DIBL}_{\mathrm{FDSOI}} = 0.8\frac{\varepsilon_{si}}{\varepsilon_{ox}}\left(1+\frac{T_{si}^2}{L_{el}^2}\right)\cdot\frac{T_{ox}}{L_{el}}\cdot\frac{T_{si}}{L_{el}}\cdot V_{DS} \tag{6}$$

where T_{si} is the channel thickness.

By comparing Equation (5) and Equation (6), the UTBB FD-SOI has better DIBL than that of the bulk transistor because UTBB FD-SOI takes into consideration the ultra-thin channel, T_{si}.

To improve the transistor performance, a voltage can be applied to the substrate. This method is called Body Biasing which facilitates the creation of the

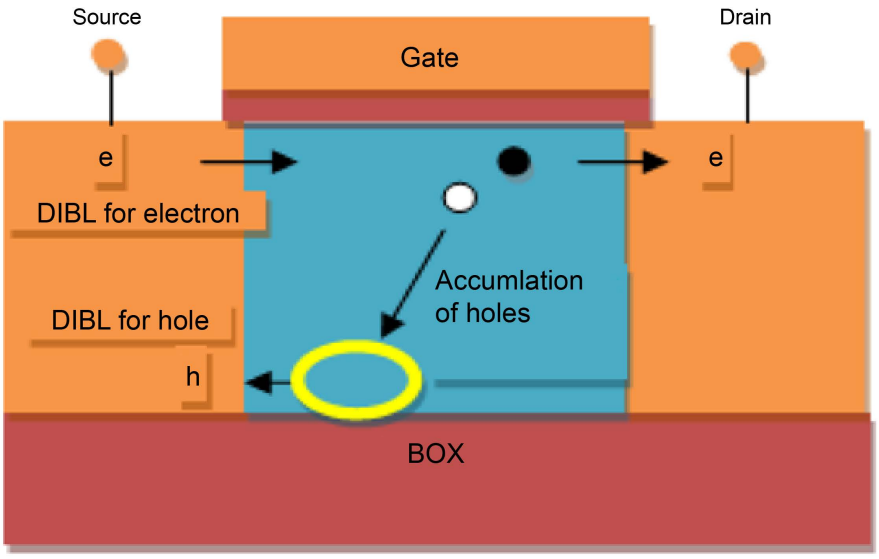

Figure 7. DIBL mechanism [11].

channel between the source and the drain resulting a faster switching. Because of the ultra-thin layer in FD-SOI, the biasing creates a buried gate below the channel making the transistor act as a double vertical gate transistor. Scaling down the silicon thickness under the gate of a FD-SOI transistor below 5 nm [12] is optimum on SOI substrate in order to limit the leakage current flows as shown in **Figure 8** [13].

This Ultra-thin body and BOX (UTBB) FD-SOI transistor architecture (7 nm silicon thickness and 25 nm BOX thickness) has a stronger body effect than bulk transistors and therefore enables effective threshold voltage (V_{th}) management through body biasing. The BOX thickness (25 nm) is a compromise between an increased parasitic source/drain to substrate capacitance and enhanced body effect. While in bulk technology, the ability of doing body biasing is limited due to the parasitic current leakage, the buried gate in UTBB FD-SOI prevents any leakage in the substrate. Thus, it allows much more voltage on the body leading to a significant boost performance. The range of back-gate biasing in UTBB FD-SOI is quite wider by a factor of 10 (*i.e.* $-3\text{ V} < V_{BB} < 3\text{ V}$) compared to the bulk technology ($-300\text{ mV} < V_{BB} < 300\text{ mV}$). And the slope of threshold voltage is 85 mV/V vs. 25 mV/V as shown in **Figure 9**, which leads to a significant drive current boost [14]. If V_{BB} is positive, then it is a forward body bias (FBB). But, if it is negative, then it is a reverse body bias (RBB), for NMOS transistor and vice versa for the PMOS transistor.

The characteristics of UTBB FD-SOI vertical double transistor allow the creation of new concept in processor design. Different voltage can be applied independently at the top and at the buried gate [15], and dependently change the

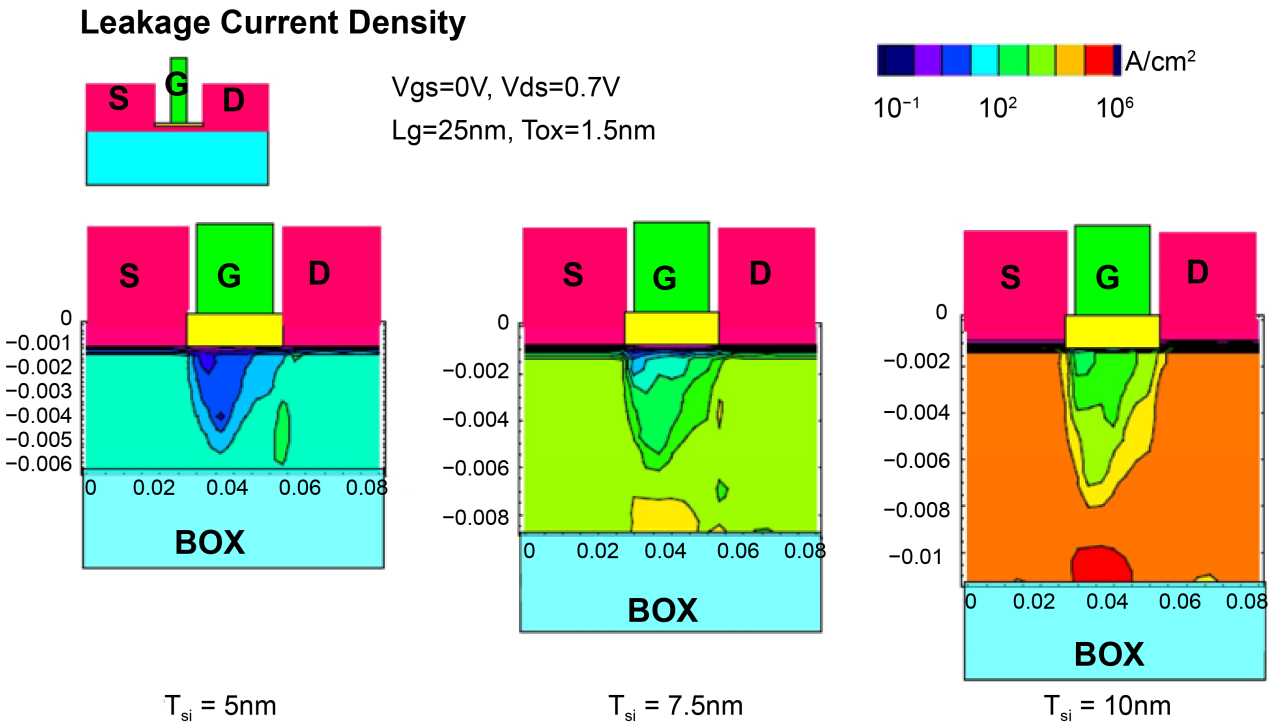

Figure 8. Leakage current w.r.t silicon thickness [13].

characteristics of the transistor. By choosing the optimum voltages at the top gate and the buried one, the transistor characteristics can transform from high performance to low power transistor.

Since the leakage current strongly depends on the threshold voltage V_{th}, different V_{th} transistors can be optimized for speed and low power as shown in Figure 10. A higher I_{ON} maximizes the circuit speed because it reduces the charging time of the pad output capacitances of the transistor cell. That higher I_{ON} can be achieved by a lower V_{th}. However, lowering V_{th} increases exponentially

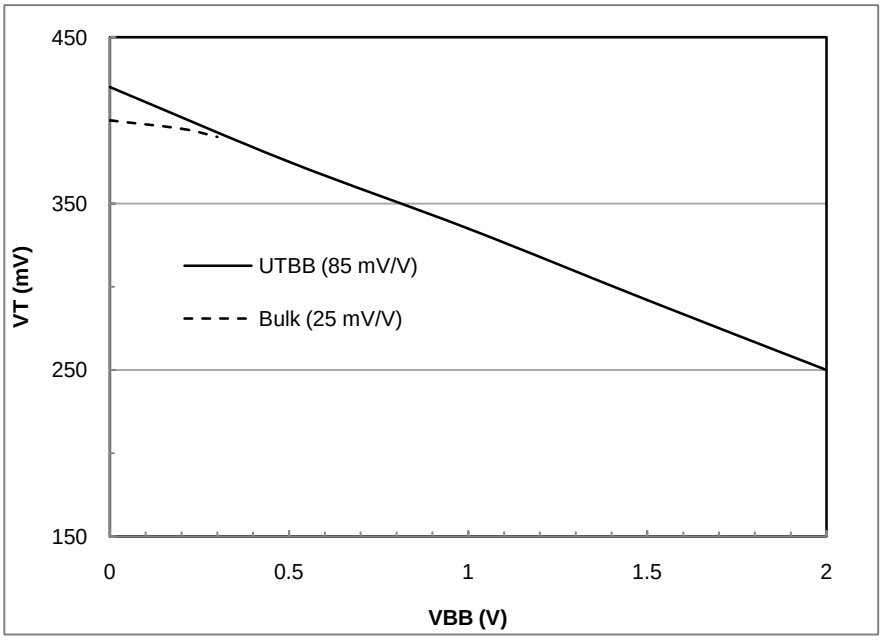

Figure 9. Threshold voltage w.r.t. UTBB FD-SOI & bulk BODY bias voltage [14].

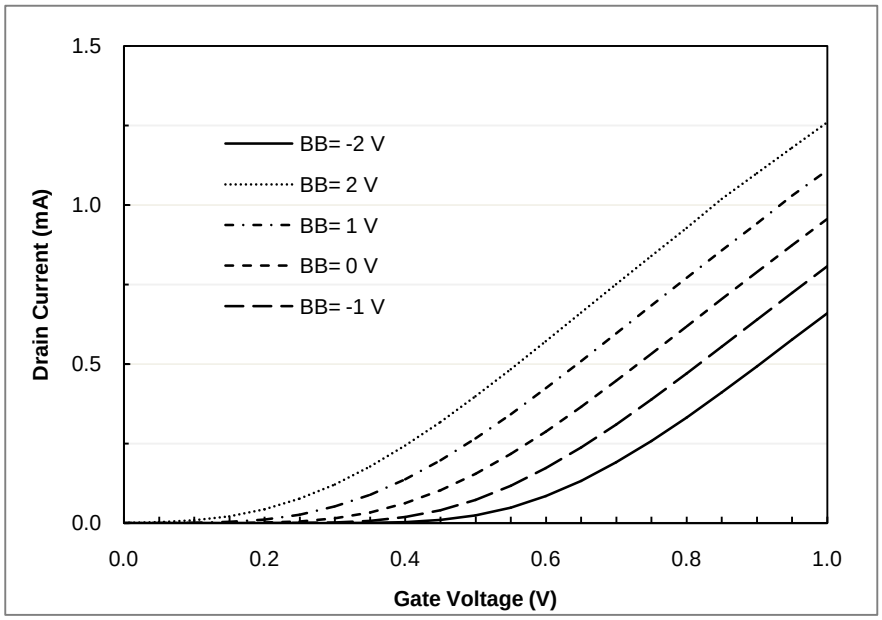

Figure 10. Simulation of the shifting effects on the VT introduced by the back-gate biasing n-channel UTTB FDSOI.

the leakage current. That leads to a compromise between speed and power that the designer should balance.

Body bias can be used to vary the maximum frequency: while the FBB can be applied to increase the frequency, the RBB can be applied to decrease it. The dynamic body bias combined with a different voltage frequency scaling (DVFS) can provide the best performance power tradeoffs. **Figure 11** gives an example for NMOS UTBB FD-SOI transistor. By raising the V_{DD} by 100 mV, the performance is raised on the penalty of larger active power. Similarly, by reducing the V_{DD} by 100 mV, the leakage and active power is reduced. It can be applied as a FBB to reduce the threshold voltage by 60 mv to introduce frequency gain and more efficient active power, or it can be applied as an RBB to reduce the leakage power as shown in **Figure 12** [16]. Some points can be optimally selected to make a tradeoff between active and leakage power as in **Figure 11**. So, by overdriving the V_{DD} of the device and applying FBB, a best performance can be reached with x1.6 of the original maximum frequency. On the other hand, lowering the V_{DD} reduces active power but sacrificing the performance. Moreover, by applying RBB, the leakage power is reduced as well as the maximum frequency, which is reduced to the half. The leakage can achieve 1 pA/um [17].

The lower leakage current makes the transistor less sensitive to the temperature; **Figure 13** is a demo of a processor using the 28-nm UTBB FD-SOI with other bulk transistor which shows the difference in temperature and power efficiency improvement [18].

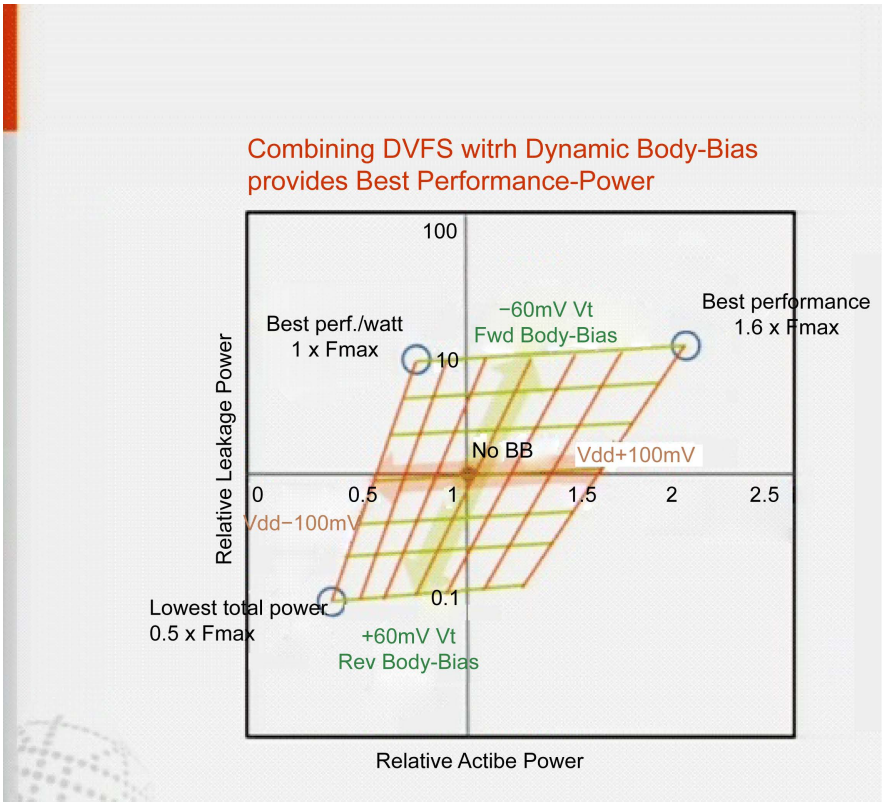

Figure 11. Combining DVFS with body Bias [17].

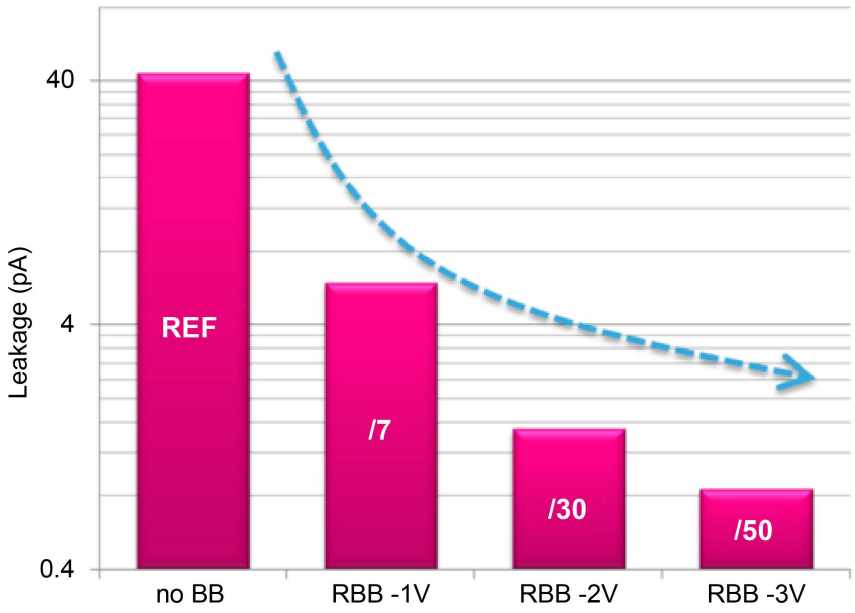

Figure 12. RBB impacts on leakage current [16].

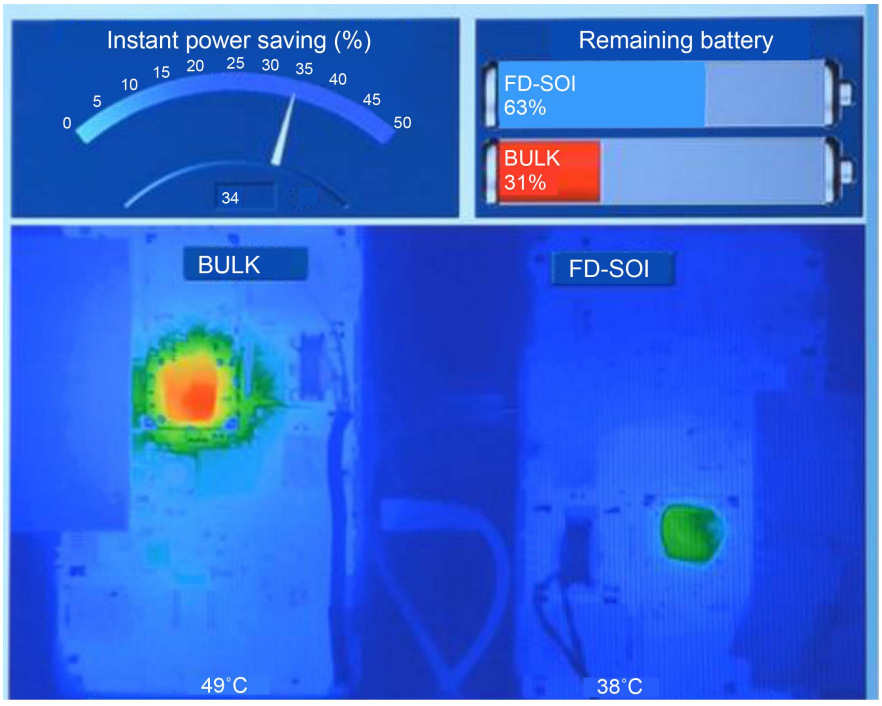

Figure 13. Temperature of UTBB vs. bulk [18].

The 28-nm UTBB FD-SOI offers two types of transistors to optimize leakage and performance: RVT (conventional well) and LVT (flip well) as seen in **Figure 14**. The forward and reverse bias ranges depend on the doping of the well in which the transistor is residing; keeping in mind that going beyond the bias range creates a parasitic diode between the "n" and "p" wells. If optimized for forward body bias using the "flip well" doping, the effective gate voltage of the transistor can be boosted by as much as 3 V, but this restricts the reverse bias

shift to −300 mV. Conversely, using the conventional well, reverse body bias can be extended to −3 V, limiting forward bias to 300 mV [19].

2.2. 22-nm Intel's 3D Tri-Gate Transistor

In a conventional planar FET transistor, the current flowing through the channel is closely related to the width (W) of the device, divided by the length (effective L). As the industry scales to smaller nodes, it is ideal to decrease effective L, which improves the drive strength of the transistor. However, shorter transistors have less control over the channel and exponentially higher sub-threshold leakage. To control leakage, the channel is heavily doped, which makes everything more susceptible to variability. A 3D Tri-Gate transistor looks a lot like the planar transistor but with one fundamental change. Instead of having a planar inversion layer (where electrical current actually flows), Intel's 3D Tri-Gate transistor creates a three-sided silicon fin that the gate wraps around, creating an inversion layer with a much larger surface area as shown in Figure 15. The width ($W_{\text{effective}}$) of a Tri-Gate transistor is the sum of all three sides: twice the fin height plus the fin width which is approximately the 2x of the planar width [20].

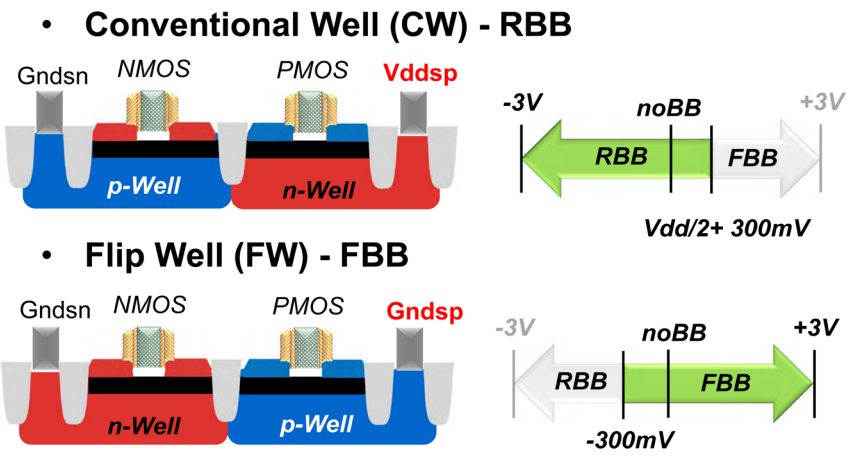

Figure 14. Types of UTBB-FD-SOI [16].

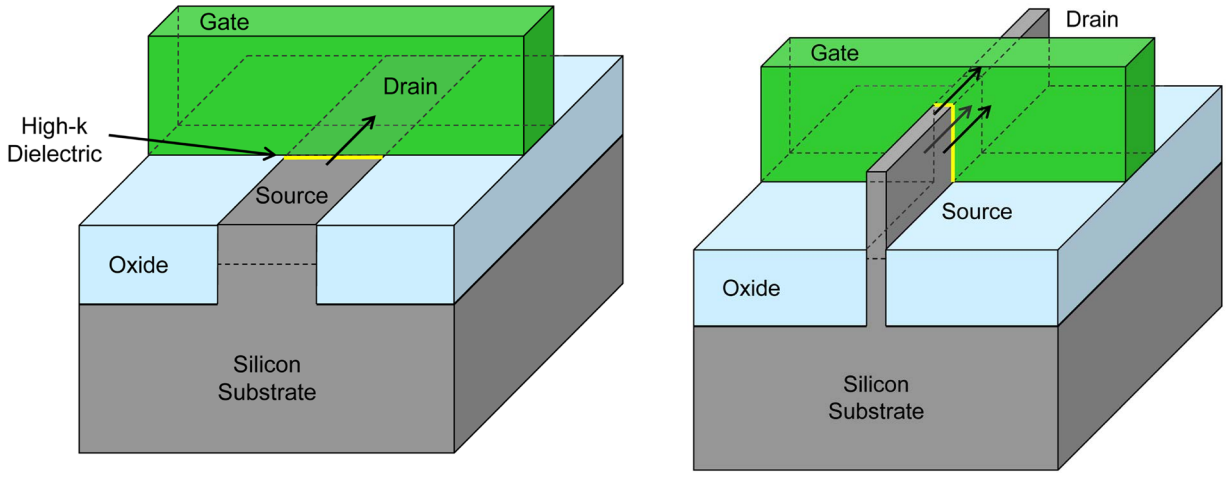

Figure 15. Planar (to the left) and Tri-Gate FinFETs [21].

The gate exerts more control over the flow of current through the transistor; it surrounds the channel on all three sides and has much better control so that all the charge below the transistor is removed (fully depleted) and there is no depletion capacitance, so it is tightly controlled. This reduces dopants variability because no—or lightly—doping is needed to control the channel. The "fully depleted" characteristics of Tri-Gate transistors provide a steeper sub-threshold slope that reduces leakage current (from 0 V to 0.4 V). The DIBL is given as in Equation (7) which is the lowest compared to bulk and UTBB FD-SOI transistors.

$$\mathrm{DIBL}_{\text{TRI-Gate}} = 0.8\frac{\varepsilon_{si}}{\varepsilon_{ox}}\left(1+\frac{\frac{T_{si}^2}{4}}{L_{el}^2}\right)\cdot\frac{T_{ox}}{L_{el}}\cdot\frac{\frac{T_{si}}{2}}{L_{el}}\cdot V_{DS} \tag{7}$$

The steeper sub-threshold slope can also be used to target a lower threshold voltage, allowing the transistors to operate at lower voltage to reduce power and/or improve switching speed as shown in **Figure 16**. To build transistors with different performance and leakage, multiple fins are ganged together and share a single gate essentially multiplying the width (higher drive current), and the threshold voltage can be varied by adjusting gate length or by low doping the channel [22].

The 22-nm Tri-Gate transistors are 18% and 37% faster at 1 V and 0.7 V respectively than Intel's 32 nm transistors [21]. When transistors are not fully switched on—at low voltage, it shows a very big improvement over conventional planar FET transistor closer to 37% as shown in **Figure 17**. This improves the frequency, but still in practice the actual frequency in the chip is determined by the slowest circuits. Also, the operation at lower voltage comes with good performance, reducing active power by >50% ($P \sim F * V^2$) [21].

The Tri-Gate FinFET transistors are fully depleted so the carriers flow in

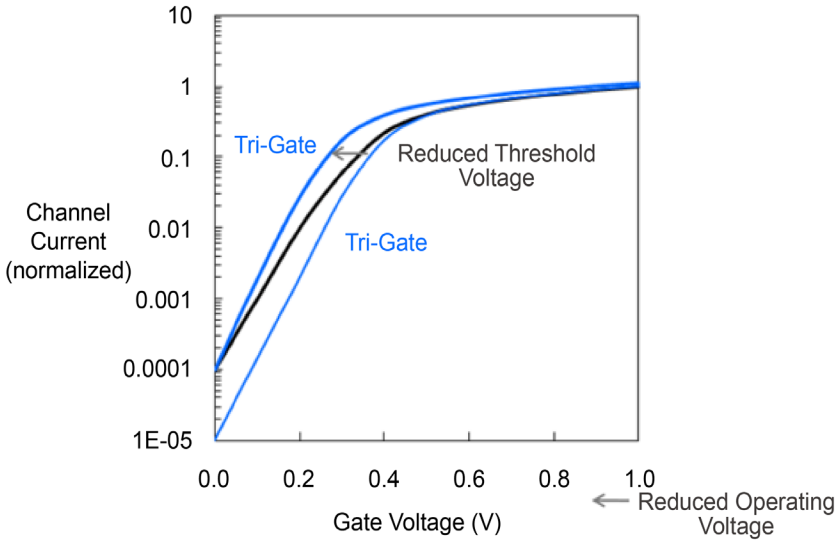

Figure 16. Tri-Gate FinFET drain current w.r.t. gate voltage [21].

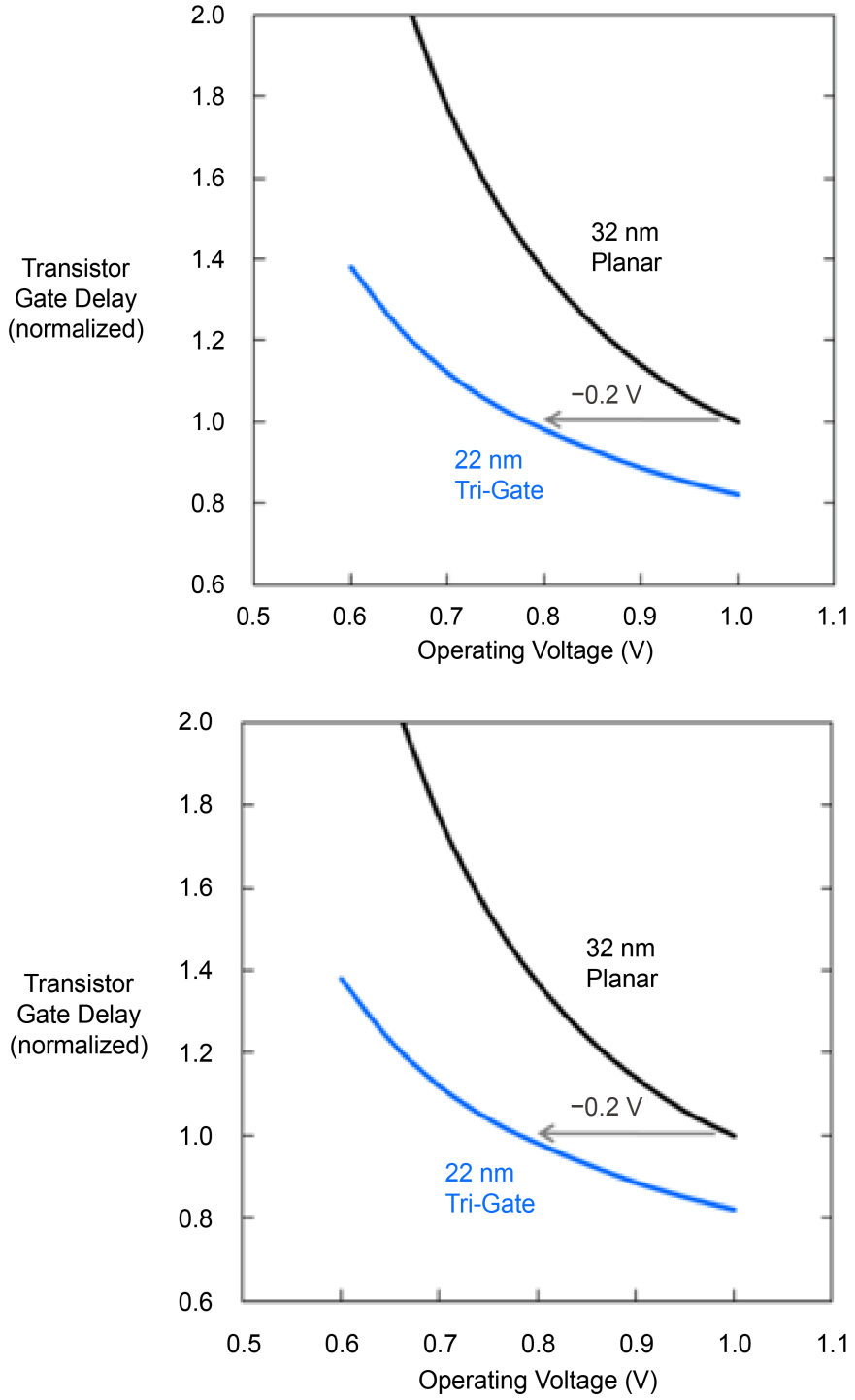

Figure 17. Tri-Gate FinFET performance improvement [21].

threshold and sub-threshold voltage in different places compared to where they flow in high gate bias condition. As seen in **Figure 18**, the charges distribution is at the middle of the channel, and by increasing the gate bias voltage, the charges start to move to the interface and can have fringing effects. So, the charges distribution in the channel isn't uniform and complicated. More charges are located at the sharp corner which will have strong field. Then current passes at the mid

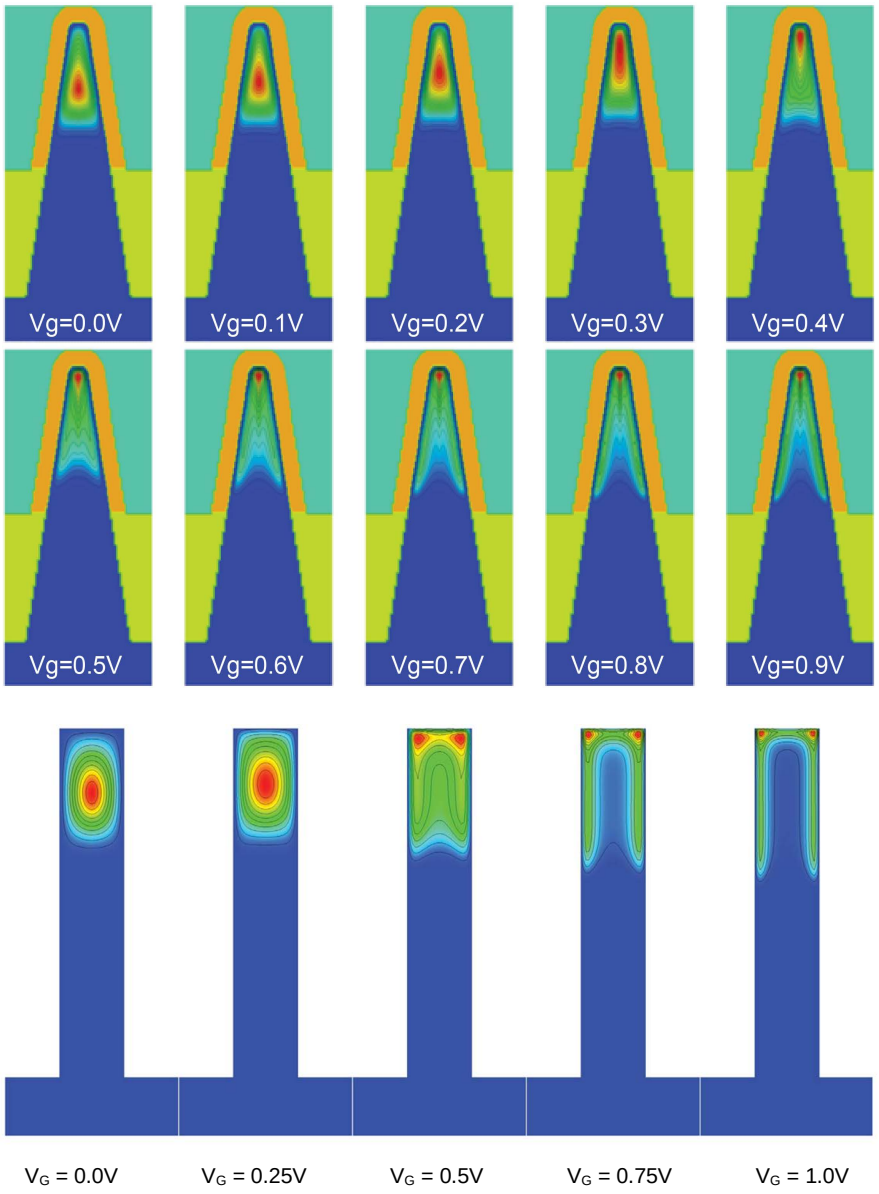

Figure 18. Charge distribution in the taper and rectangular Fin respectively [5].

dle at a low bias, and it passes at the surface at a high bias. Intel chooses the trapezoidal shape of the fin while in terms of performance the rectangular fin shape is optimum more than trapezoidal by about 15% [5] as shown in **Figure 19** and slightly better SS and DIBL [23]. Intel, maybe, wanted to avoid the high concentration of the charges at the two corners of the rectangular shaper, so it goes with the trapezoidal shape which has one angle where the charges distribution is highly concentrated at high bias. Moreover, the next generation of Intel transistor (14-nm) is going to be more rectangular.

The 3D nature of Tri-Gate FinFET transistor introduces a new number of parasitic capacitances to be considered. For example, between the gate and the source there will be two sided capacitors other than the top and the bottom capacitors as shown in **Figure 20** [24]. And the transistor which has multiple fins

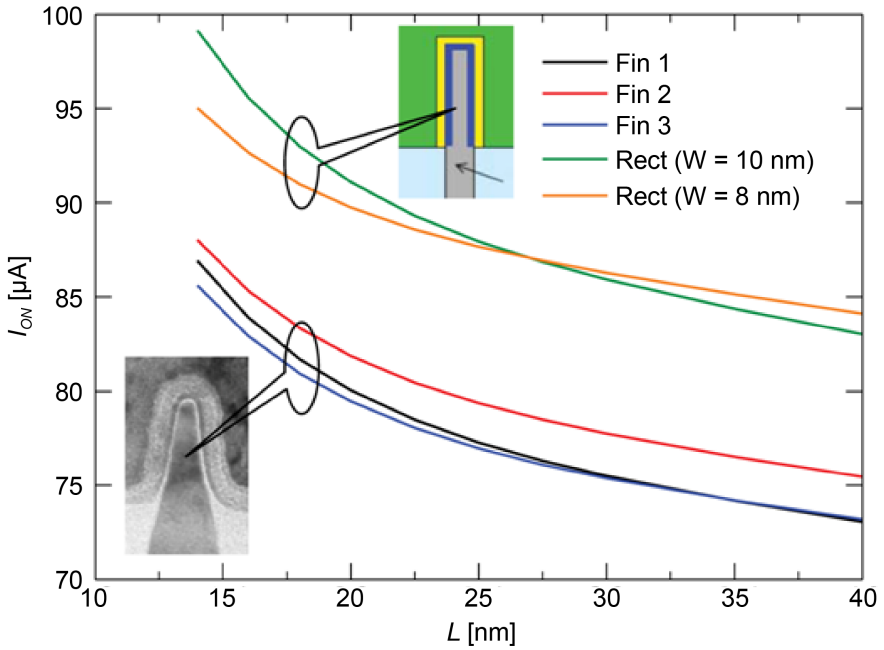

Figure 19. Comparison of I_{ON} between rectangular and taper Fins for equivalent width and heights [5].

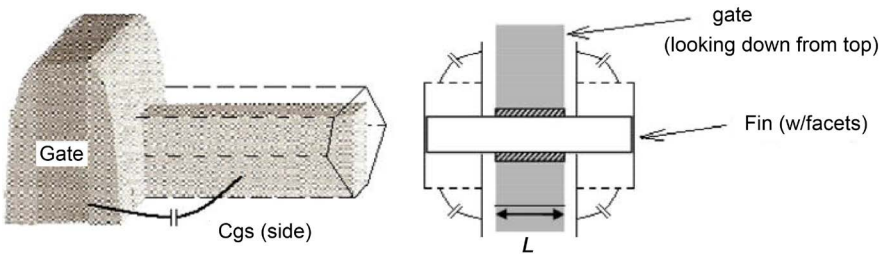

Figure 20. Tri-Gate FinFET additional parasitic capacitors [24].

increases the parasitic resistance (from each fin) and adds interconnect capacitances between fins [24] [25]. Also, the fabrication process is complicated and more complex than planar technologies especially for the vertical etching, which gives more opportunities to have variations between the shapes and heights of the Fins [26] which causes a variation of the threshold voltage of each transistor [27] as shown in **Figure 21**.

3. Conclusion

This paper provides an overview of the challenges faced by conventional CMOS scaling. It explains fully depleted devices, such as planar UTBB FD-SOI and Tri-Gate FinFET, as the alternative solutions of bulk transistors at 28-nm and beyond, shedding the light on their designs and performance.

4. Future Work

A detailed comparison between 28-nm UTBB FD-SOI and 22 nm Tri-Gate FinFET transistors to be elaborated in later work will make a solid comparison

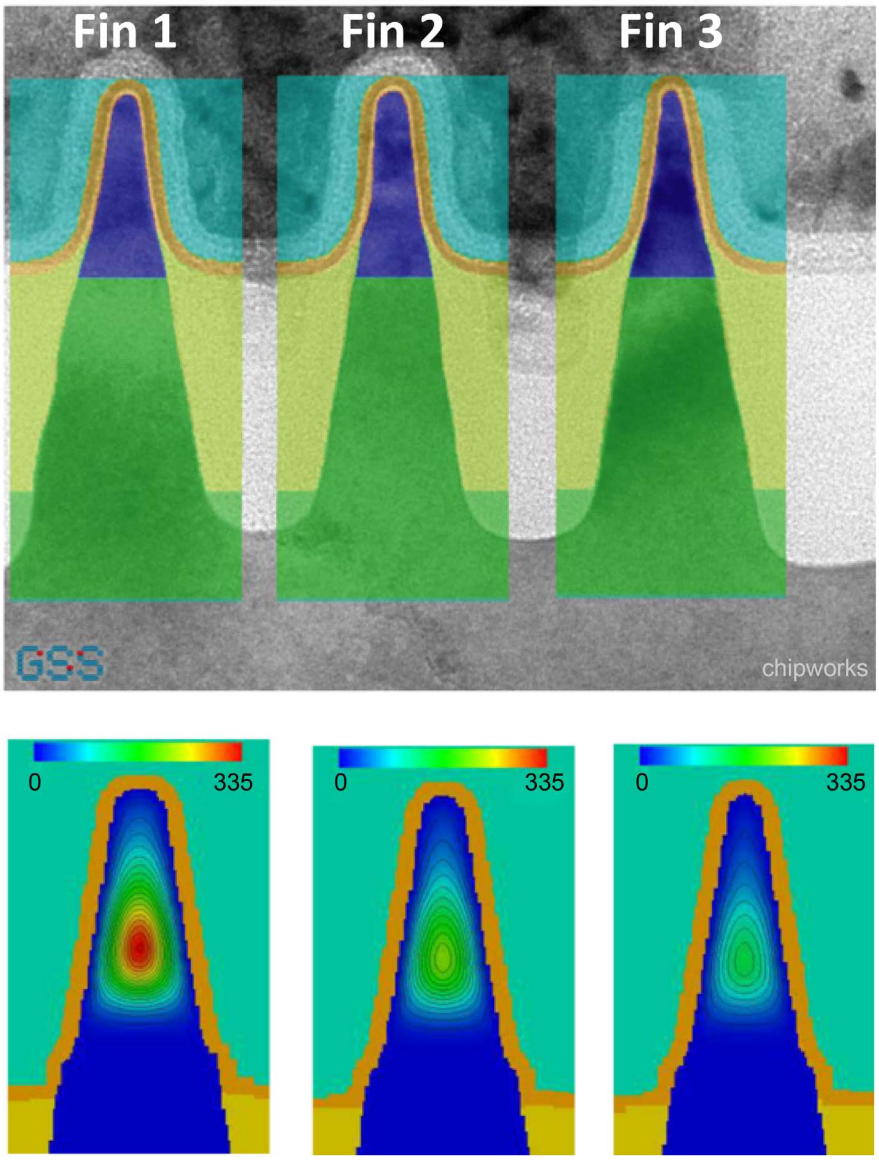

Figure 21. Different fins shape due fabrication [5].

between them and will explain each technology features like: physical characteristics, electrical characteristics, and their reliability test.

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